EE434
ASIC & Digital Systems

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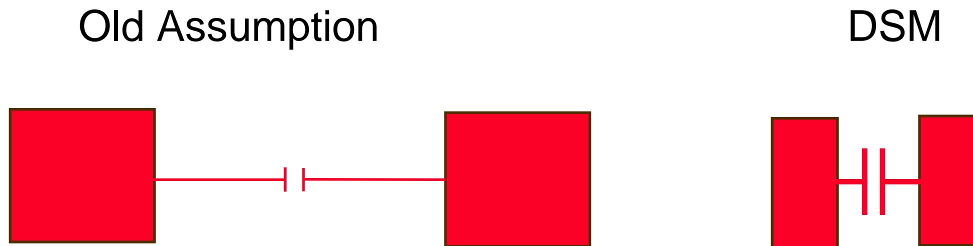
Lecture 11

Physical Design Issues

Interconnect Scaling Effects

- Dense multilayer metal increases coupling capacitance



- Long/narrow line widths further increases resistance of interconnect

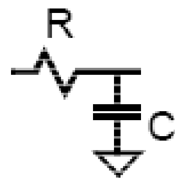
Wire Modeling

Wires are a distributed RC circuit

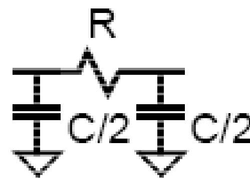
- Wire has r= resistance/mm and c=capacitance/mm

How should you model the interconnect for hand calc?

Use a simple L, Π, or T model assuming C=cL and R = rL



L



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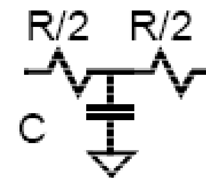


T

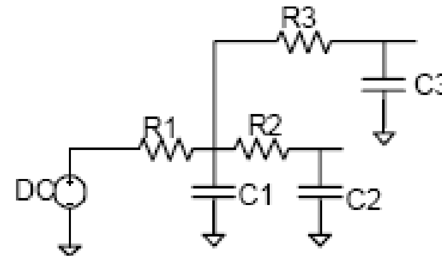
- One of the three models above is not useful for distributed RC modeling
- Even with proper modeling, we still have to deal with RC trees

Elmore Delay

- Follow board notes

Elmore Delay

$$\tau_i = \sum R_{ik} \sum C_k$$



- C_k = every capacitance in the network in sequence
- R_{ik} = common resistance in path between source and node i and source and node k

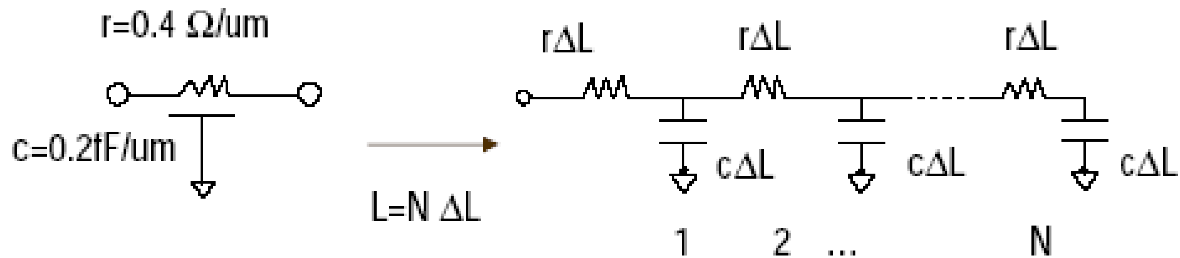
$$\tau_1 = R1C1 + R1C2 + R1C3$$

$$\tau_2 = R1C1 + (R1+R2)C2 + R1C3$$

$$\tau_3 = R1C1 + R1C2 + (R1+R3)C3$$

Delay of a wire

- What is the delay along the distributed line as a function on length L?



Use Elmore delay = $(r\,\Delta L)(c\,\Delta L) + 2(r\,\Delta L)(c\,\Delta L) + \ldots + N(r\,\Delta L)(c\,\Delta L)$

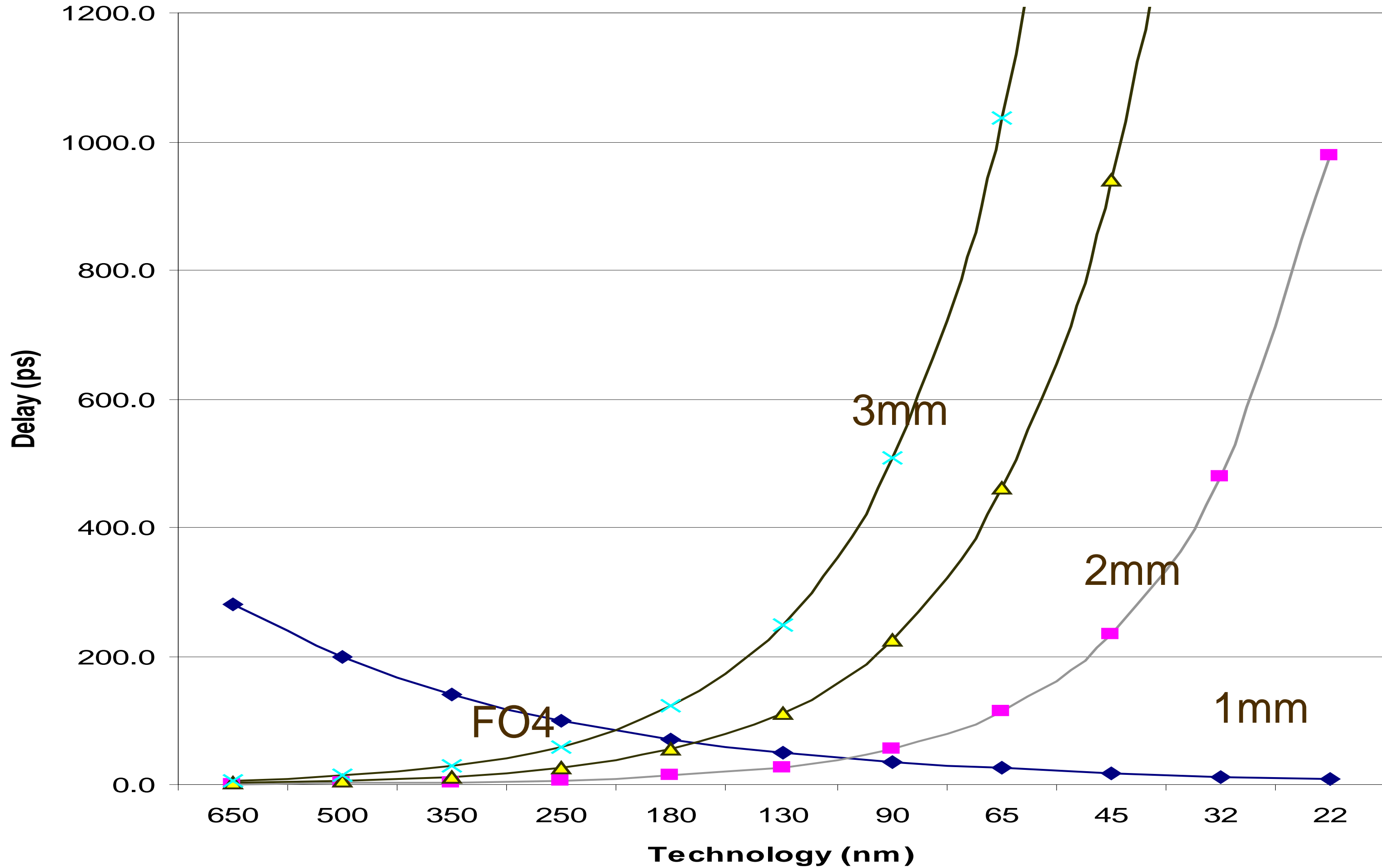
$= (\Delta L)^2 rc(1 + 2 + \ldots + N)$

$= (\Delta L)^2 rc(N)(N+1)/2 \approx (\Delta L)^2 rcN^2$

$= L^2\,rc/2 = RC/2$ (according to Elmore)

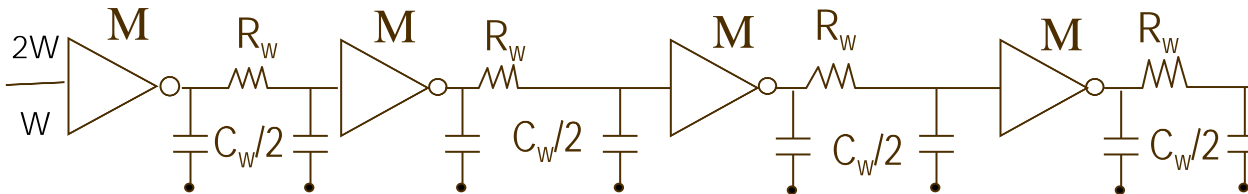
$\approx 0.4rcL^2$ (measured) Note that delay is proportional to length^2

FO4 vs. Wire Delay



Buffer Insertion for Long Wires

- Make Long wires into short wires by inserting buffers periodically. Divide interconnect into N sections as follows:



$R_{eff} = R_{eqn}/M$ $\quad C_{self}=C_j3W*M$ $\quad C_{fanout} = C_g3W*M$ $\quad R_w = R_{int}L/N$ $\quad C_w = C_{int}L/N$

- Then delay through buffers and interconnect is given by:

  $t_p = N *[R_{eff}(C_{self}+ C_W/2) + (R_{eff} + R_W)(C_W/2+C_{fanout})]$

- What is the optimal number of buffers?

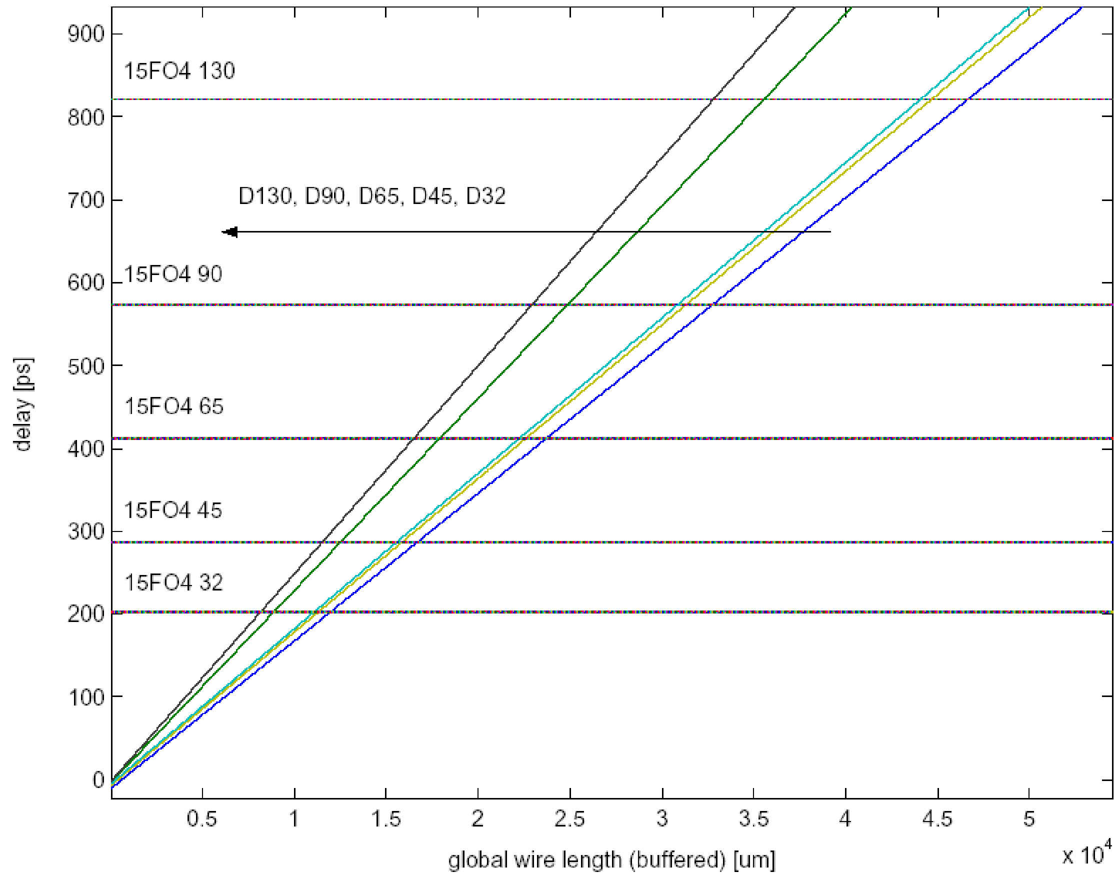
  Find N such that $\partial t_P/ \partial N = 0 \quad \Rightarrow \quad N \approx \mathrm{sqrt}(0.4R_{int}C_{int}\, L^2 /t_{pbuf})$

  where $t_{pbuf} = R_{eff}(C_{self} + C_{fanout})$

- What size should the buffers be?

  Find M such that $\partial t_P/ \partial M = 0 \quad \Rightarrow \quad M = \mathrm{sqrt}((R_{eqn}/C_g3W)(C_{int}/R_{int}))$

Global wire delay

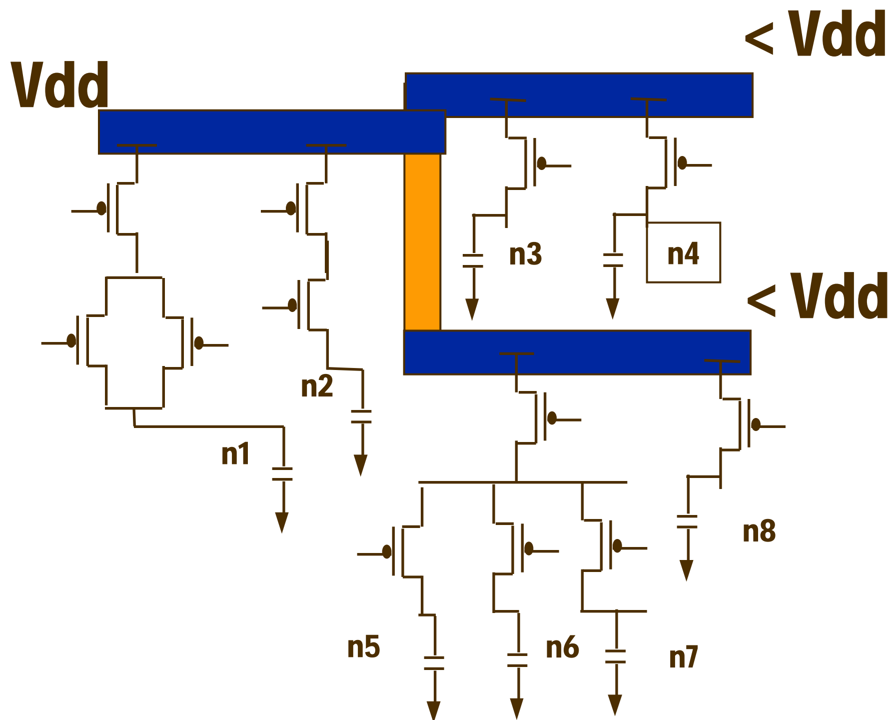


Global wires limit the system performance

Purpose of Power Distribution

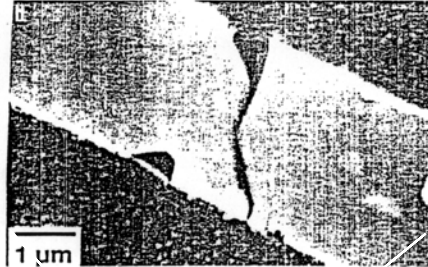
- Goal of power distribution system is to deliver the required current across the chip while maintaining the voltage levels necessary for proper operation of logic circuits
- Must route both power and ground to all gates
- Design Challenges:
  - How many power and ground pins should we allocate?
  - Which layers of metal should be used to route power/ground?
  - How wide should be make the wire to minimize voltage drops and reliability problems
  - How do we maintain V_{DD} and Gnd within noise budget?
  - How do we verify overall power distribution system?

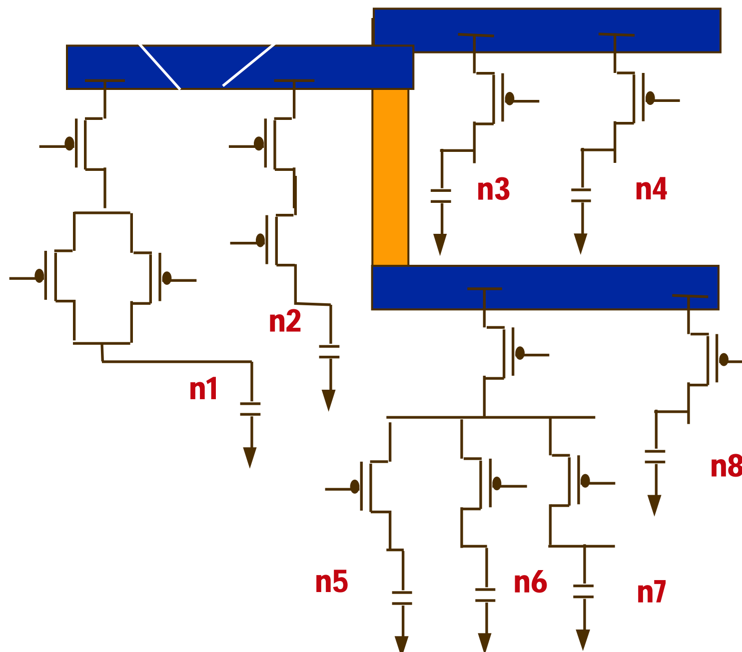
Power Distribution Issues - IR Drop



- Narrow line widths increase metal line resistance
- As current flows through power grid, voltage drops occur
- Actual voltage supplied to transistors is less than Vdd
- Impacts speed and functionality
- Need to choose wire widths to handle current demands of each segment

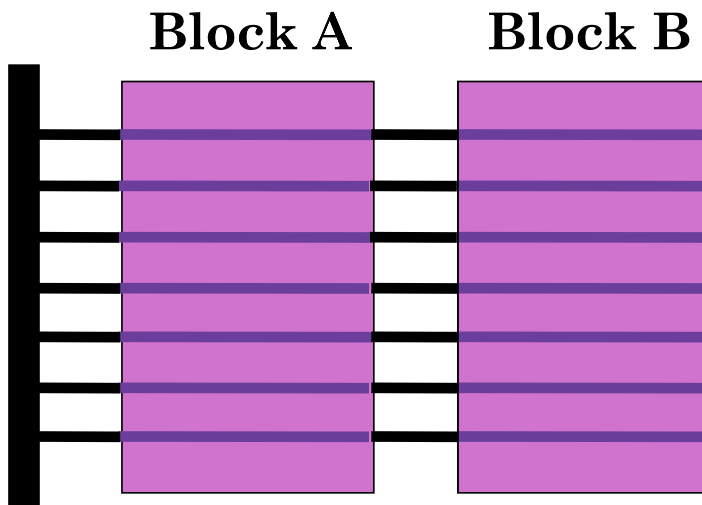
Power Grid Issues - Electromigration

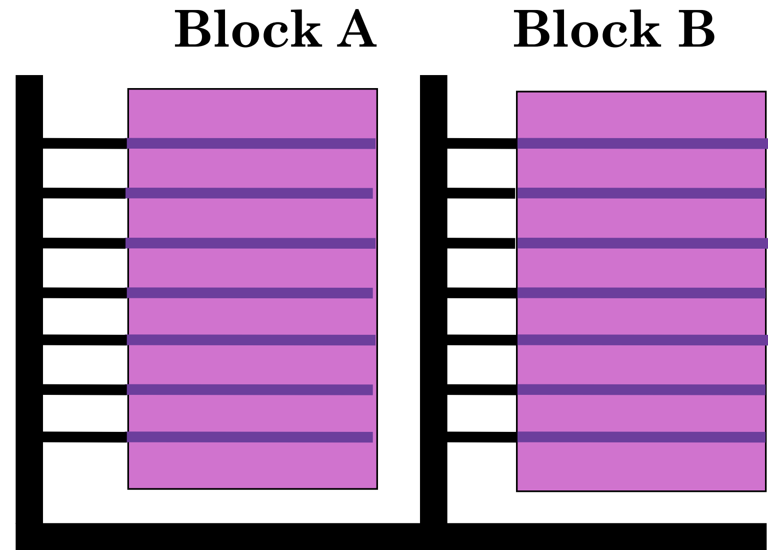




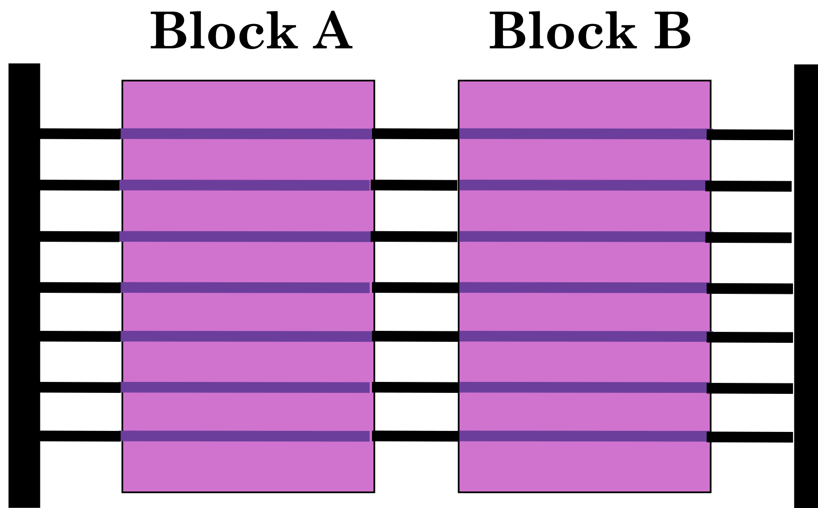
- As current flows down narrow wires, metal begins to migrate
- Metal lines break over time due to metal fatigue
- Based on average/peak current density
- Need to widen wires enough to avoid this phenomenon

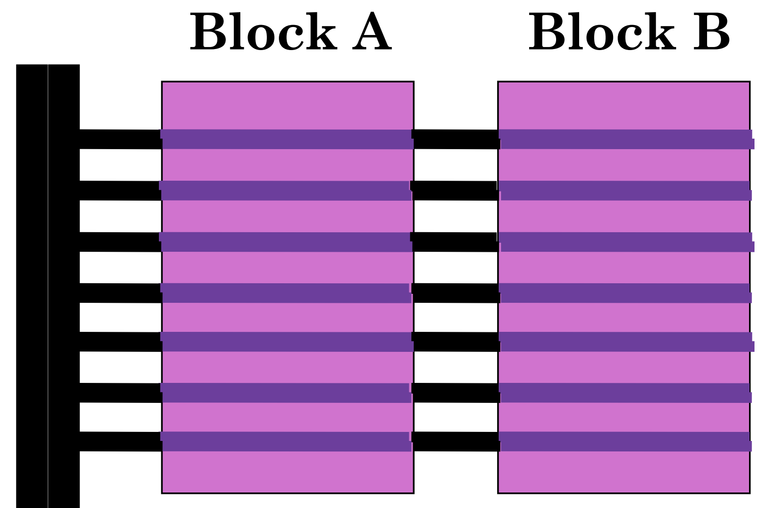
Power Routing Examples



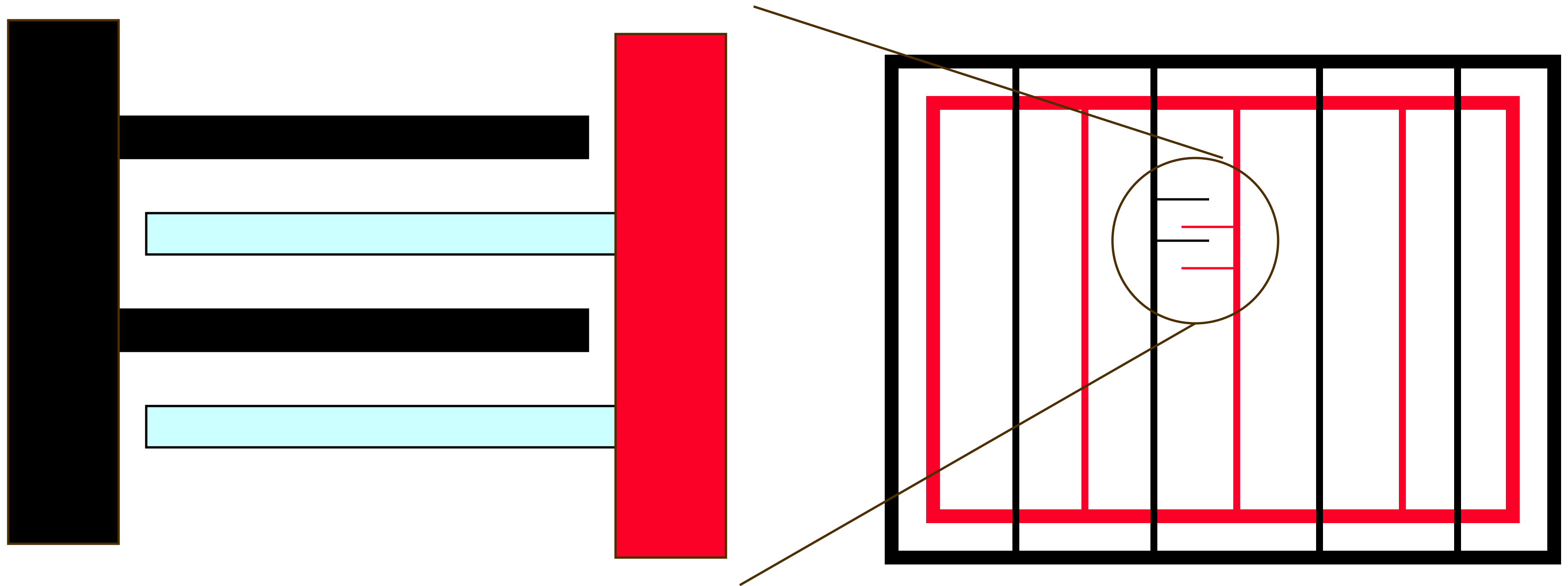


Simple Routing Examples





Interleaved Power/Ground Routing



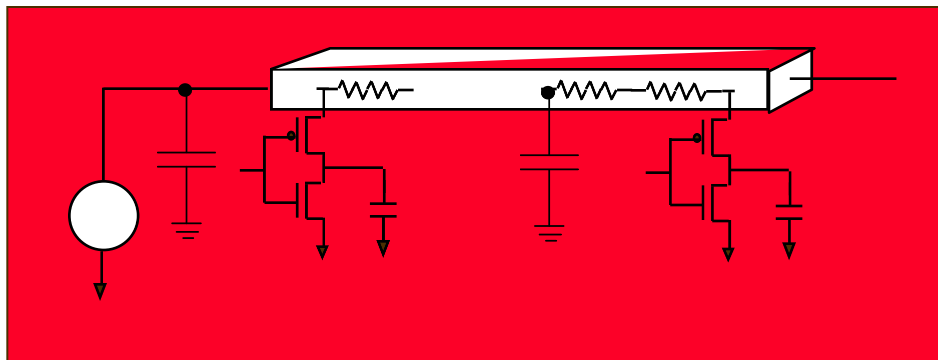
Interleaved Vdd/Vss

Ldi/dt Effects in the Power Supply

- In addition to IR drop, power system inductance is also an issue
- Inductance may be due to power pin, power bump or power grid
- Overall voltage drop is:

$$V_{drop} = IR + Ldi/dt$$

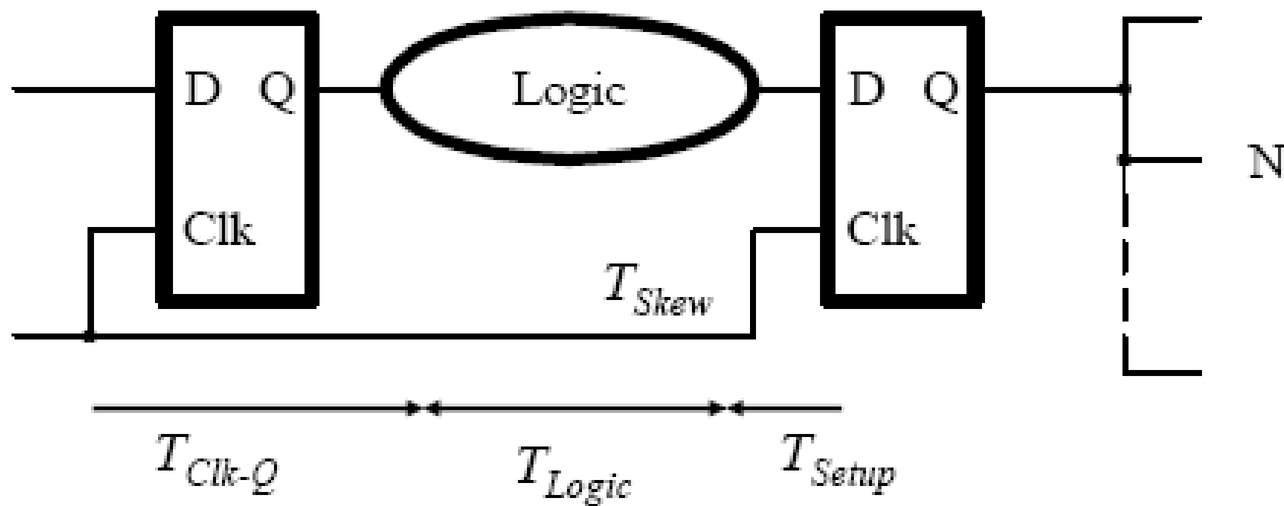
- Distribute decoupling capacitors (de caps) liberally throughout design
  - Capacitors store up charge
  - Can provide instantaneous source of current for switching



Clock Design Issues

- Clock cycle depends on a number of factors:

  $T_{cycle} = T_{Clk\text{-}Q} + T_{Logic} + T_{setup} + T_{skew}$



Sources of clock skew

Main sources:

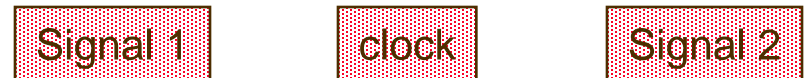
1. Imbalance between different paths from clock source to FF's
   - interconnect length determines RC delays
   - capacitive coupling effects cause delay variations
   - buffer sizing
   - number of loads driven
2. Process variations across die
   - interconnect and devices have different statistical variations

Power Dissipation in Clocks

- Significant power dissipation can occur in clocks in high-performance designs:
  - clock switches on every cycle so $P = CV^2f$ (i.e., $\alpha=1$)
  - clock capacitance can be ~nF range, say 1nF = 1000pF
  - assuming a power supply of 1.8V, CV = 1800pC of charge
  - if clock switches every 2ns (500MHz), that's 0.9A
  - for V_{DD} = 1.8V, P=IV=0.9(1.8)=1.6W in the clock circuit alone
- Much of the power (and the skew) occurs in the final drivers due to the sizing up of buffers to drive the flip-flops
- Key to reducing the power is to examine equation CV^2f and reduce the terms wherever possible
  - V_{DD} is usually given to us; would not want to reduce swing due to coupling noise, etc.
  - Look more closely at C and f

Reducing Power in Clocking

- Gated Clocks:
  - can gate clock signals through AND gate before applying to flip-flop; this is more of a total chip power savings
  - all clock trees should have the same type of gating whether they are used or not, and at the same level - total balance
- Reduce overall capacitance (again, shielding vs. spacing)



(a) higher total cap./less area

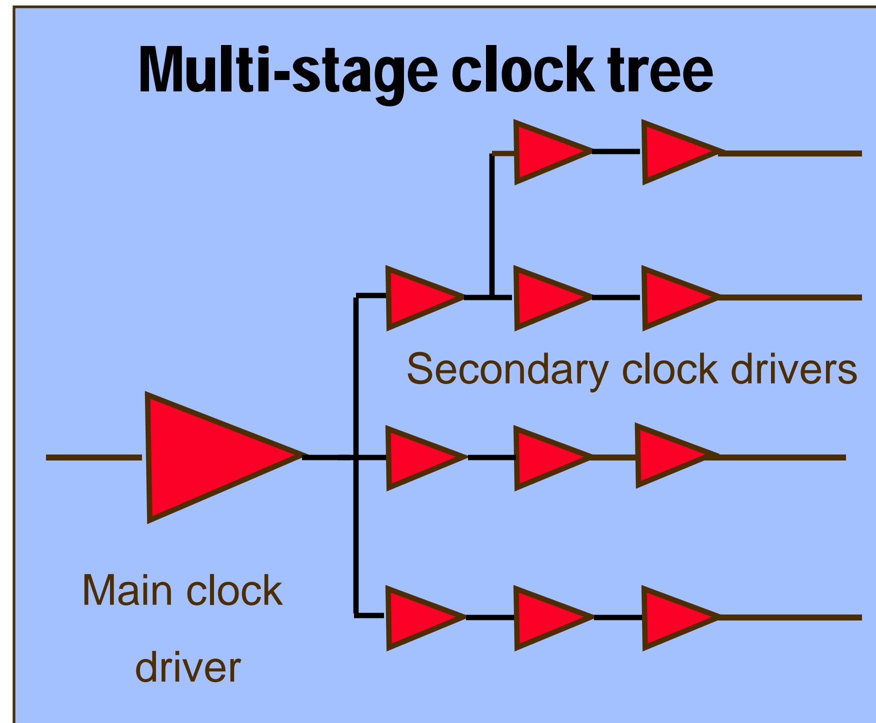
(b) lower cap./ more area

  - Tradeoff between the two approaches due to coupling noise
  - approach (a) is better for inductive noise; (b) is better for capacitive noise

Clock Design

Tree

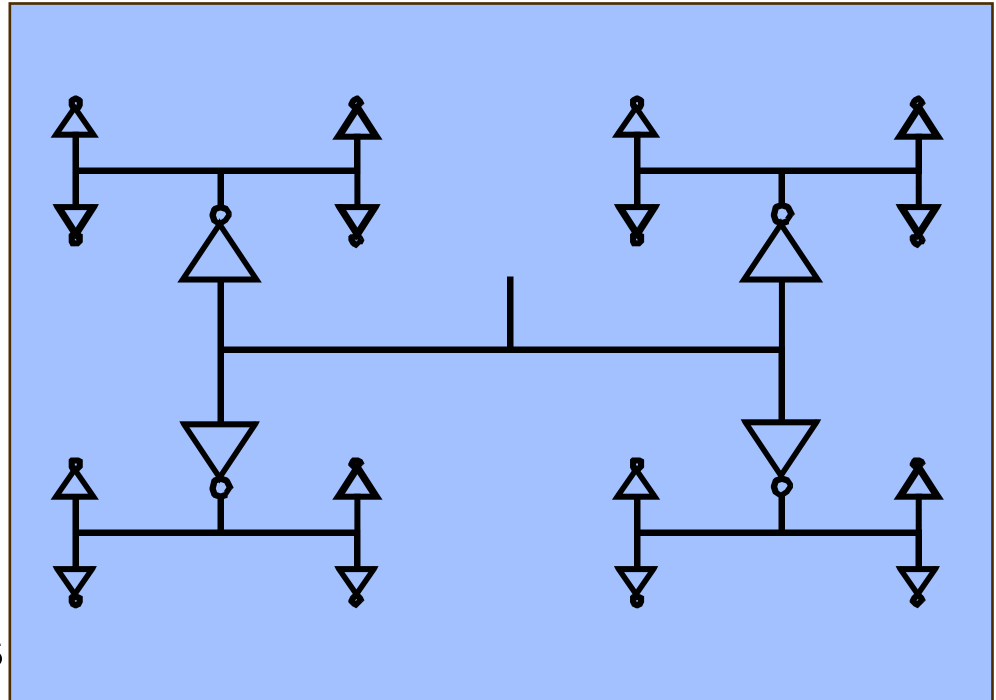
- Minimal area cost
- Requires clock-tree management
- Use a large super buffer to drive downstream buffers
- Balancing may be an issue



Clock Configurations

H-Tree

- Place clock root at center of chip and distribute as an H structure to all areas of the chip
- Clock is delayed by an equal amount to every section of the chip
- Local skew inside blocks is kept within tolerable limits



Clock Configurations

Grid

- Greater area cost
- Easier skew control
- Increased power consumption
- Electromigration risk increased at drivers
- Severely restricts floorplan and routing