EE 466/586
VLSI Design

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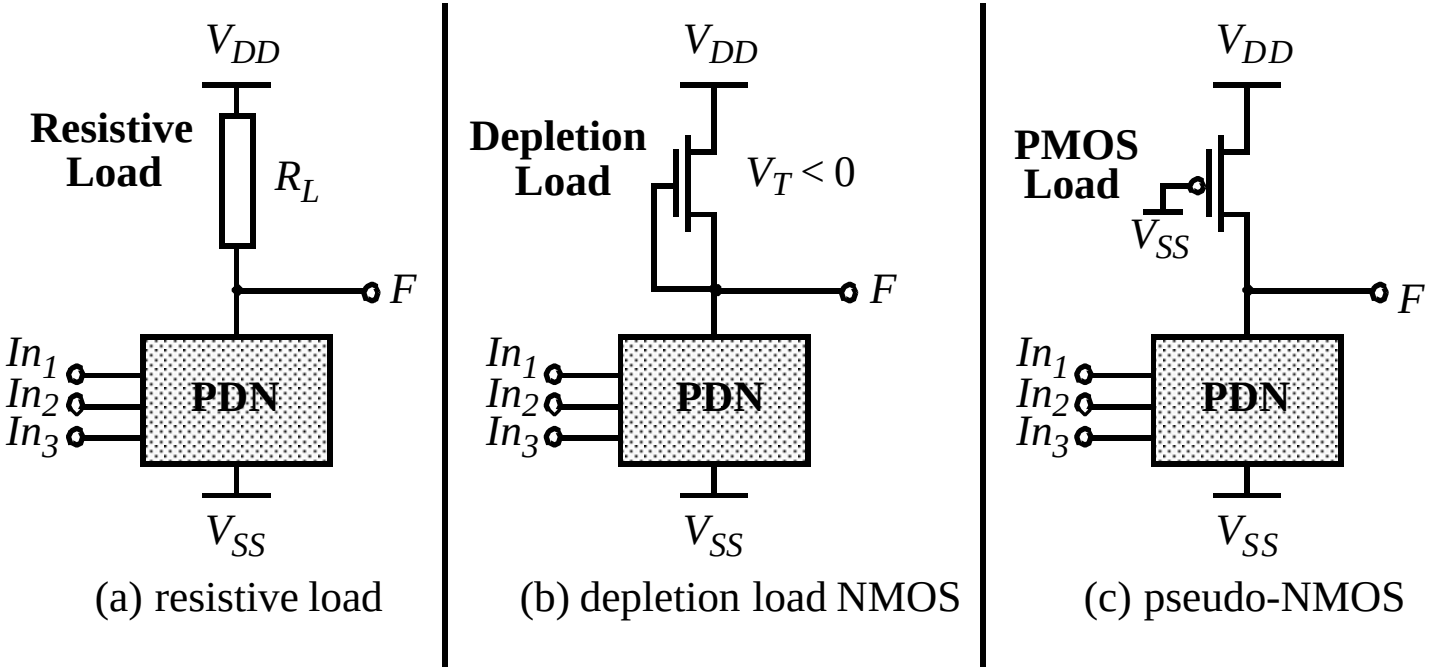
Lecture 13

More on Gates

CMOS Properties

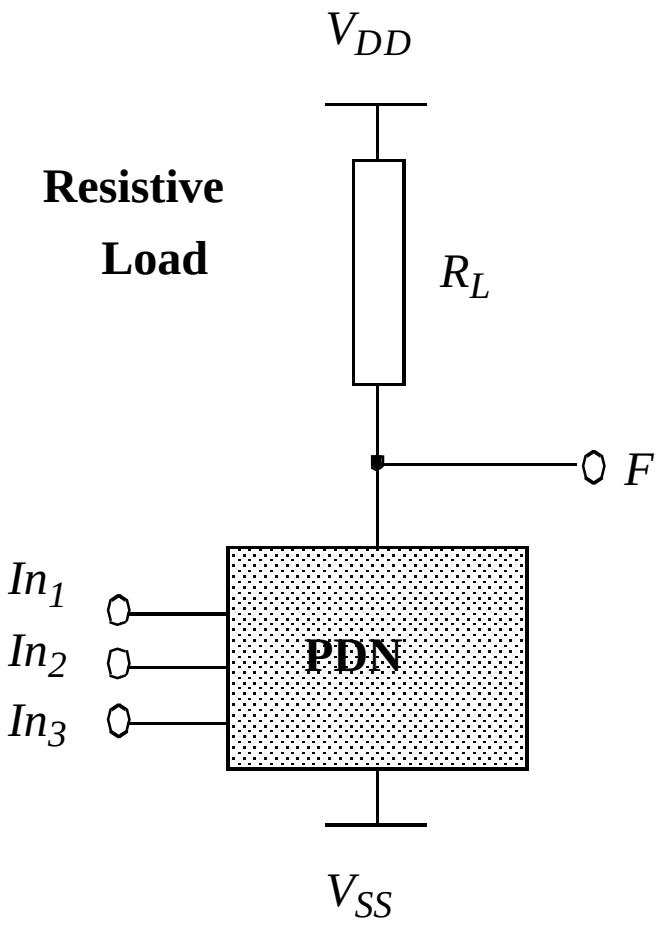
- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratio less
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors
- N fan-in gates need 2N transistors

Ratioed Logic



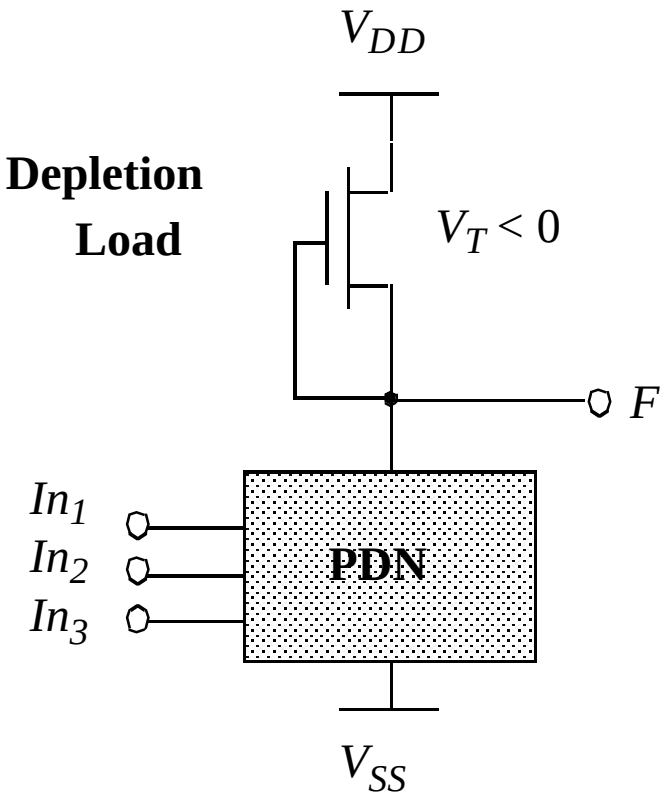
Goal: to reduce the number of devices over complementary CMOS

Ratioed Logic

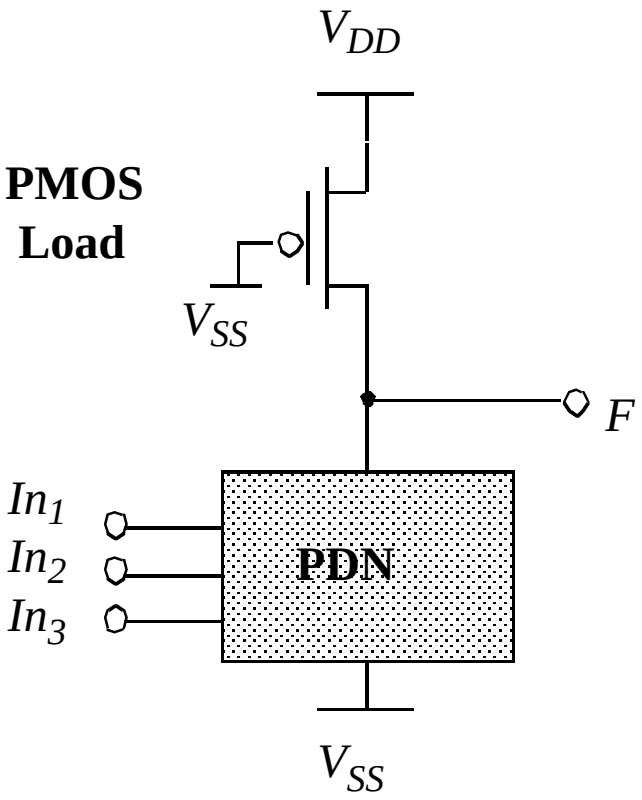


- **N transistors + Load**
- **$V_{OH} = V_{DD}$**
- **$V_{OL} = \dfrac{R_{PN}}{R_{PN} + R_L}$**
- **Assymetrical response**
- **Static power consumption**
- **$t_{pL} = 0.69\, R_L C_L$**

Active Loads

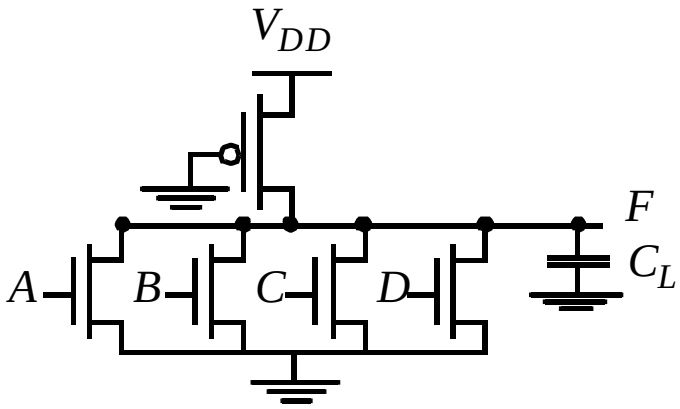


depletion load NMOS



pseudo-NMOS

Pseudo-NMOS



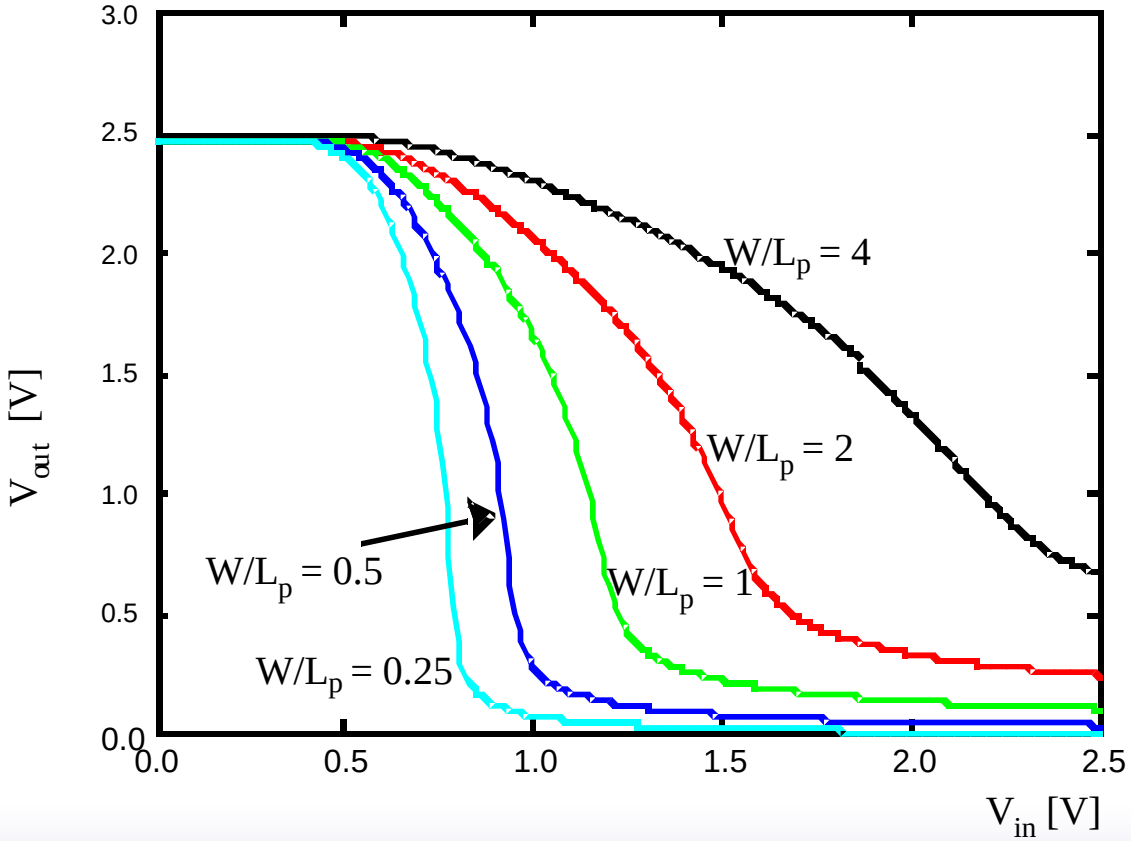
$V_{OH} = V_{DD}$ (similar to complementary CMOS)

$$k_n\left((V_{DD} - V_{Tn})V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{k_p}{2}(V_{DD} - |V_{Tp}|)^2$$

$$V_{OL} = (V_{DD} - V_T)\left[1 - \sqrt{1 - \frac{k_p}{k_n}}\right] \text{ (assuming that } V_T = V_{Tn} = |V_{Tp}|)$$

SMALLER AREA & LOAD <u>BUT</u> STATIC POWER DISSIPATION!!!

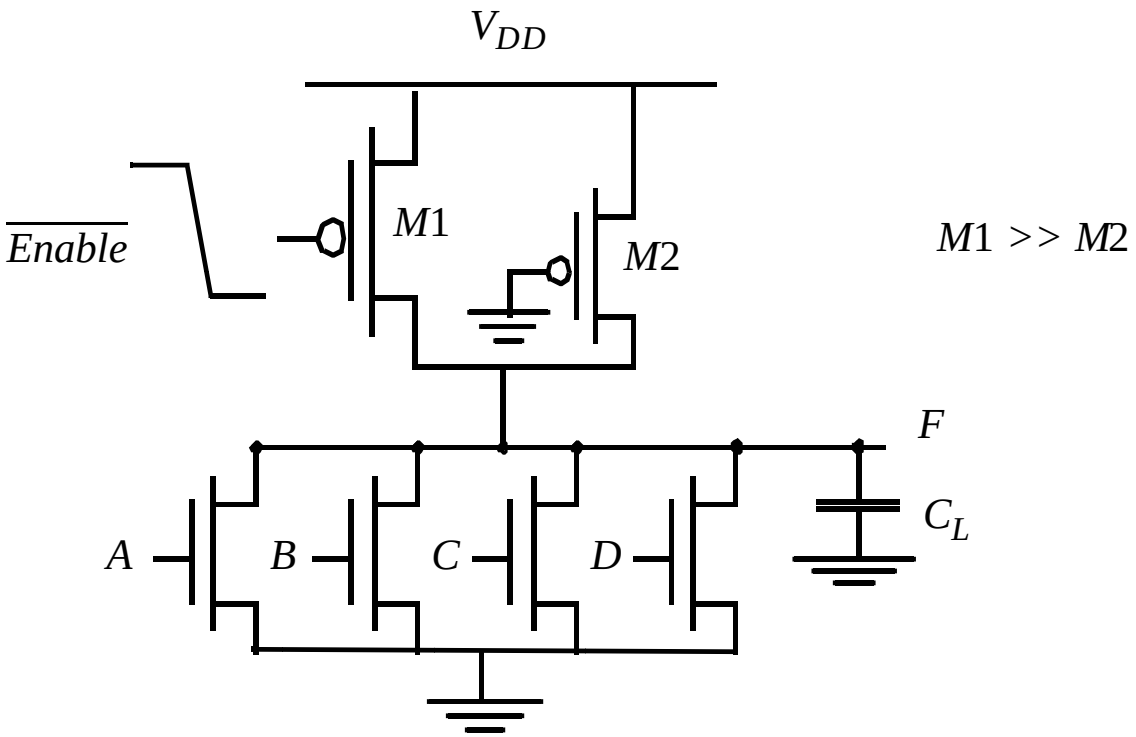
Pseudo-NMOS VTC



Performance of pseudo-NMOS Inverter

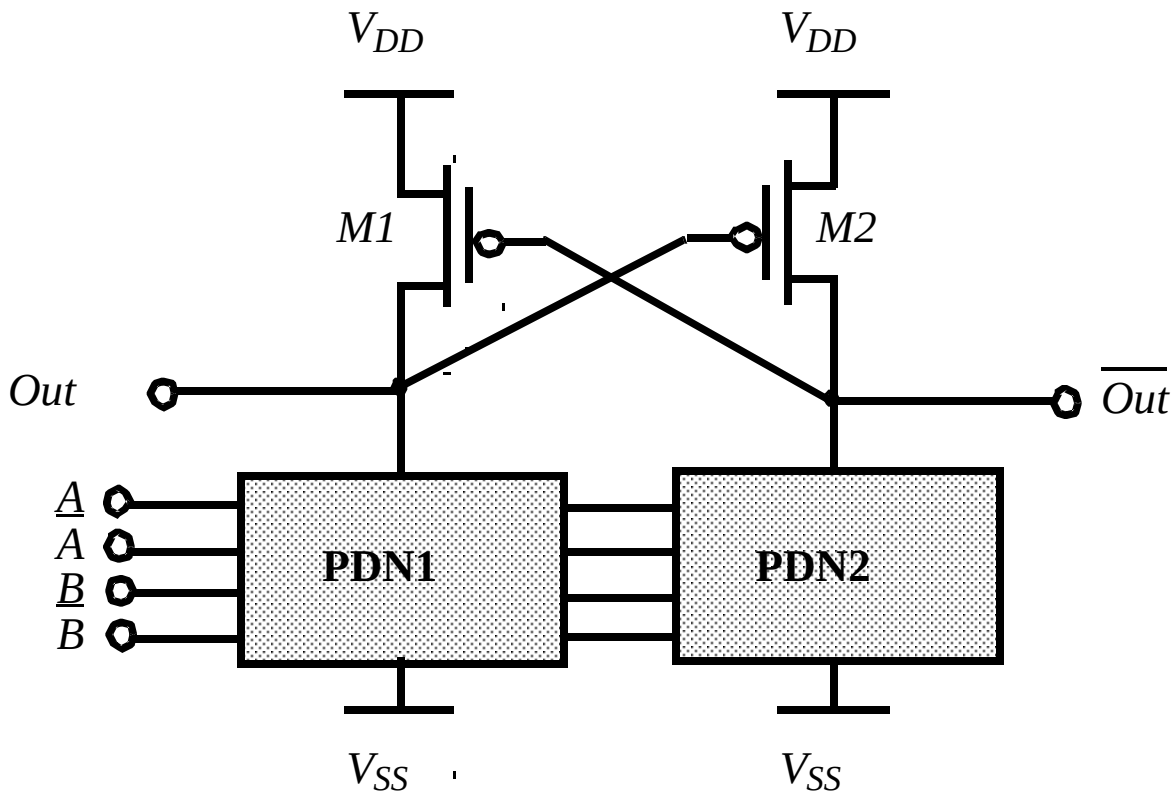
Size	V_{OL}(V)	Static Power Dissipation	t_{plh}
4	0.693	564 µw	14 ps
2	0.273	298 µw	56 ps
1	0.133	160 µw	123 ps
0.5	0.064	80 µw	268 ps
0.25	0.031	41 µw	569 ps

Improved Loads



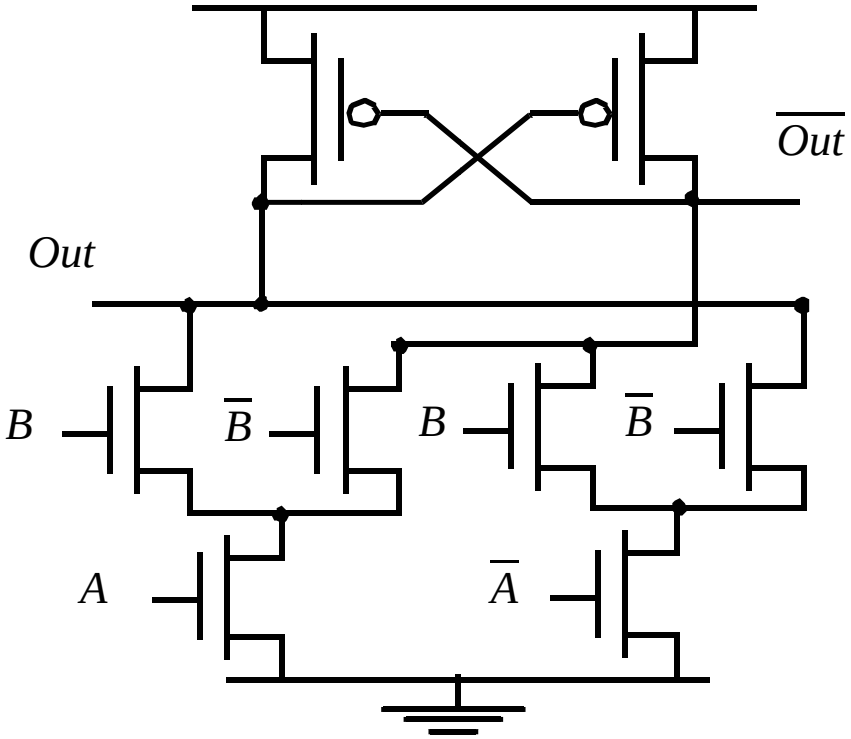
Adaptive Load

Improved Loads (2)



Differential Cascode Voltage Switch Logic (DCVSL)

DCVSL Example



XOR-NXOR gate