EE 466/586
VLSI Design

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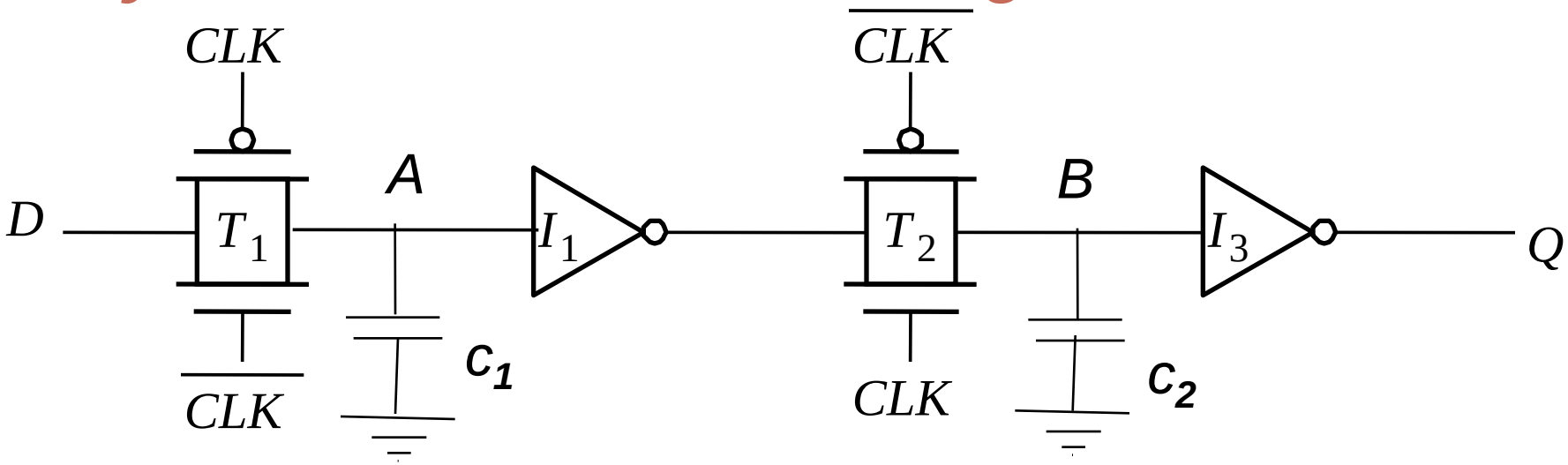
Lecture 17

Sequential Logic (Cont'd)

Dynamic Latches and Registers



- *The setup time of this circuit is the delay of the transmission gate.*
- *It is the time taken by node A to sample the D input.*
- *The hold time is approximately zero, as the T_1 is turned off on the clock edge and further input changes are ignored.*
- *The propagation delay (**tc-q**) is equal to two inverter delays plus the delay of T_2.*

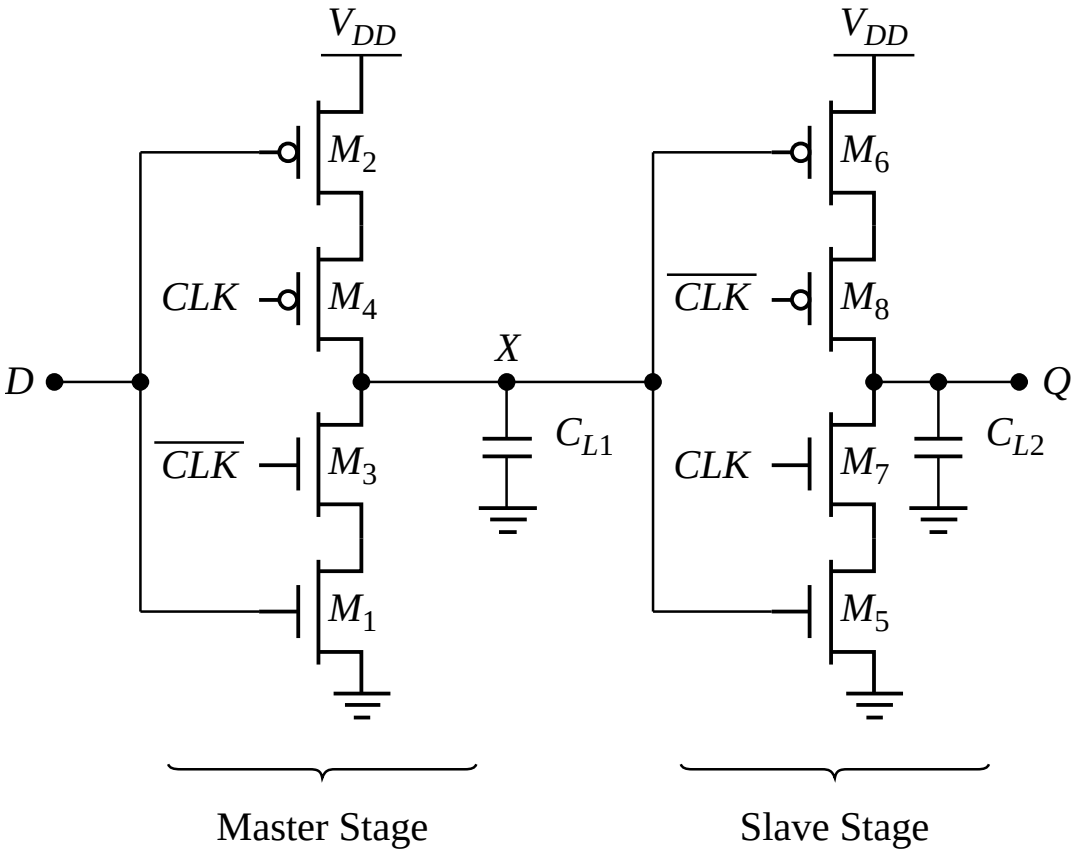
Clock Overlap

- During the 0-0 overlap period, the PMOS of T_1 and the PMOS of T_2 are simultaneously on
  - A direct path for data to flow from the D input of the register to the Q output
    - Race condition
- The output Q can change on the falling edge if the overlap period is large
  - Undesirable effect for a positive edge triggered register.
- For 1-1 overlap region
  - Path exists through NMOS of $T_1$and the NMOS of T_2.

Clock Overlap (Cont'd)

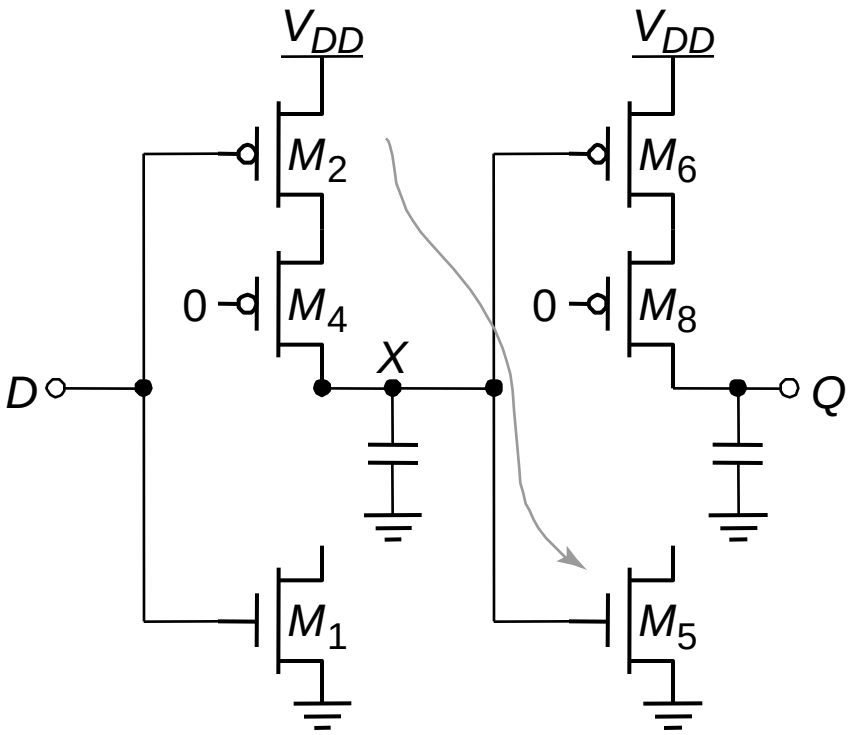
- 1-1 Overlap
  - Taken care of by enforcing a *hold time* constraint.
  - Data must be stable during the high-overlap period.
- 0-0 Overlap
  - Make sure that there is enough delay between the D input and node B
  - Ensure that the new data sampled by the master stage does not propagate through to the slave stage.

Other Latches/Registers: C²MOS

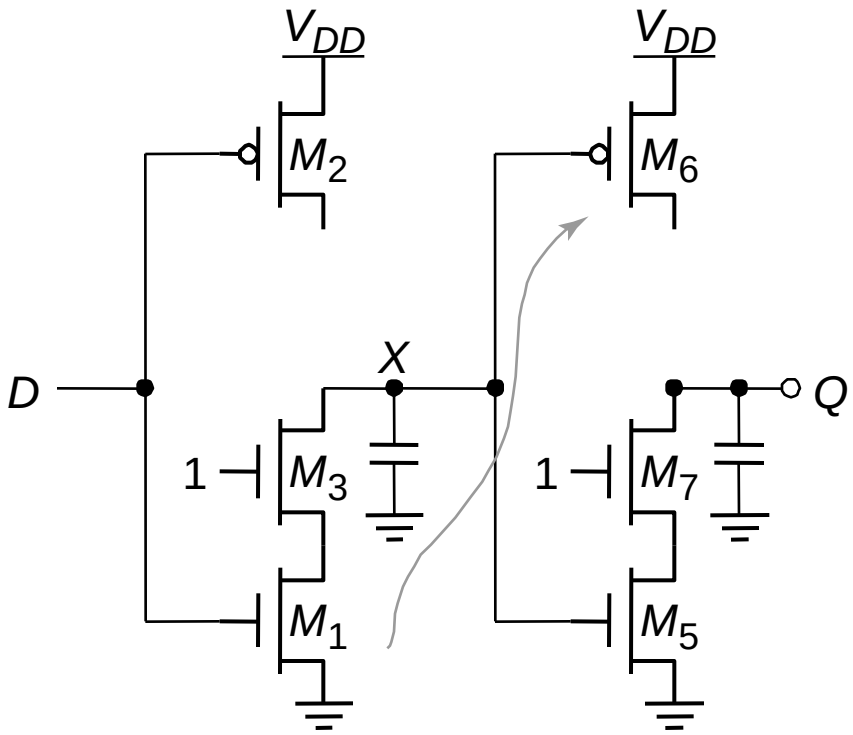


"Keepers" can be added to make circuit pseudo-static

Insensitive to Clock-Overlap

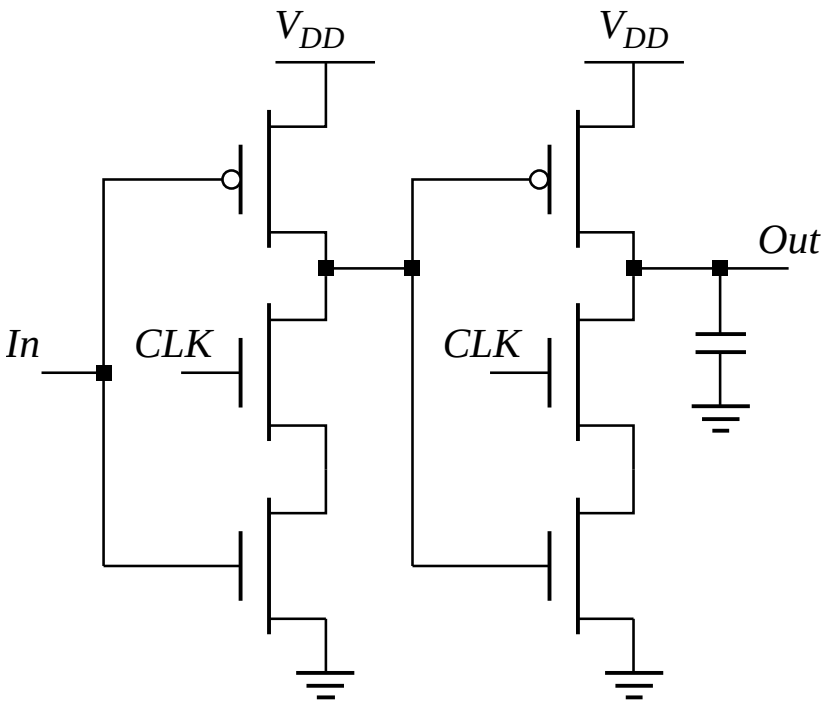


(a) (0-0) overlap

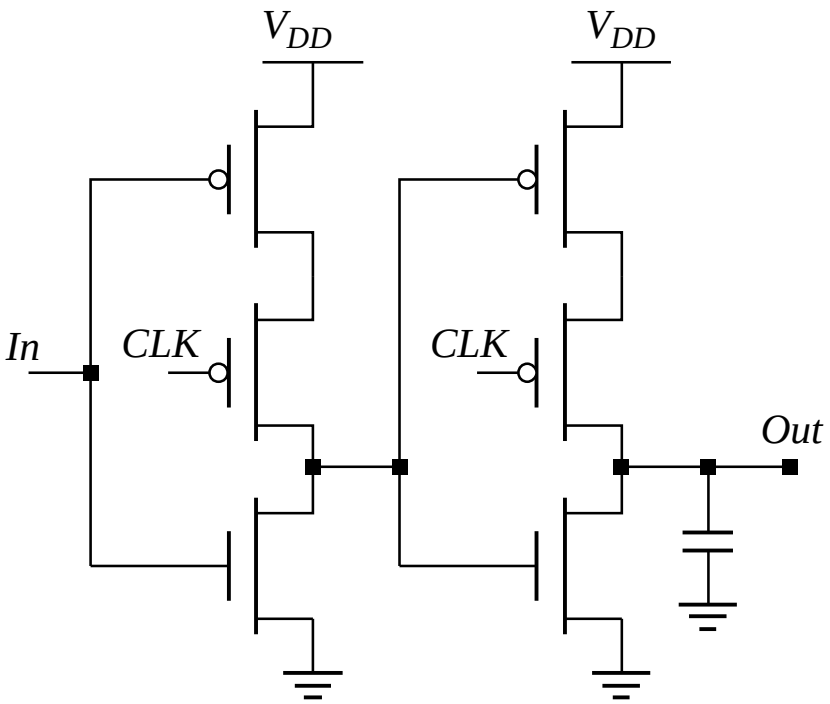


(b) (1-1) overlap

Other Latches/Registers: TSPC

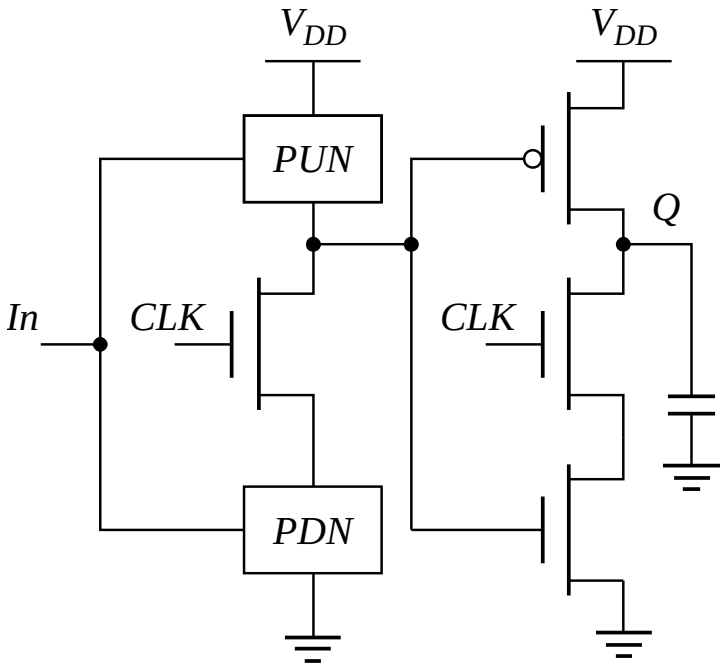


Positive latch
(transparent when CLK= 1)

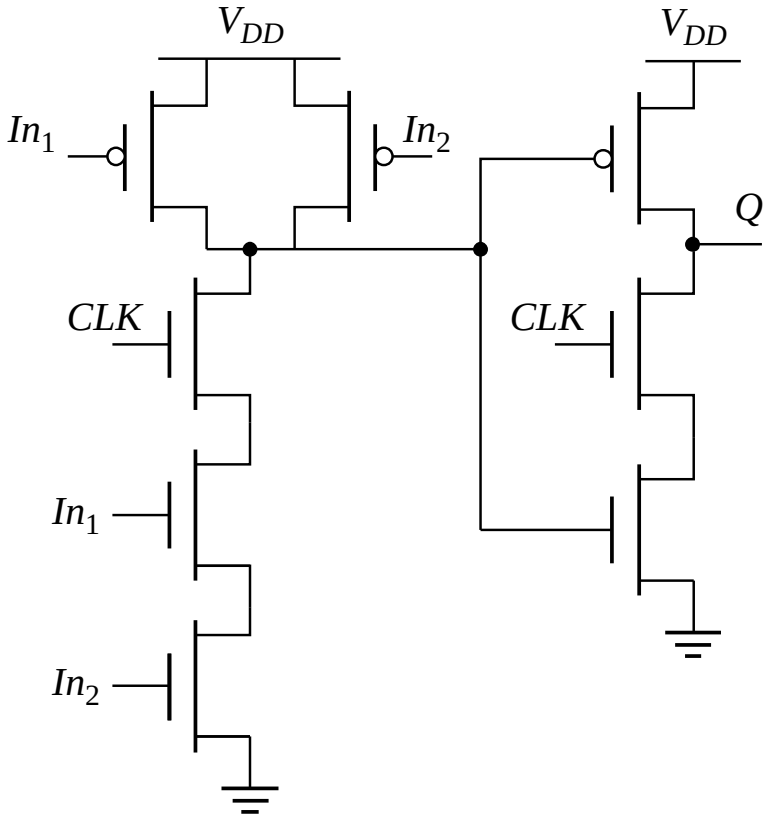


Negative latch
(transparent when CLK= 0)

Including Logic in TSPC

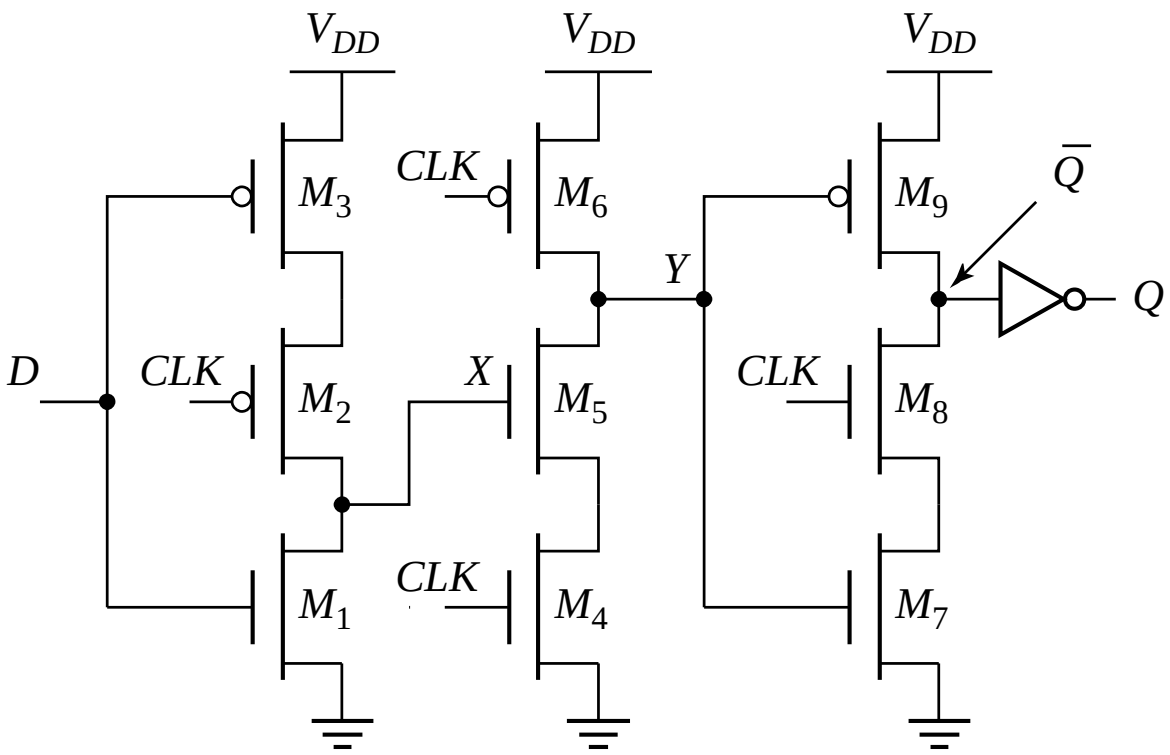


Example: logic inside the latch



AND latch

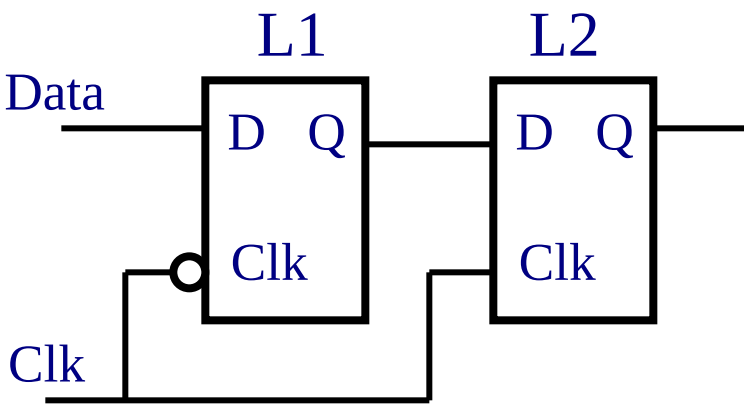
TSPC Register



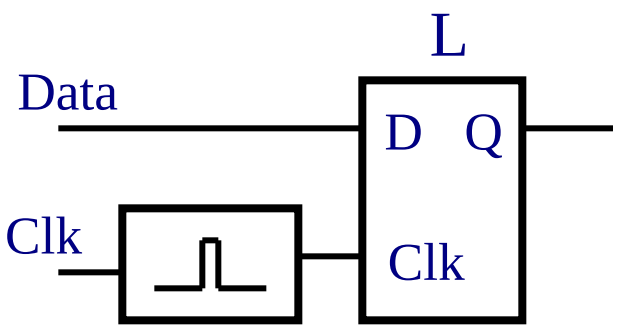
Pulse-Triggered Latches
An Alternative Approach

Ways to design an edge-triggered sequential cell:

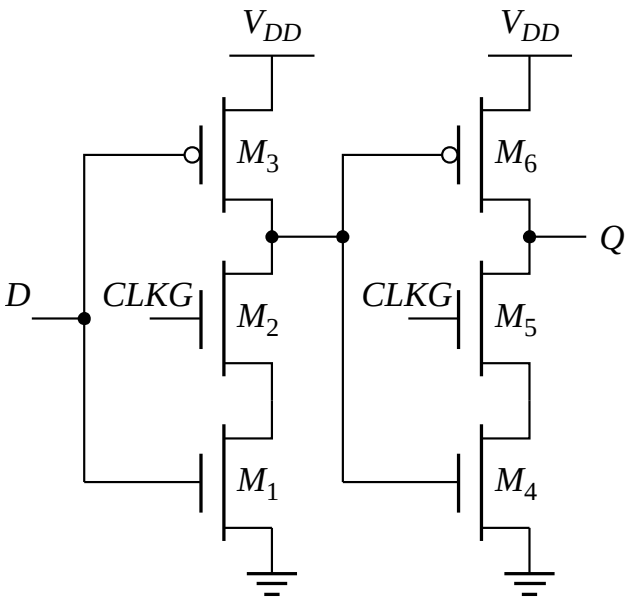
Master-Slave Latches



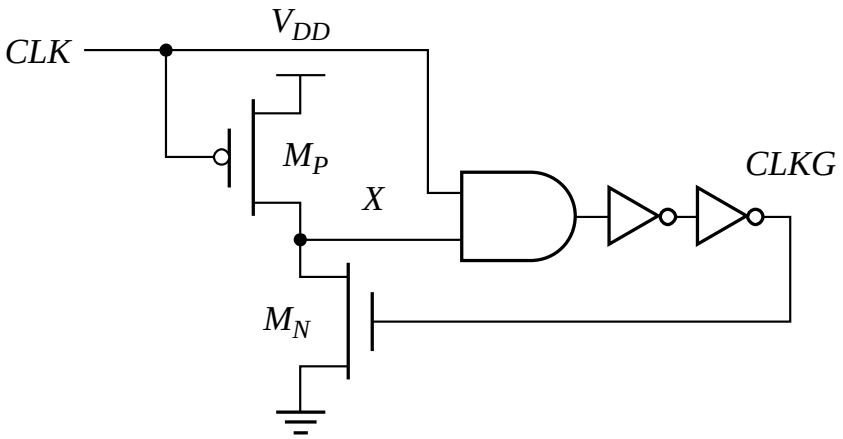
Pulse-Triggered Latch



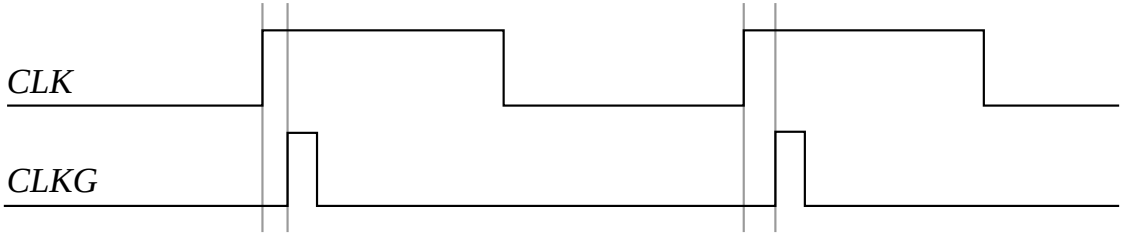
Pulsed Latches



(a) register



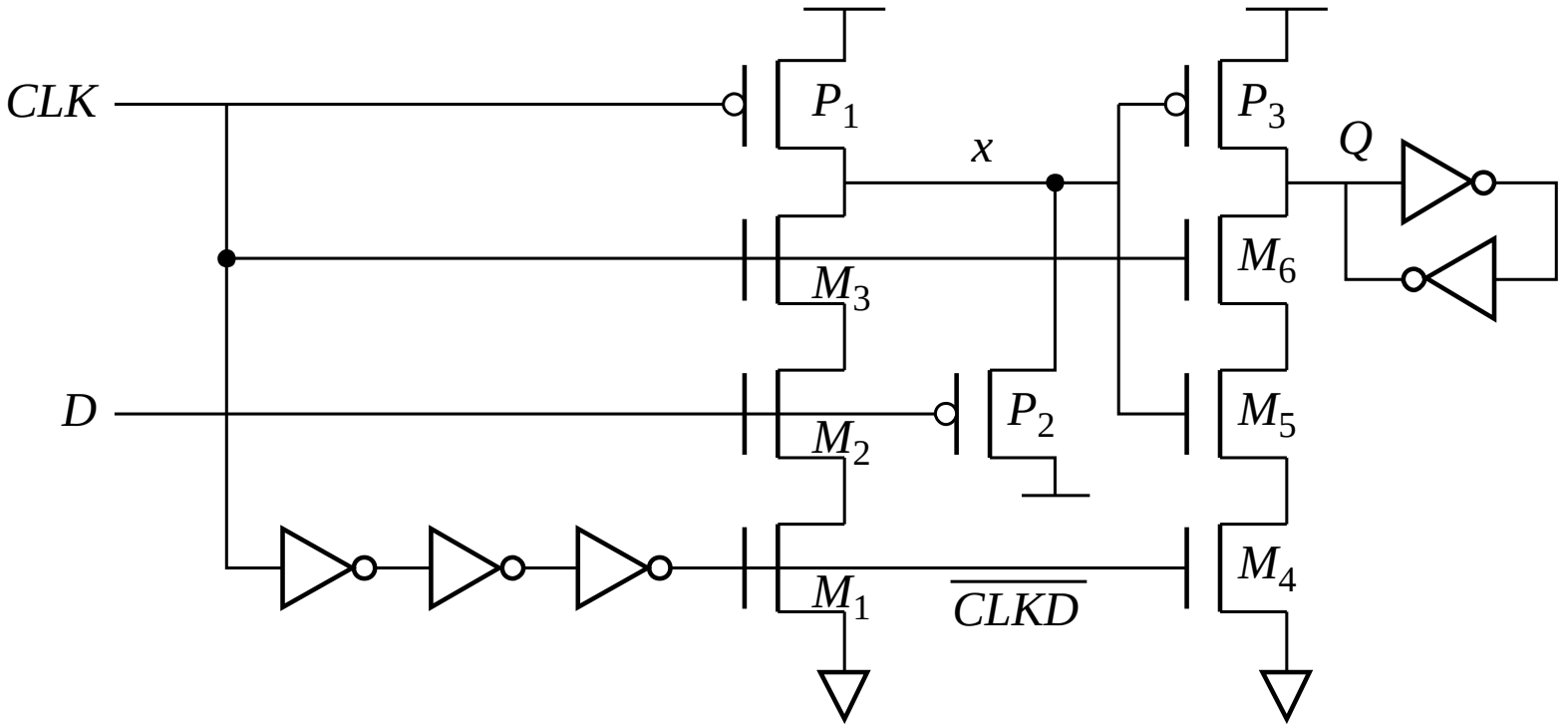
(b) glitch generation



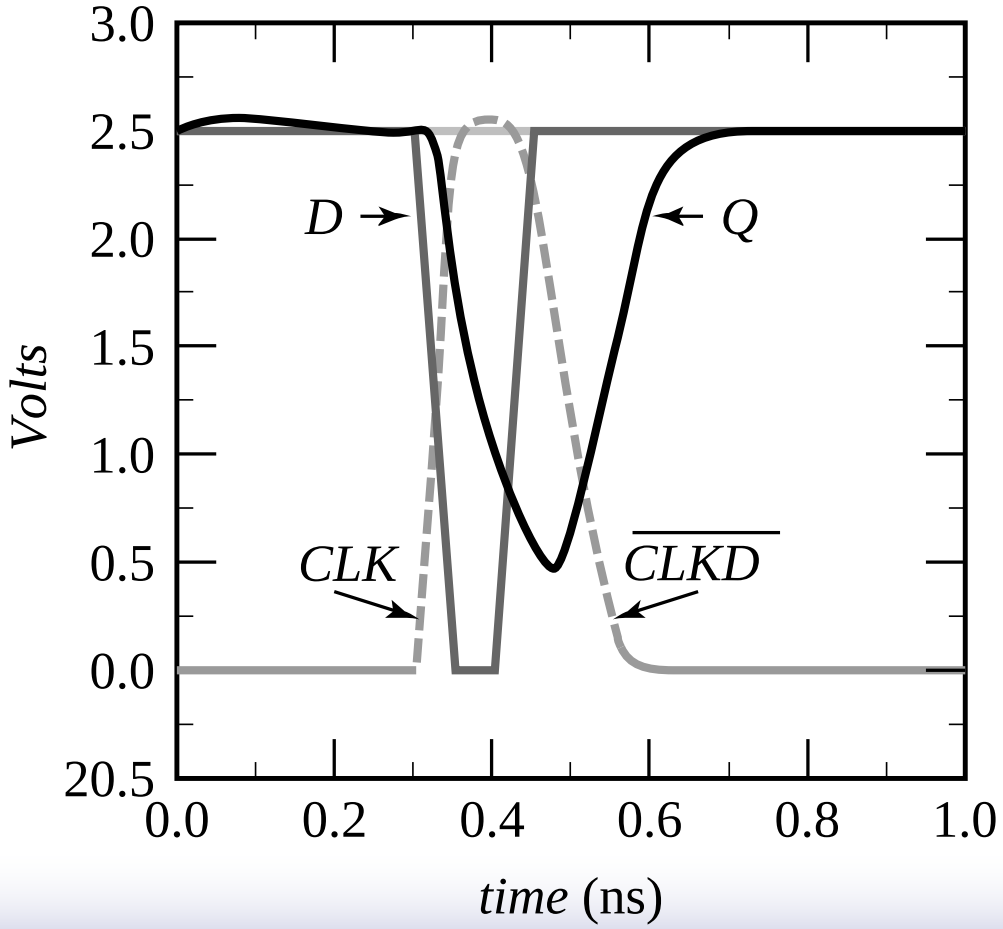
(c) glitch clock

Pulsed Latches

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :



Hybrid Latch-FF Timing



Latch-Based Pipeline