EE 466/586
VLSI Design

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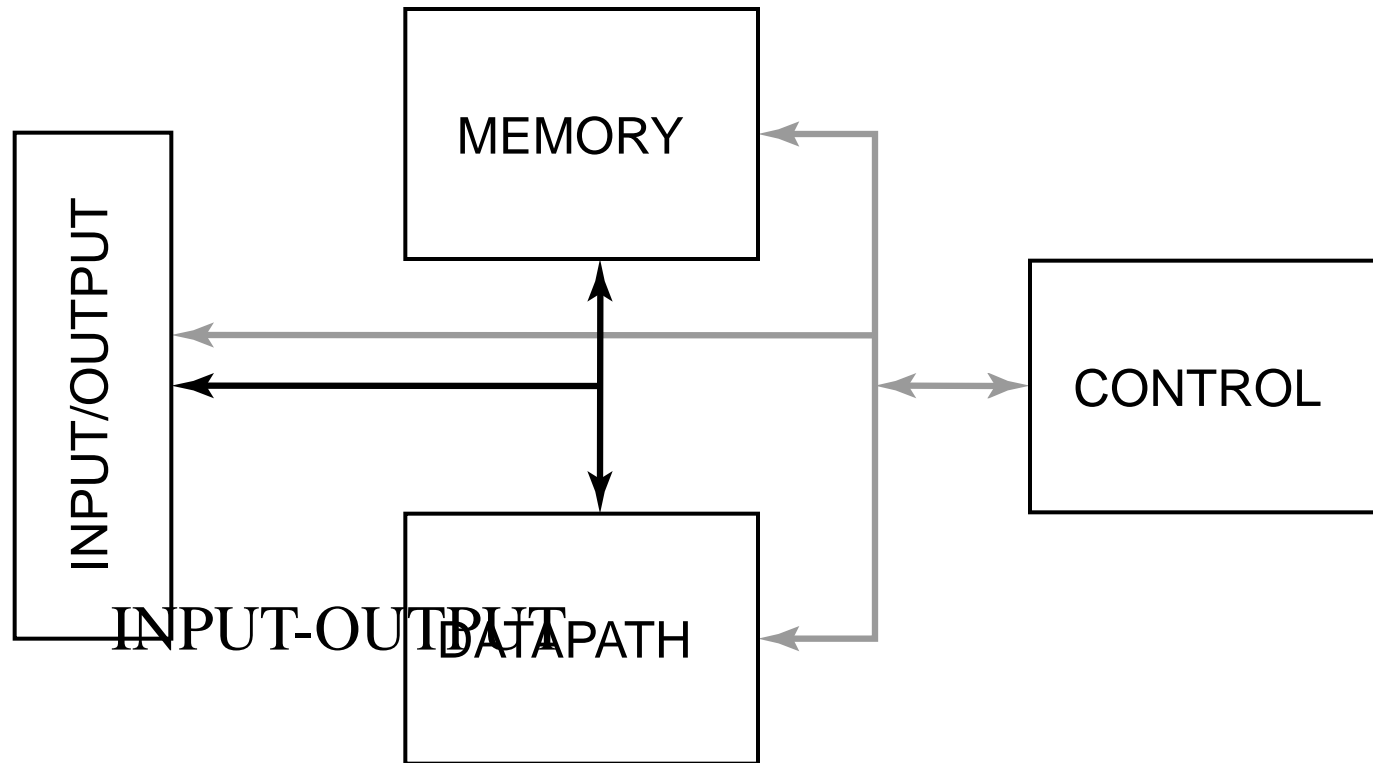
Lecture 18
Implementation Methods

The Design Productivity Challenge
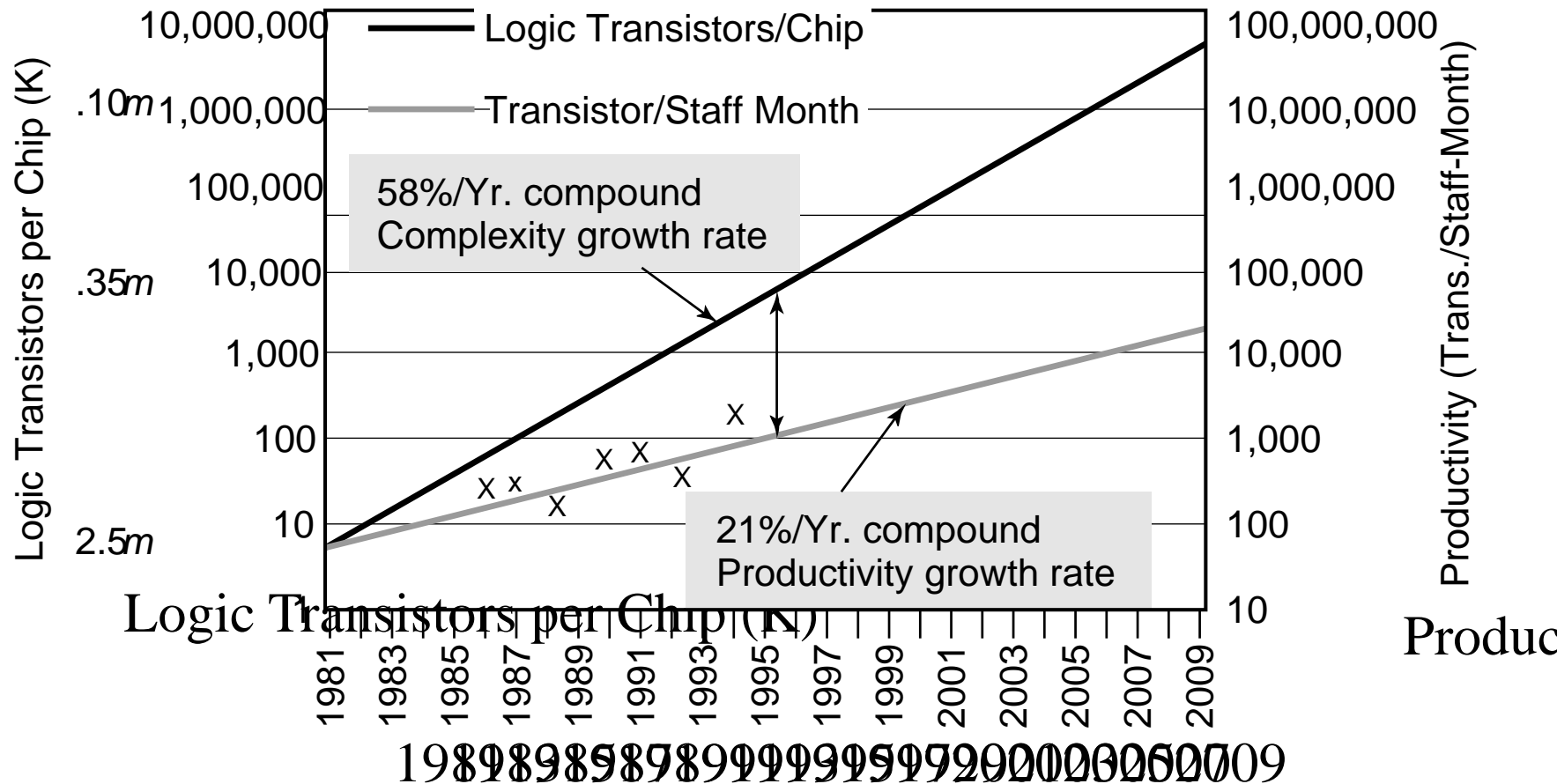
A growing gap between design complexity and design productivity

Source: sematech97

A Simple Processor

MEMORY

INPUT/OUTPUT

CONTROL

INPUT-OUTPUT DATAPATH

Simple Processor (Cont'd)

❖ *Datapath*
- *All computations are performed*
- *Combinational & Arithmetic operations*

❖ *Control Module*
- *Sequential circuit*
- *FSM*

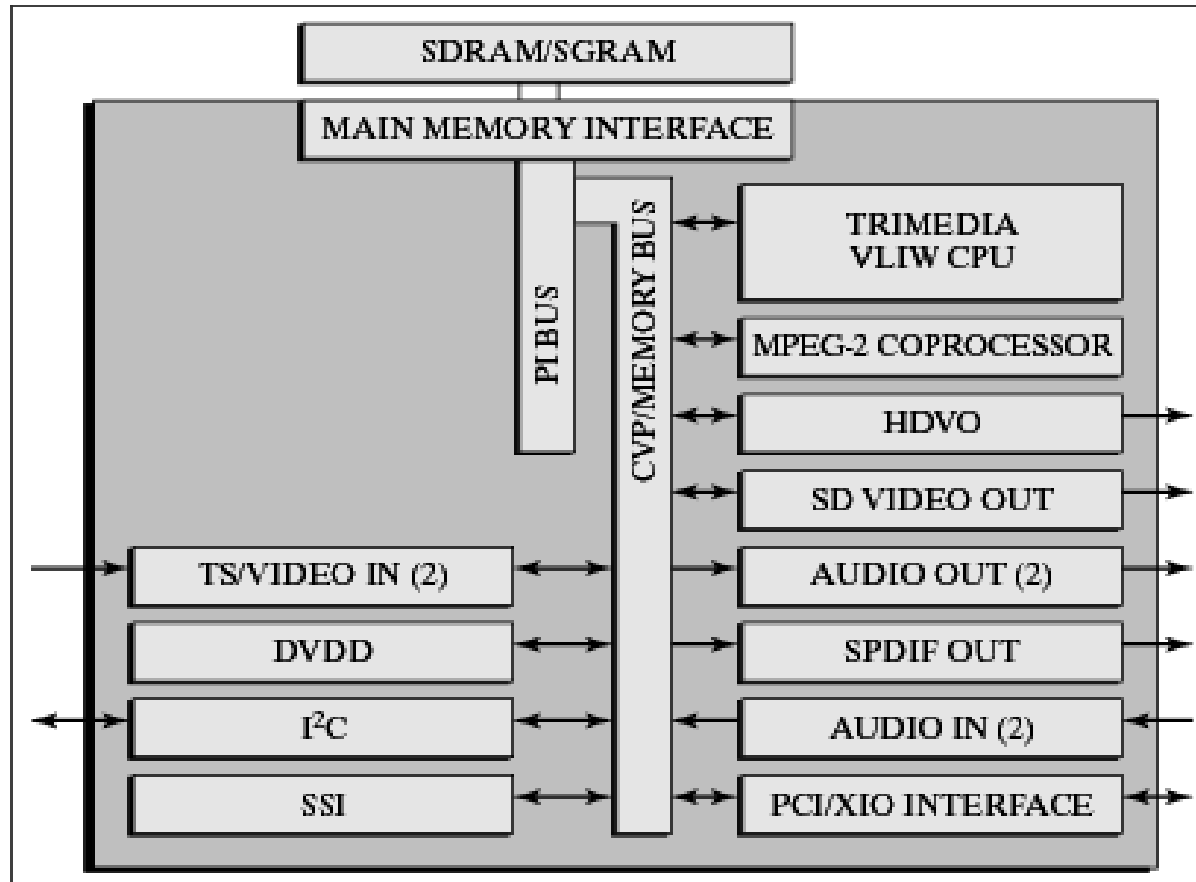❖ *Memory module*
- *Data storage*

❖ *Interconnect*
- *Integrating the whole system*

❖ *I/O circuitry*
- *Connects to outside world*

A System-on-a-Chip: Example

Courtesy: Philips

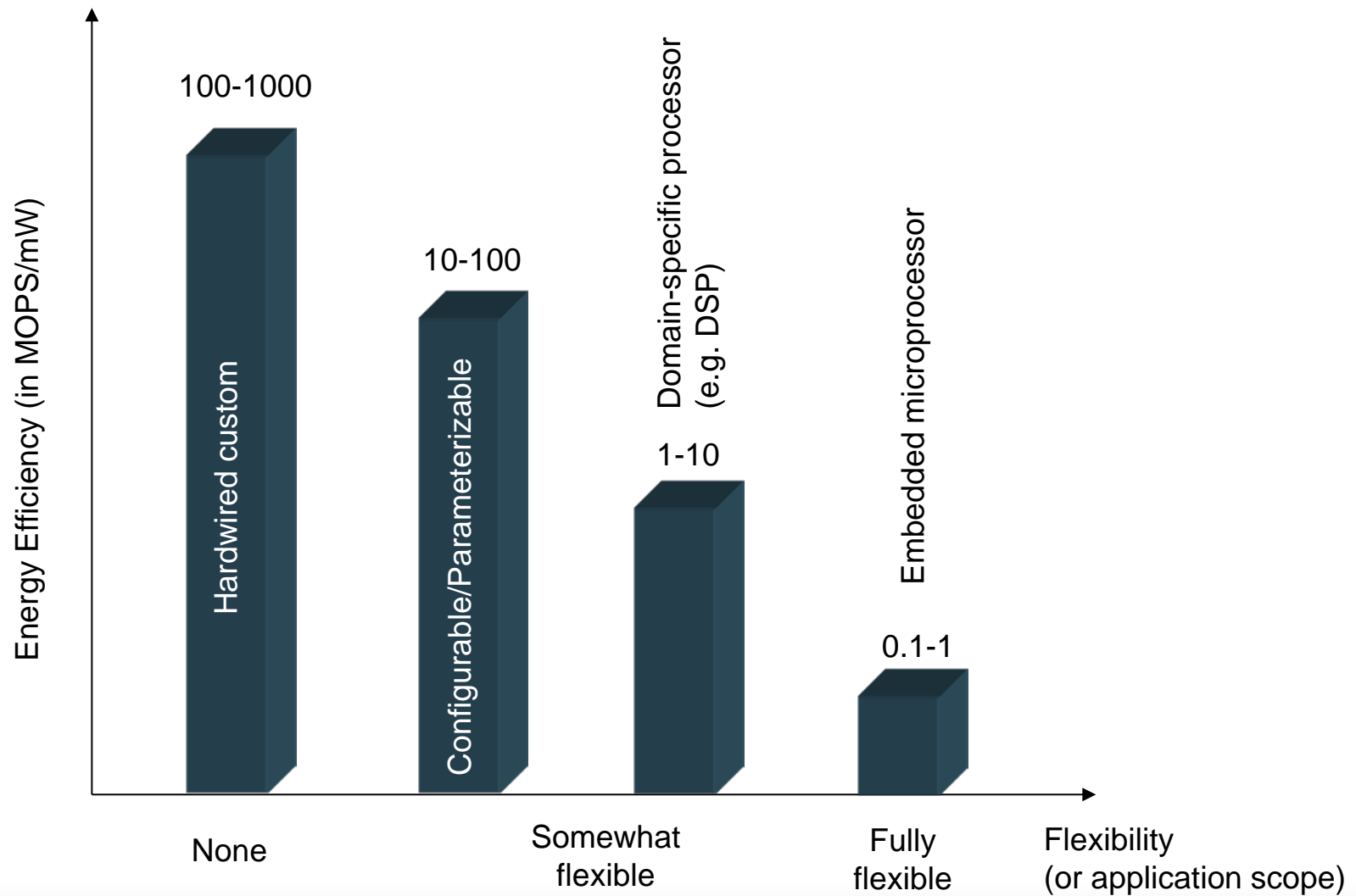# Implementation Approach

❖ *Flexibility (Programmable design)*
  - *Reuse of single design for multiple applications*
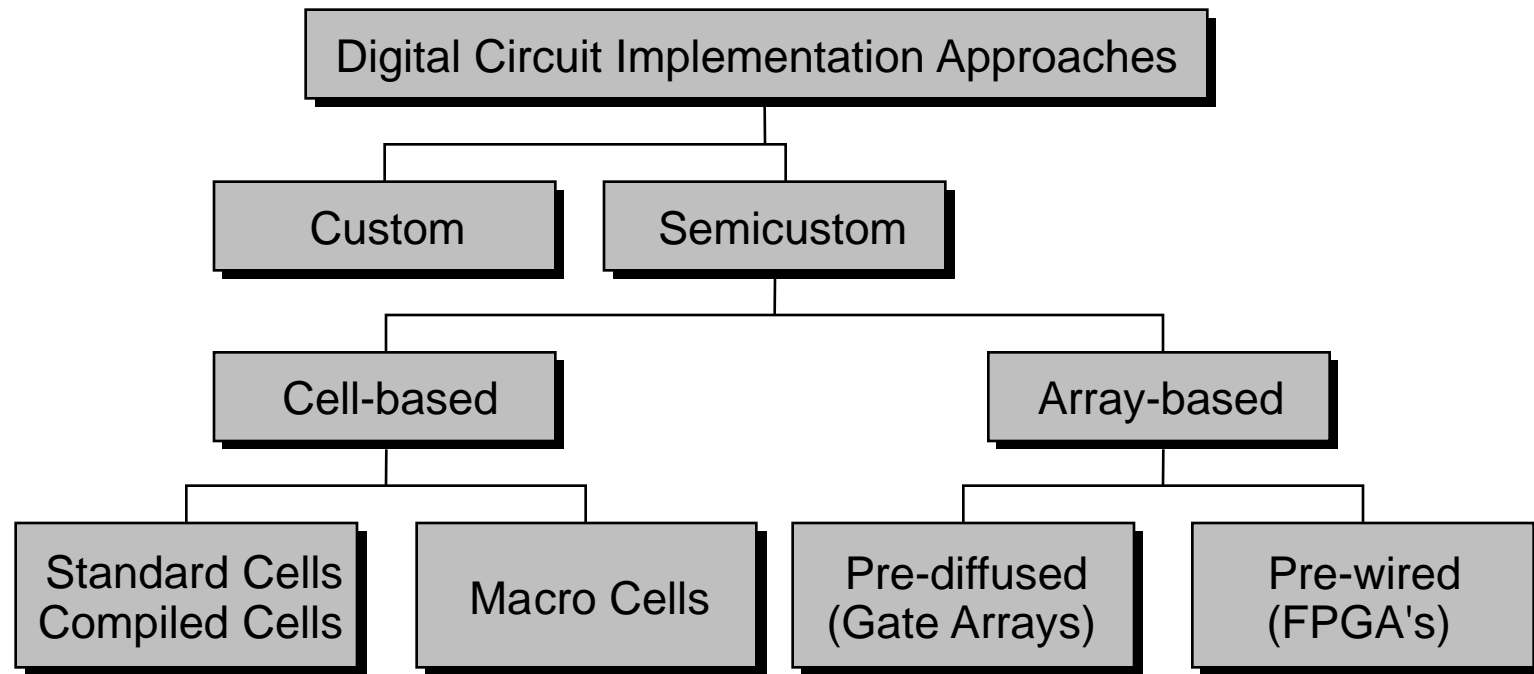 - *Upgrade in the field*

❖ *Hard-wired*
  - *Totally fixed at the manufacturing time*

❖ *Flexibility comes at the cost of higher energy dissipation*

Impact of Implementation Choices

Implementation Choices

Custom Circuit Design

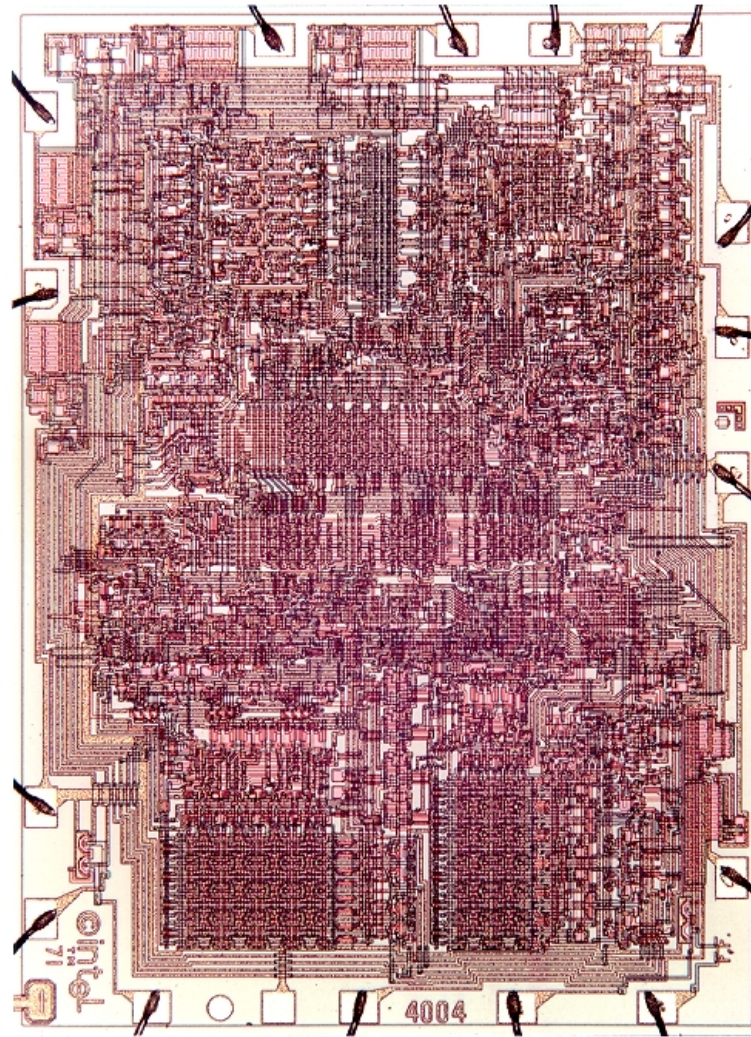❖ *Performance or Design density is of prime importance*
- *Long time to market*

❖ *Can be justified in limited situations*
- *Custom block can be reused many time (e.g. memory blocks)*
- *Cost can be amortized over large volumes*

❖ *Design automation*
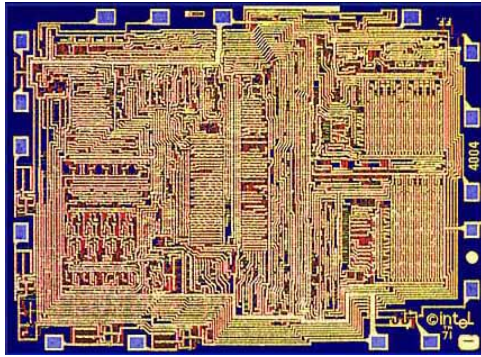- *Very critical components are designed manually*
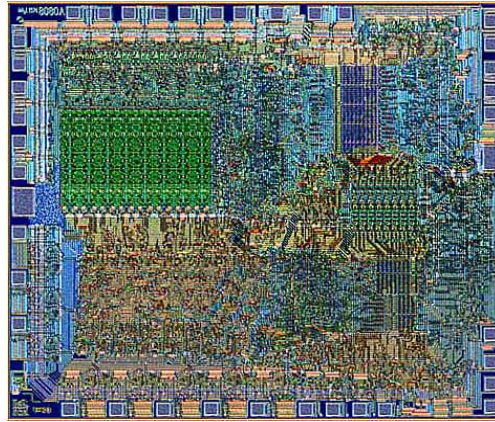
The Custom Approach
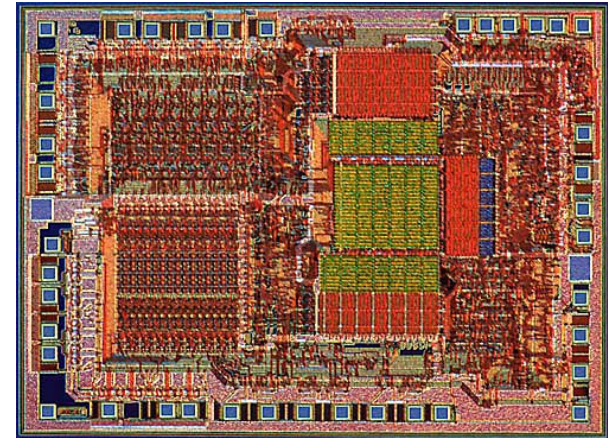

Intel 4004

Courtesy Intel

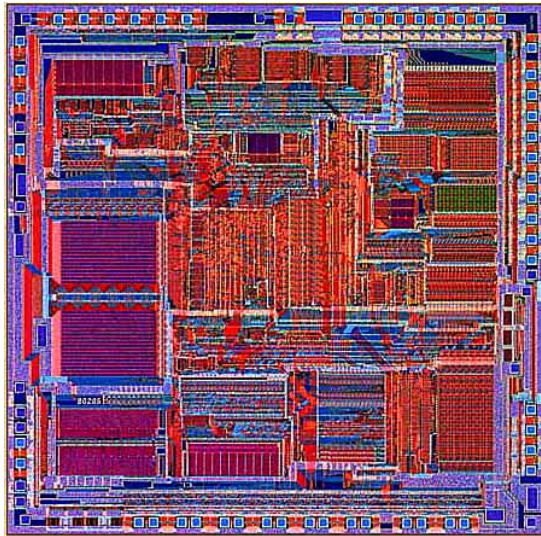# Transition to Automation and Regular Structures
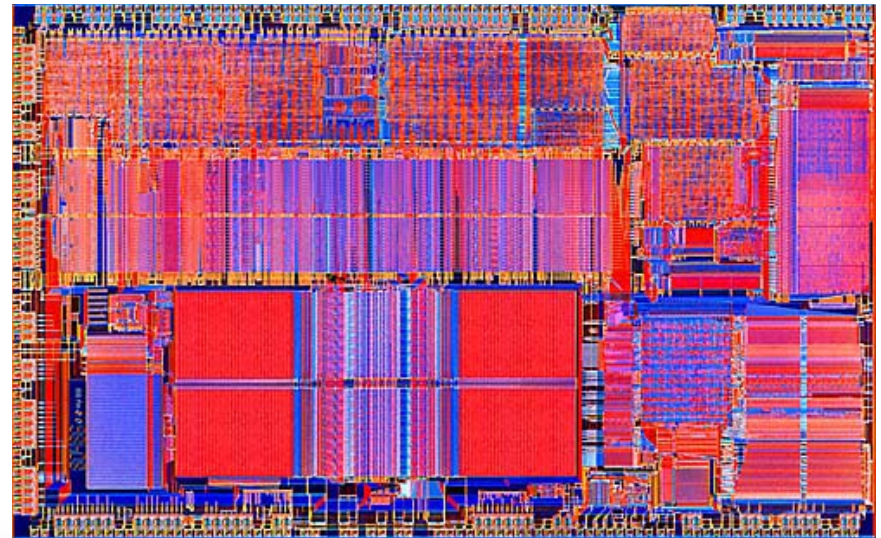

Intel 4004 ('71)
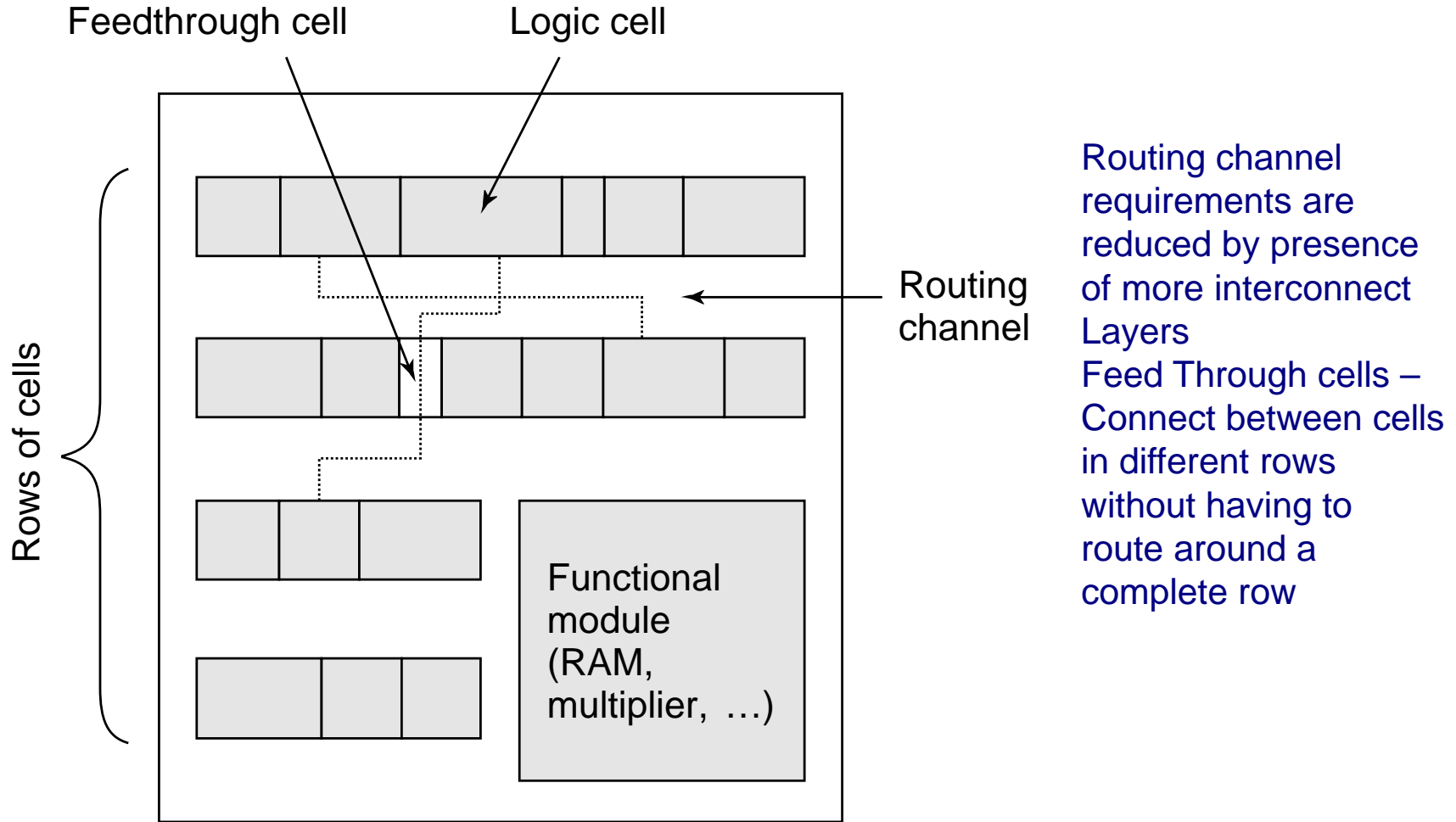
Intel 8080

Intel 8085

Intel 8286

Intel 8486

Courtesy Intel

Cell-based Design

❖ **Standardizes the design entry level at the logic gate**

❖ **Library of logic gates**
- **Inverter, AND/NAND, OR/NOR, Flip-flops**
- **More complex functions, AOI…..**

❖ **Design generation**
- **Schematic using the cells**
- **Higher level description language (VHDL, Verilog)**

❖ **All cells have identical heights**

❖ **Widths of the cells may vary**

❖ **Standard cell design can be combined with other layout methodologies**

Cell-based Design (or standard cells)

Feedthrough cell

Logic cell

Rows of cells

Routing channel

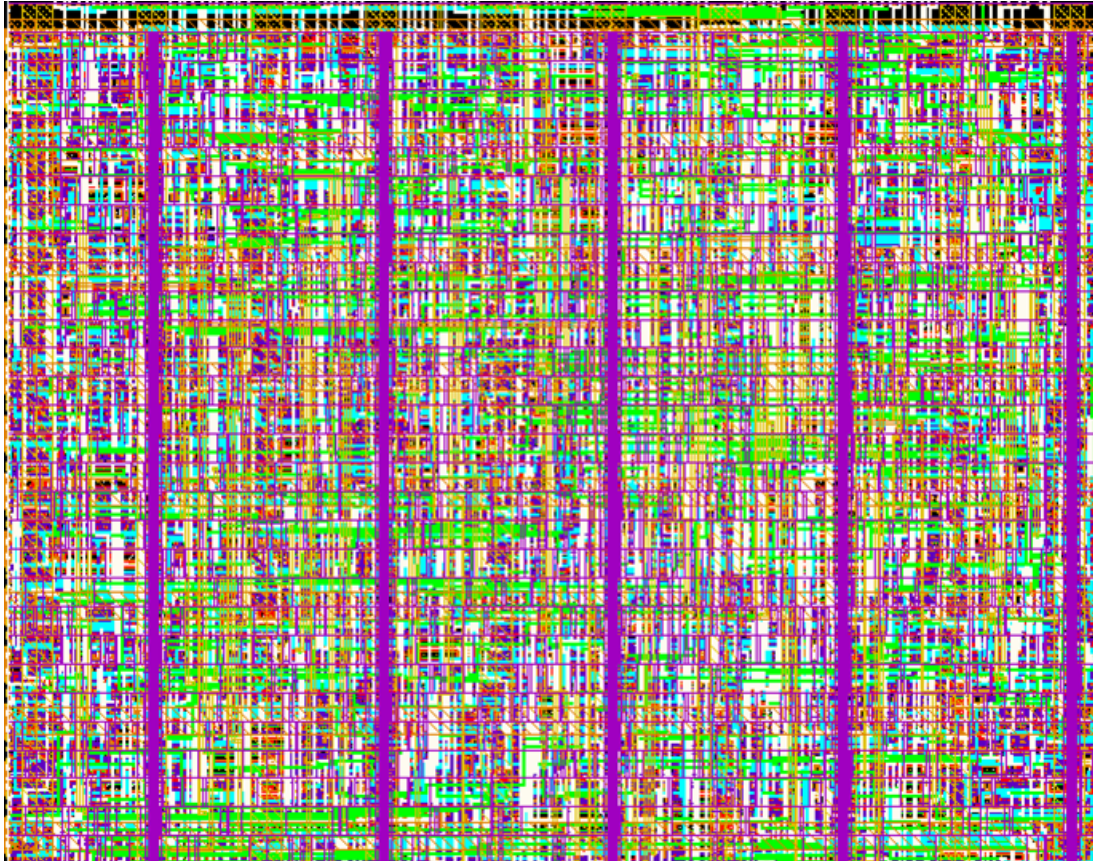Functional module (RAM, multiplier, …)

Routing channel requirements are reduced by presence of more interconnect Layers

Feed Through cells – Connect between cells in different rows without having to route around a complete row
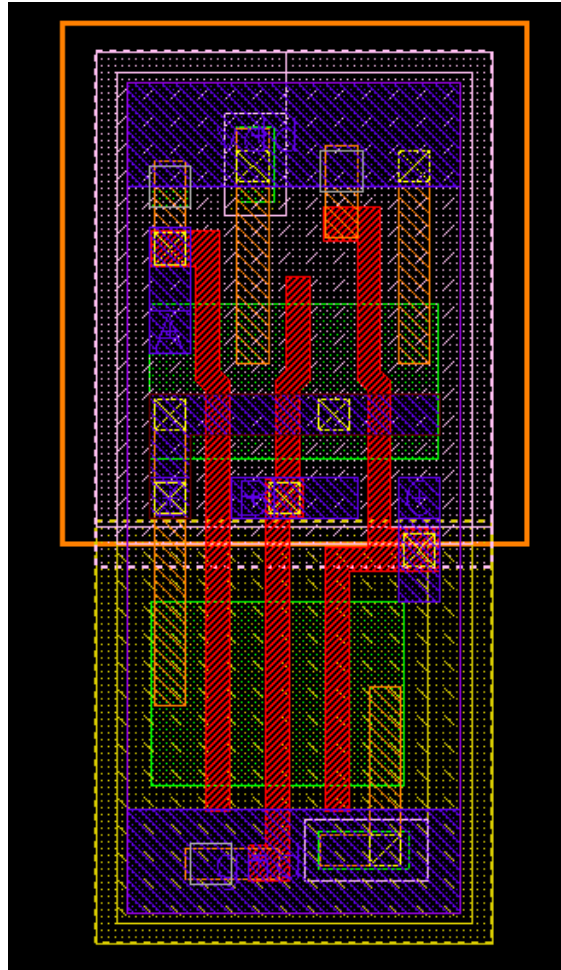
Standard Cell — Example
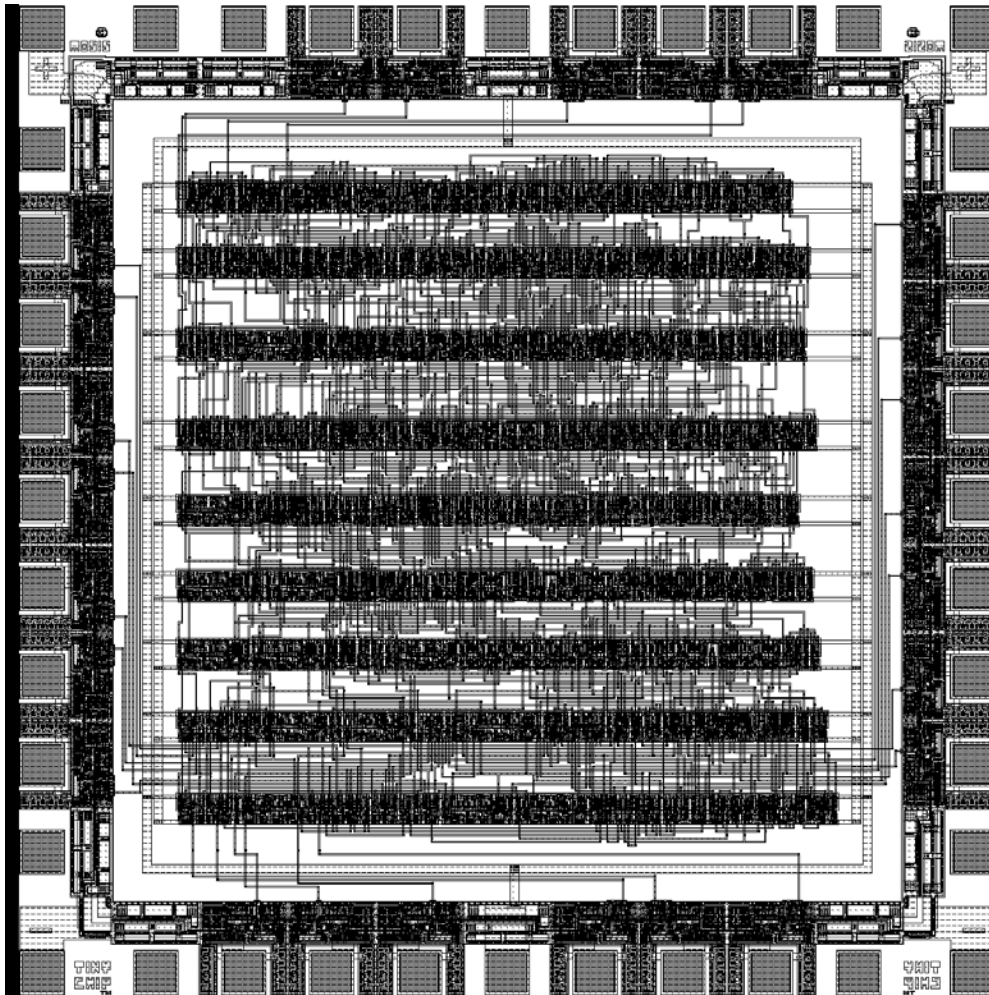
[Brodersen92]

Standard Cell – The New Generation

Cell-structure hidden under interconnect layers

Standard Cell - Example

Path	1.2V - 125°C	1.6V - 40°C
$In1 - t_{pLH}$	$0.073 + 7.98C + 0.317T$	$0.020 + 2.73C + 0.253T$
$In1 - t_{pHL}$	$0.069 + 8.43C + 0.364T$	$0.018 + 2.14C + 0.292T$
$In2 - t_{pLH}$	$0.101 + 7.97C + 0.318T$	$0.026 + 2.38C + 0.255T$
$In2 - t_{pHL}$	$0.097 + 8.42C + 0.325T$	$0.023 + 2.14C + 0.269T$
$In3 - t_{pLH}$	$0.120 + 8.00C + 0.318T$	$0.031 + 2.37C + 0.258T$
$In3 - t_{pHL}$	$0.110 + 8.41C + 0.280T$	$0.027 + 2.15C + 0.223T$

3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

Macrocells

❖ **Complex blocks than random logic functions**
❖ **(Multipliers, DSPs …)**
❖ **Complex cells – Macro cells**

Hard Macro

Macro cells
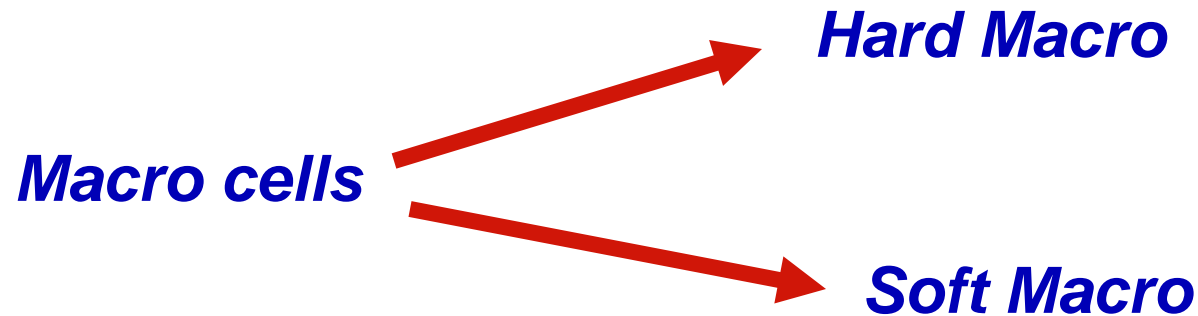
Soft Macro

Hard & Soft Macro

❖ **Hard Macro -** *Design of a logic function on a chip that specifies how the required logic elements are interconnected and specifies the physical pathways and wiring patterns between the components.*

❖ **Soft Macro -** *Design of a logic function on a chip that specifies how the required logic elements are interconnected, but not the physical wiring pattern.*
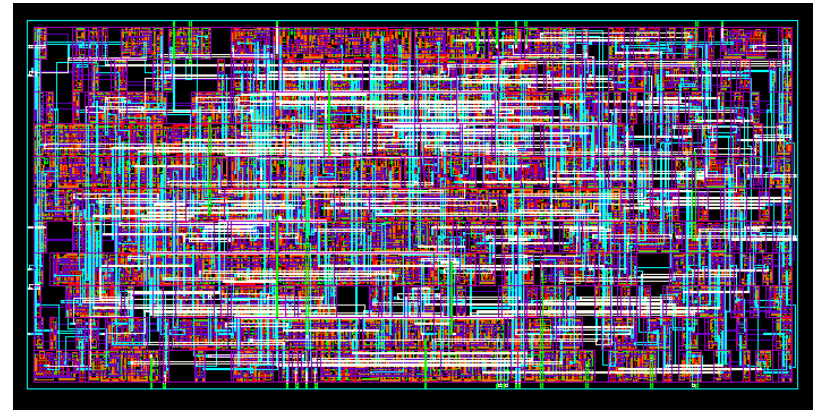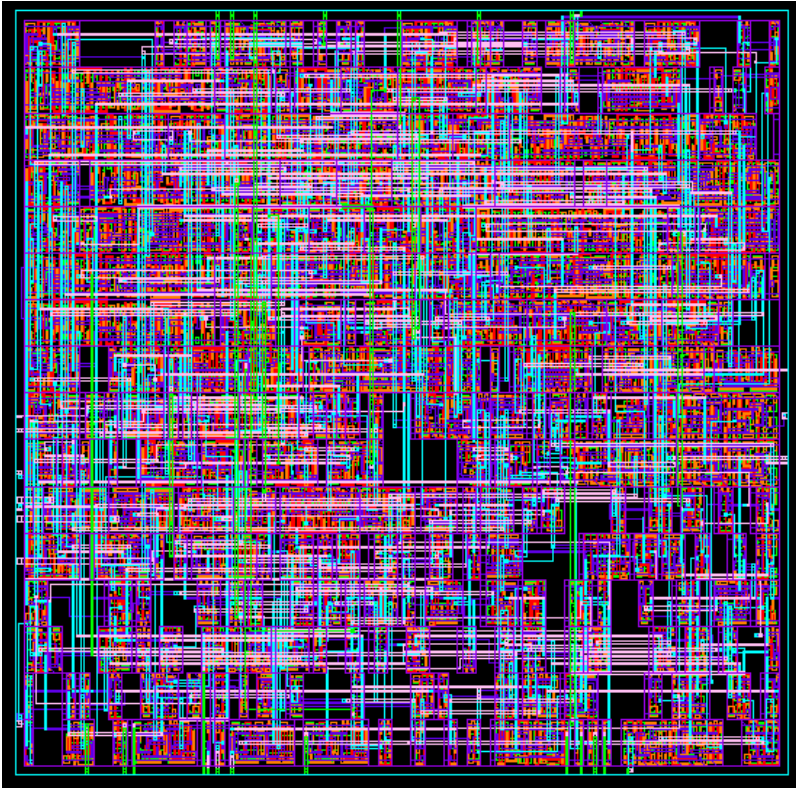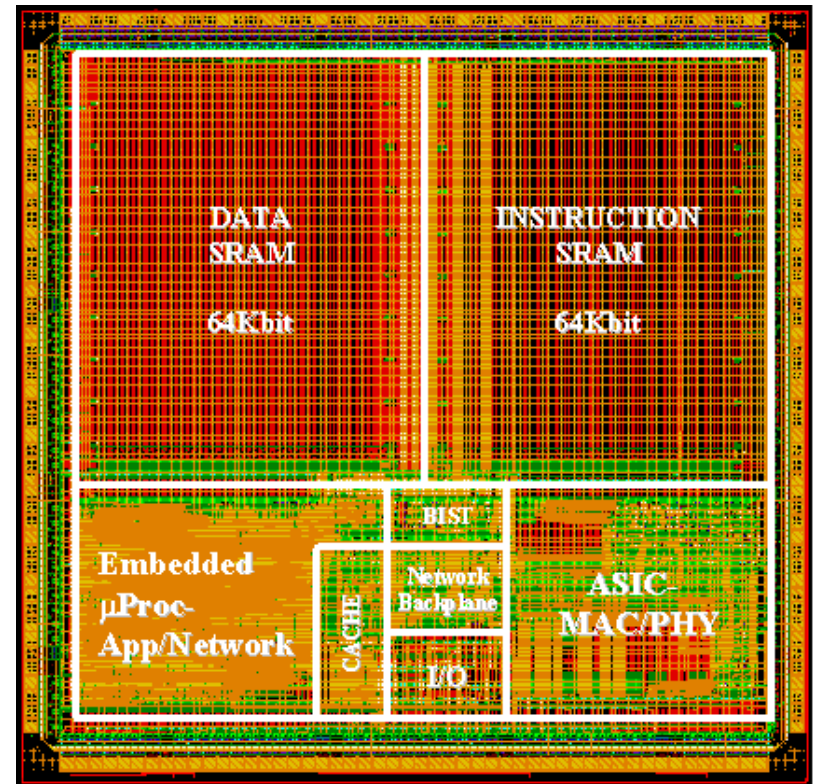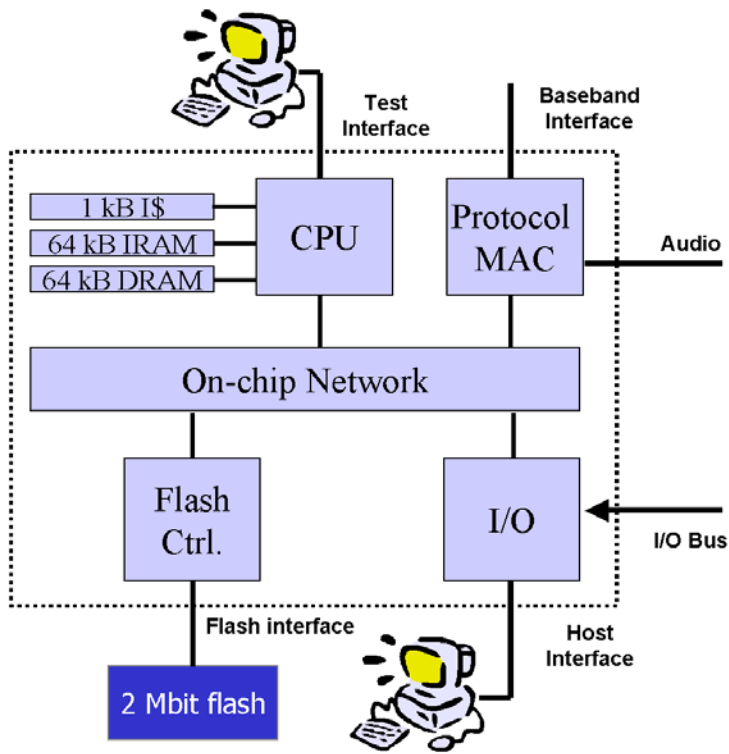
Hard MacroModules
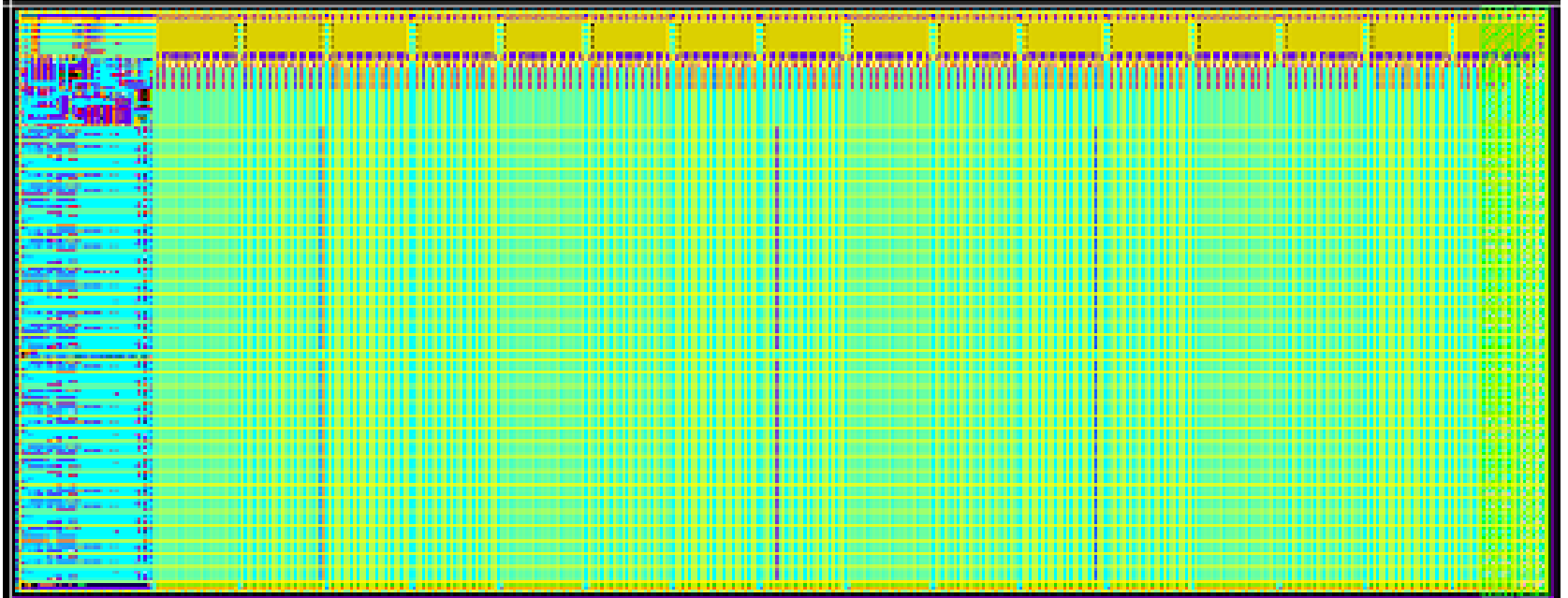
256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator

"Soft" MacroModules
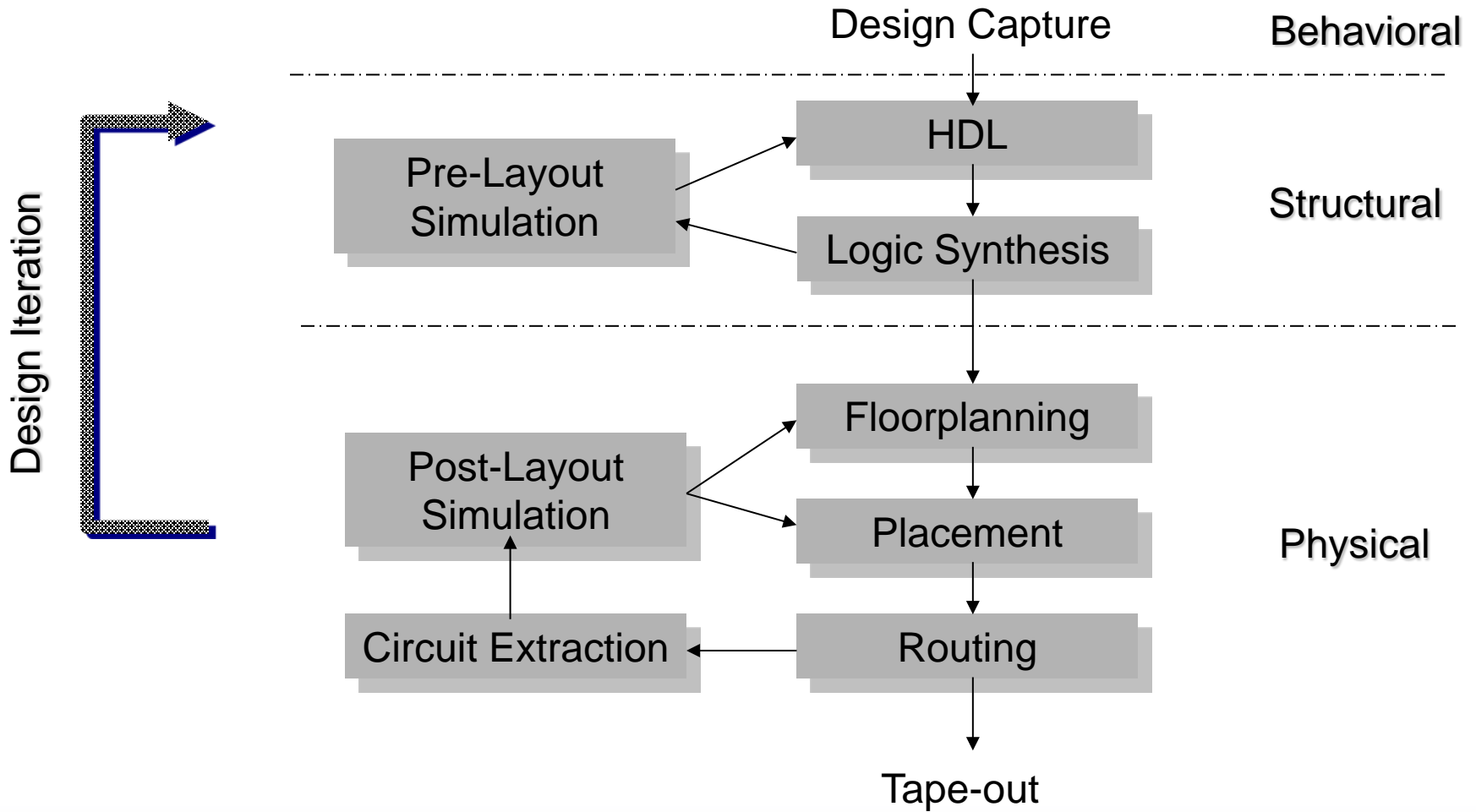

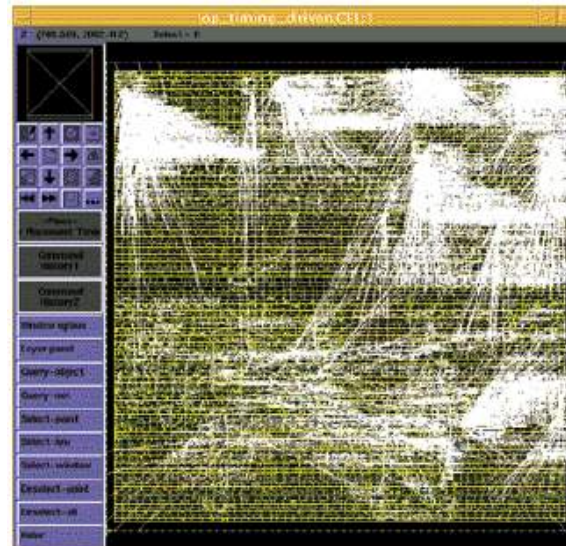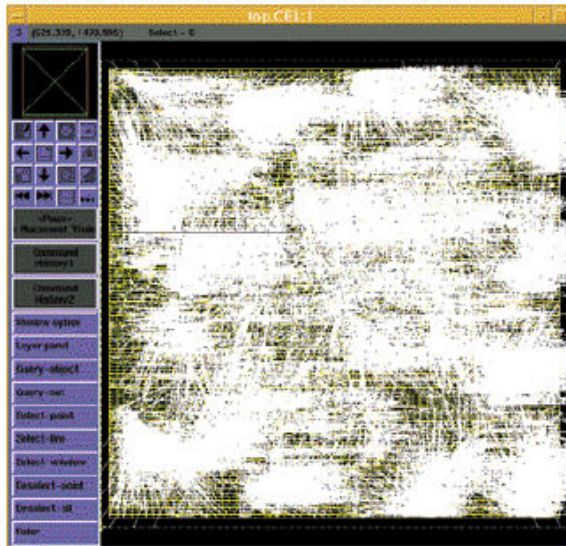*Synopsys DesignCompiler*

"Intellectual Property"

A Protocol Processor for Wireless

Semicustom Design Flow

The "Design Closure" Problem

Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys

Integrating Synthesis with Physical Design

RTL   (Timing) Constraints

Physical Synthesis

Macromodules
Fixed netlists

Netlist with
Place-and-Route Info

Place-and-Route
Optimization

Artwork