EE 466/586 VLSI Design

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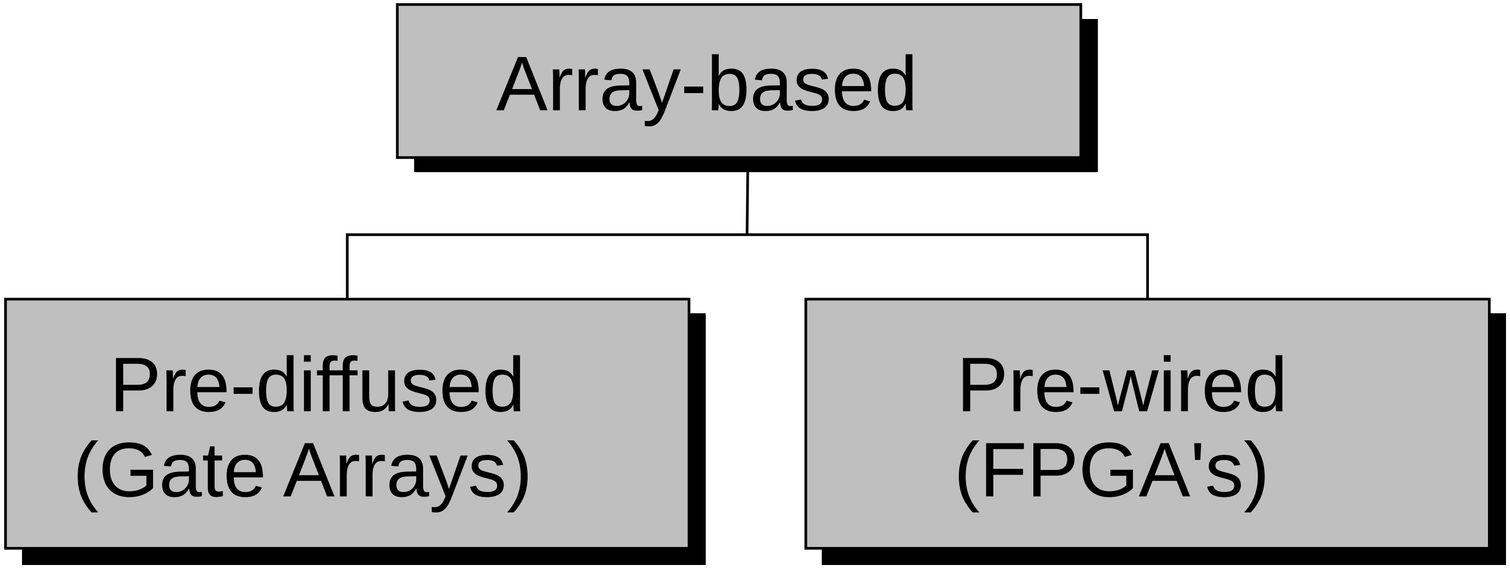
Lecture 19

Implementation Methods (Cont’d)

Late-Binding Implementation

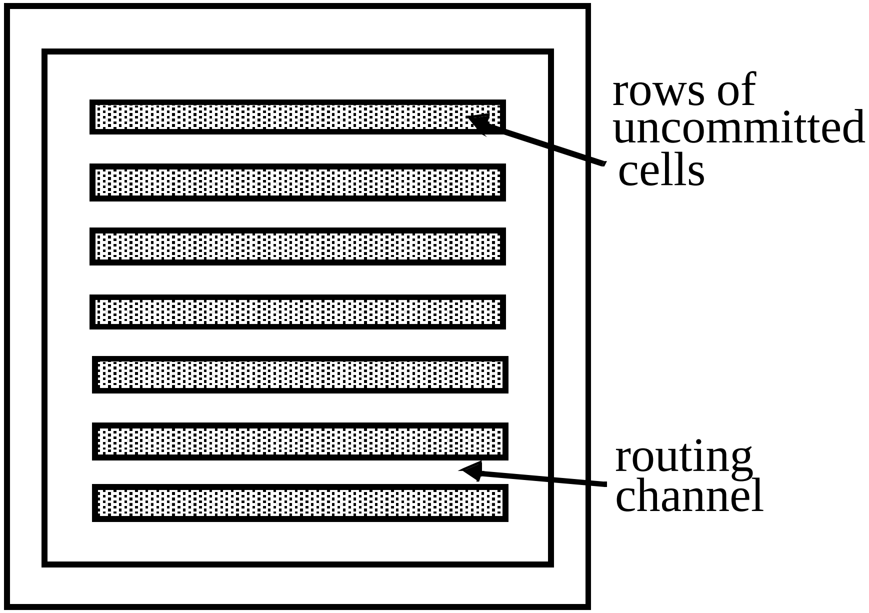


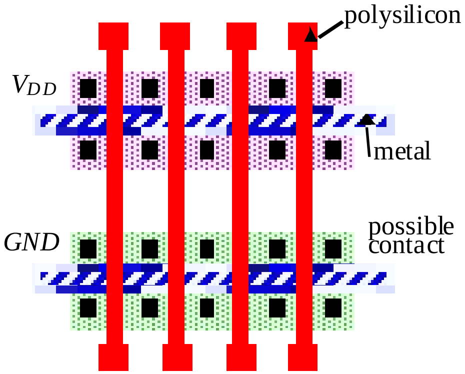
Array-based

Pre-diffused
(Gate Arrays)

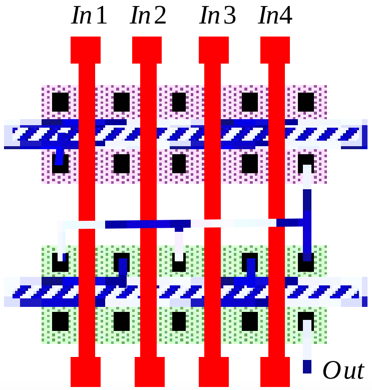
Pre-wired
(FPGA's)

Gate Array — Sea-of-gates



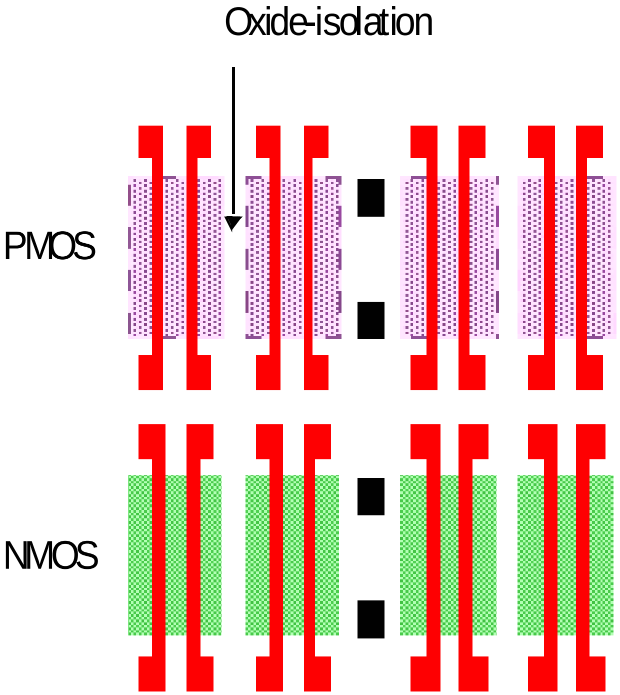


Uncommitted Cell

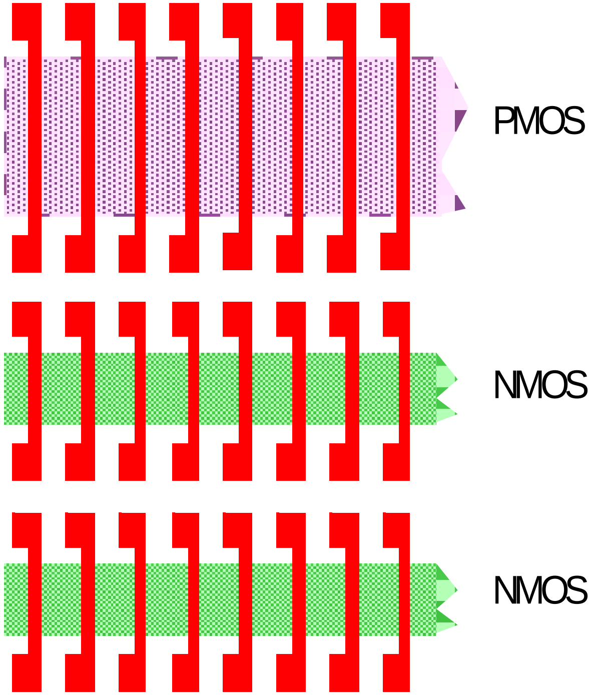


Committed Cell
(4-input NOR)

Sea-of-gate Primitive Cells

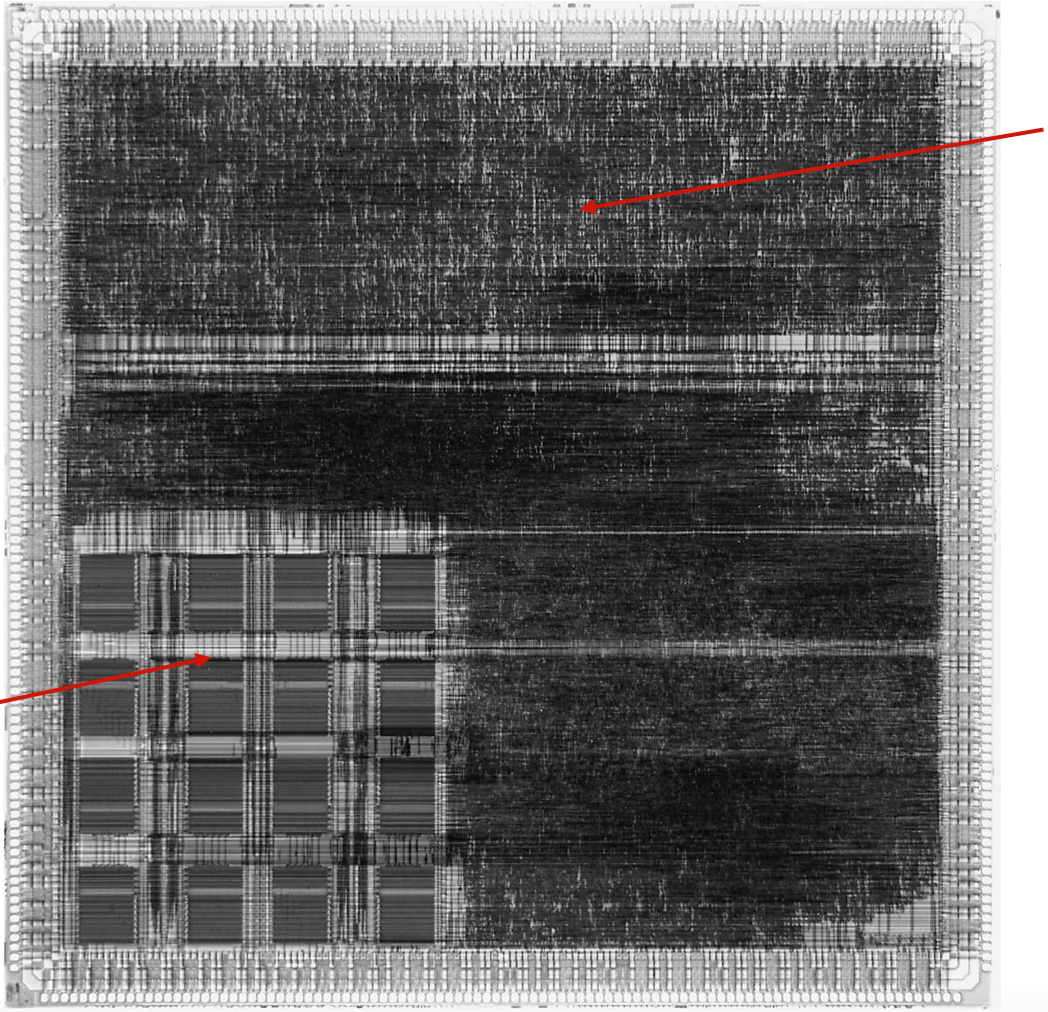


Using oxide-isolation



Using gate-isolation

Sea-of-gates



Random Logic

Memory Subsystem

LSI Logic LEA300K
(0.6 μm CMOS)

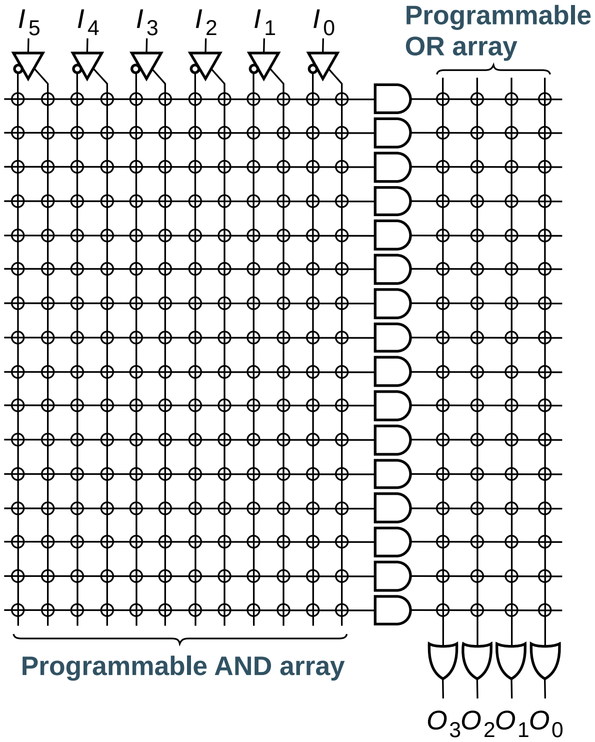
Courtesy LSI Logic

Prewired Arrays

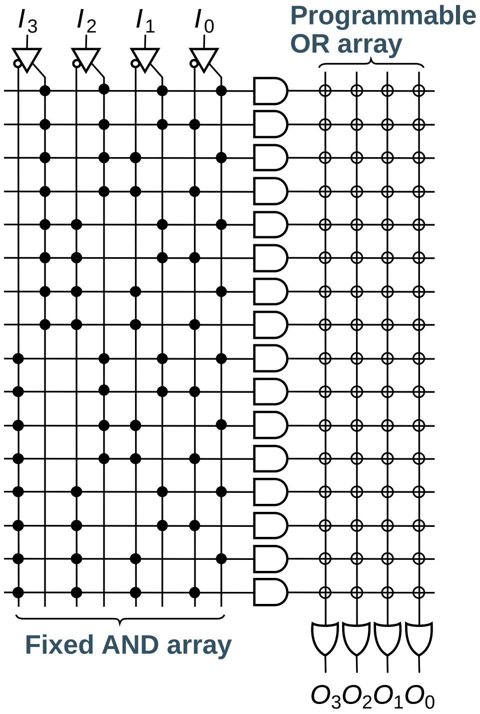
Classification of prewired arrays (or field-programmable devices):

- ❑ Based on Programming Technique
  - ▪ Fuse-based (program-once)
  - ▪ Non-volatile EPROM based
  - ▪ RAM based
- ❑ Programmable Logic Style
  - ▪ Array-Based
  - ▪ Look-up Table
- ❑ Programmable Interconnect Style
  - ▪ Channel-routing
  - ▪ Mesh networks

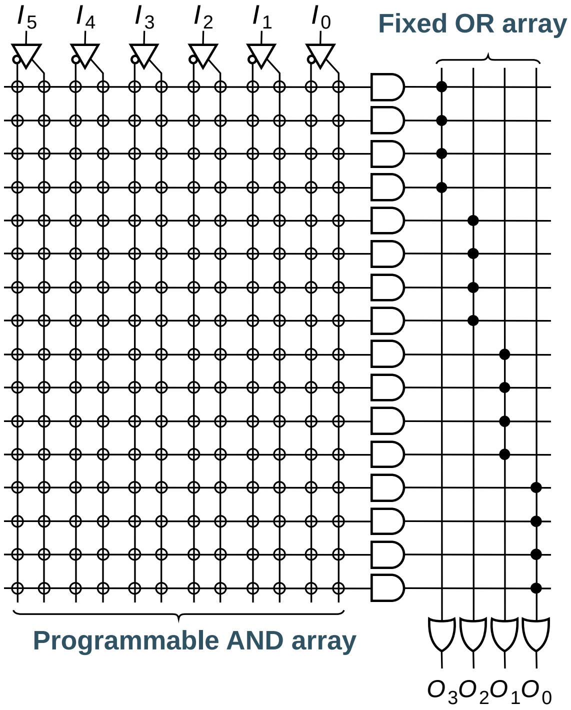
Array-Based Programmable Logic



PLA



PROM

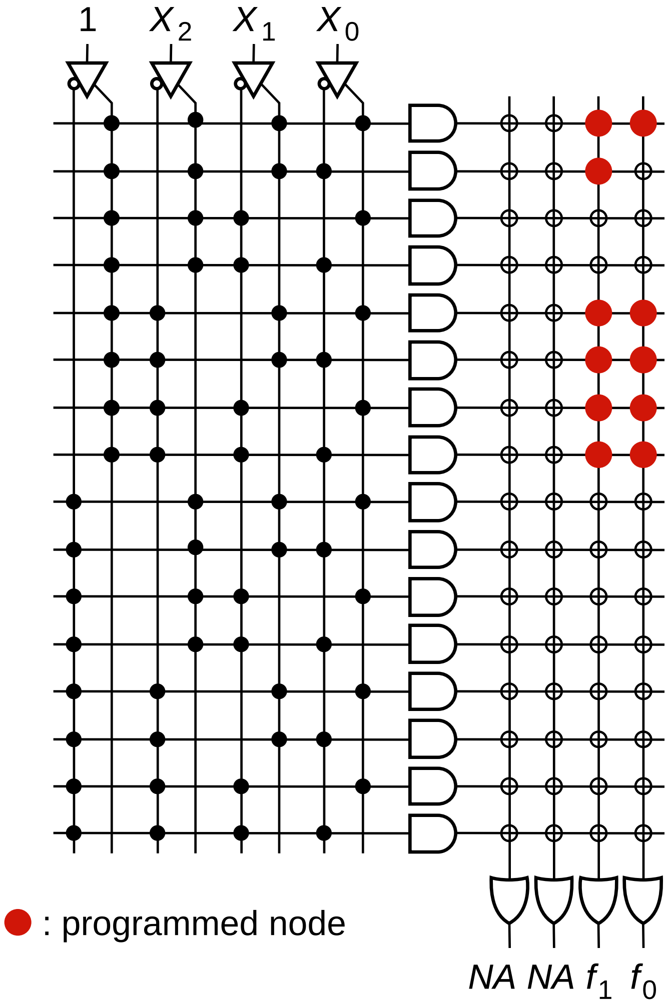


PAL

⊕ Indicates programmable connection

● Indicates fixed connection

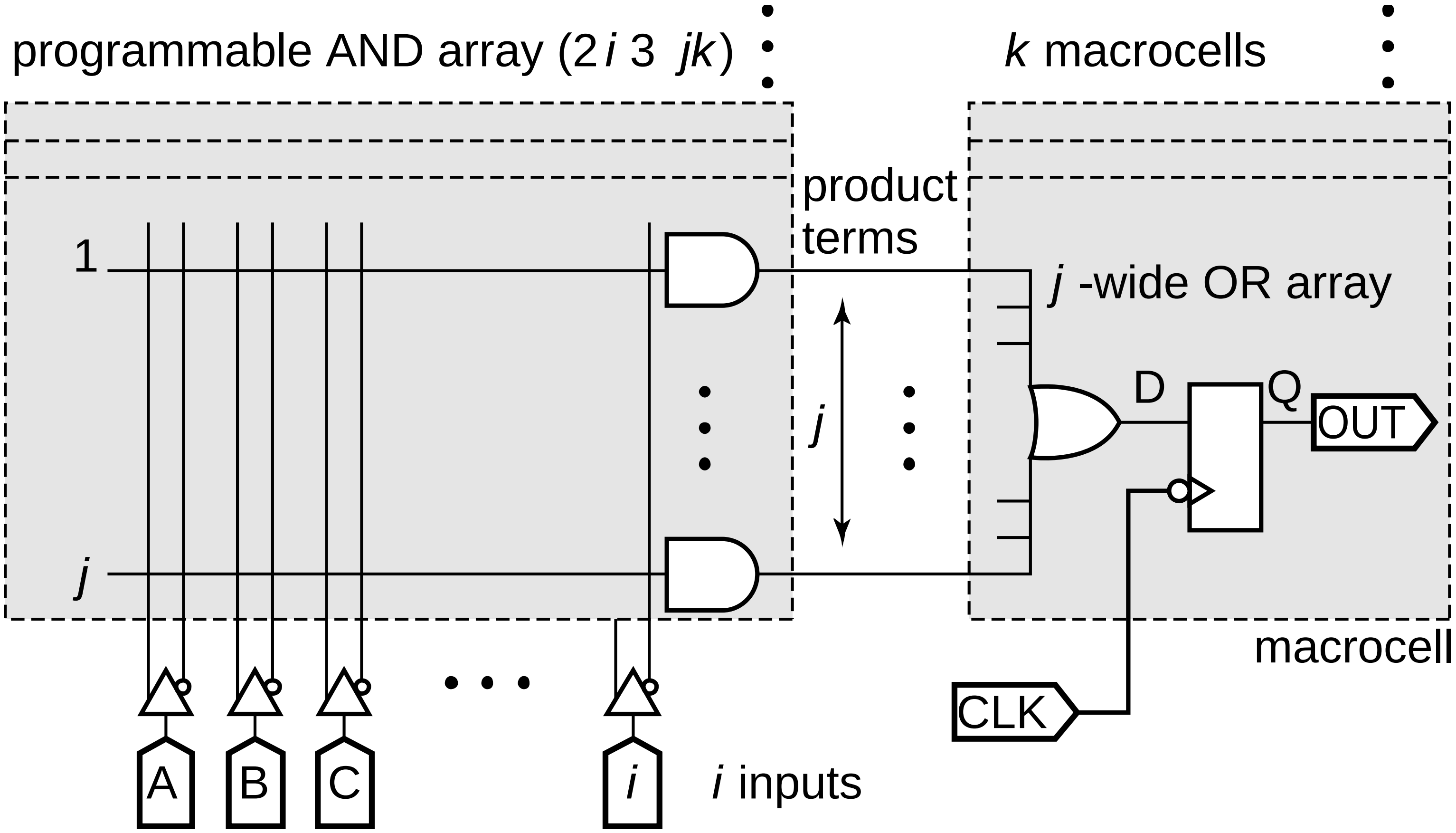
Programming a PROM



$$f_0 = x_0 x_1 + \overline{x_2}$$

$$f_1 = x_0 x_1 x_2 + \overline{x_2} + \overline{x_0} x_1$$

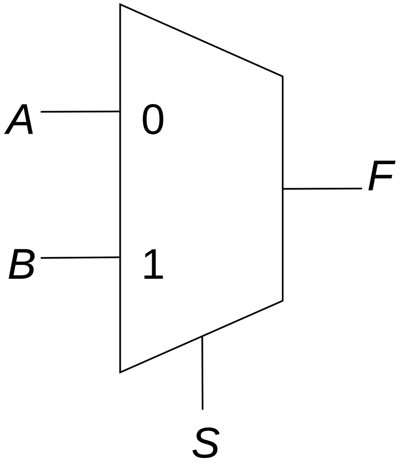
More Complex PAL



i inputs, j minterms/macrocell, k macrocells

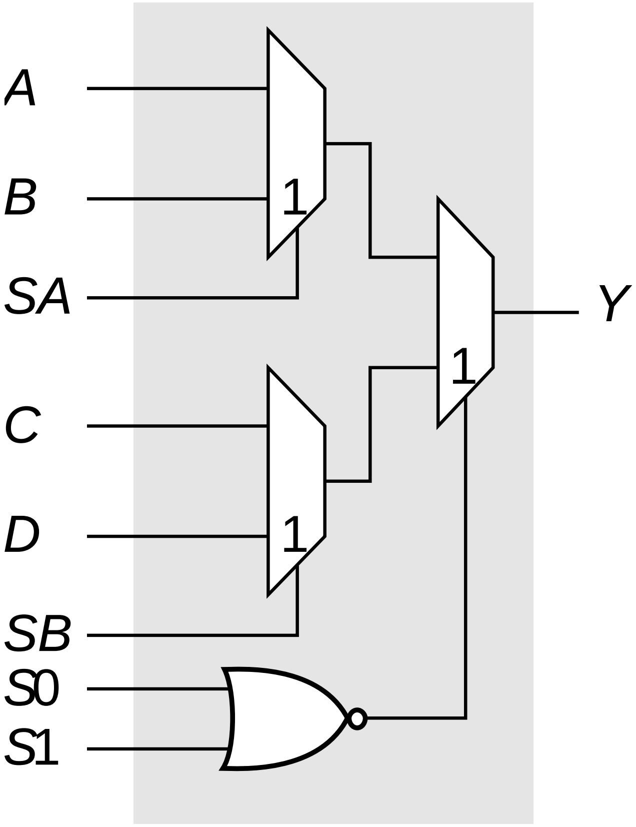
From Smith97

2-input mux as programmable logic block

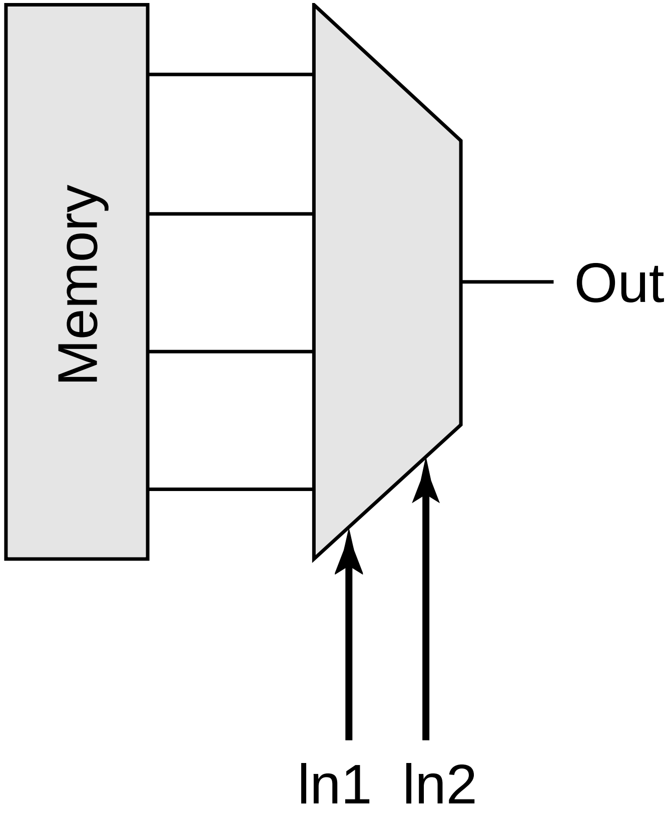


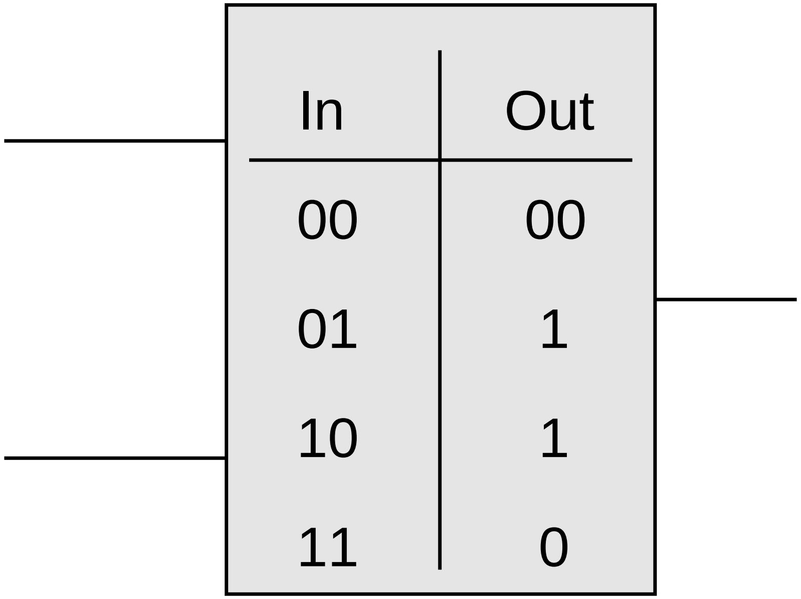
Configuration			
A	***B***	***S***	***F=***
0	0	0	0
0	*X*	1	*X*
0	*Y*	1	*Y*
0	*Y*	*X*	XY
X	0	*Y*	$X\overline{Y}$
Y	0	*X*	$\overline{X}Y$
Y	1	*X*	*X* 1 *Y*
1	0	*X*	$\overline{X}$
1	0	*Y*	$\overline{Y}$
1	1	1	1

Logic Cell of Actel Fuse-Based FPGA



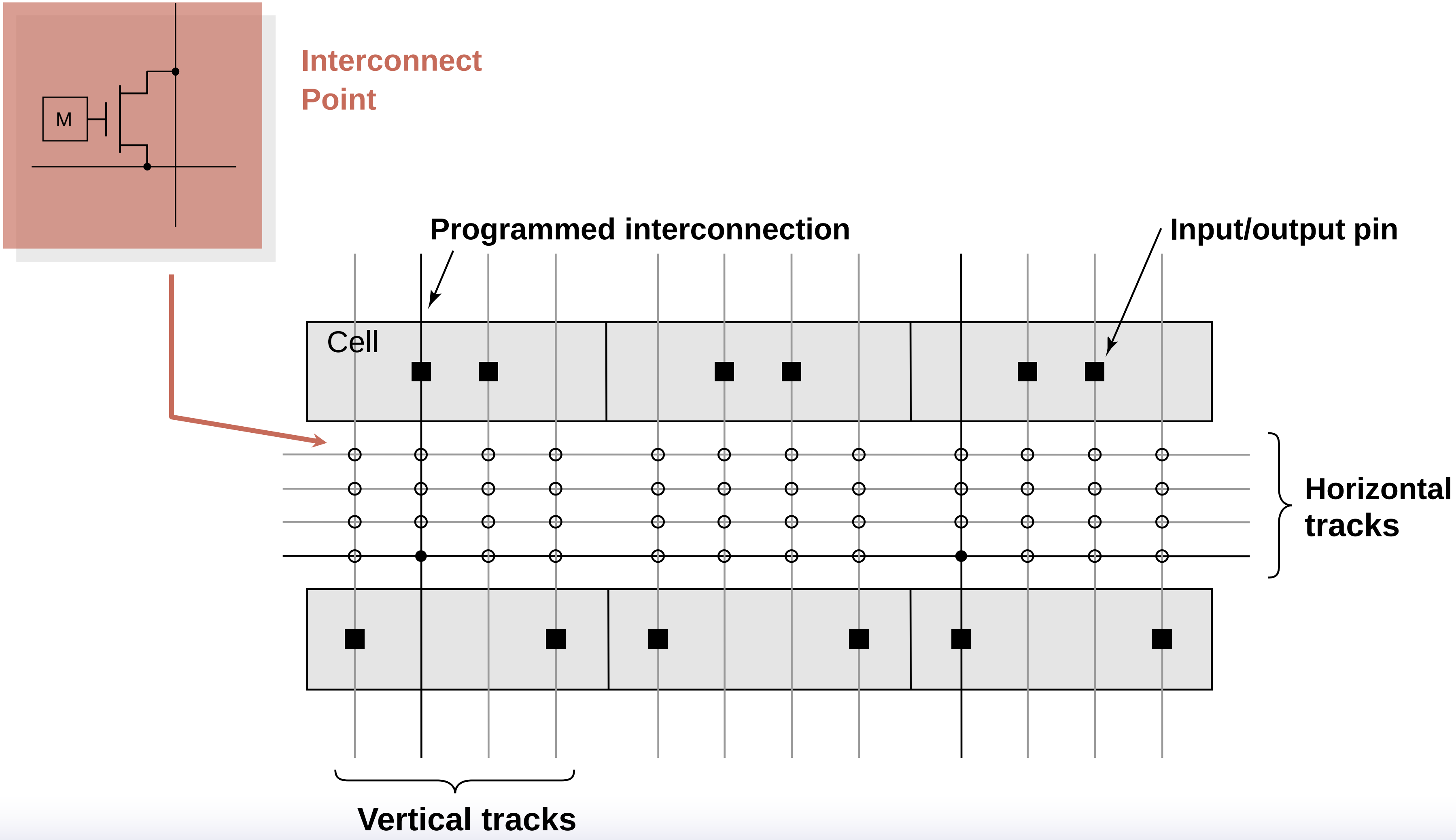
Look-up Table Based Logic Cell





In	Out
00	00
01	1
10	1
11	0

Array-Based Programmable Wiring



Programmable vs. fixed interconnect

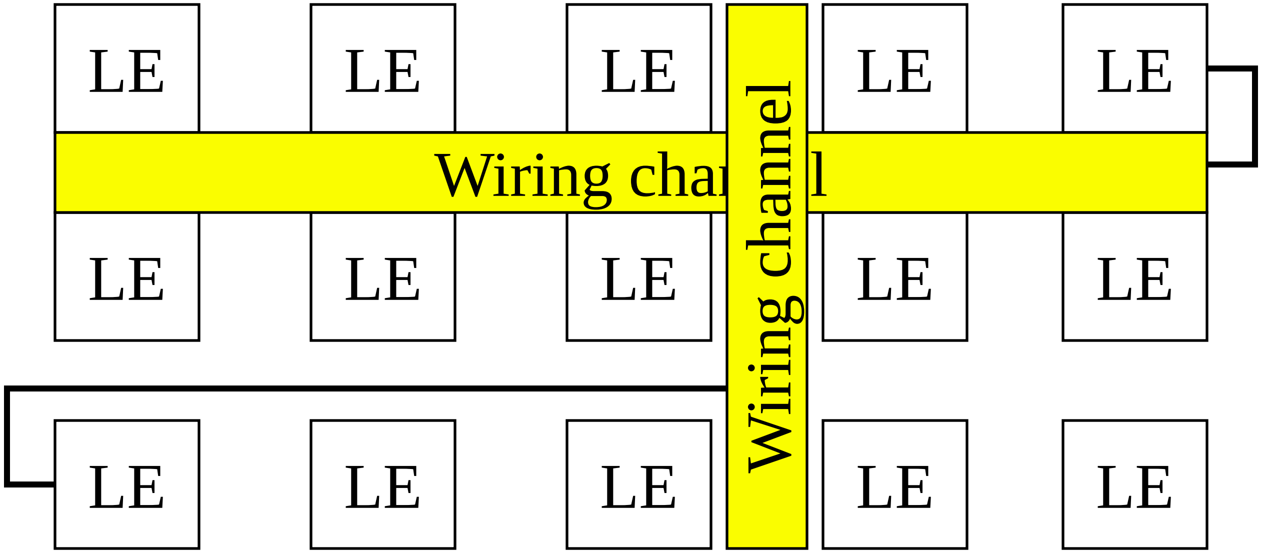
- Switch adds delay.
- Transistor off-state is worse in advanced technologies.
- FPGA interconnect has extra length = added capacitance.

Interconnect strategies

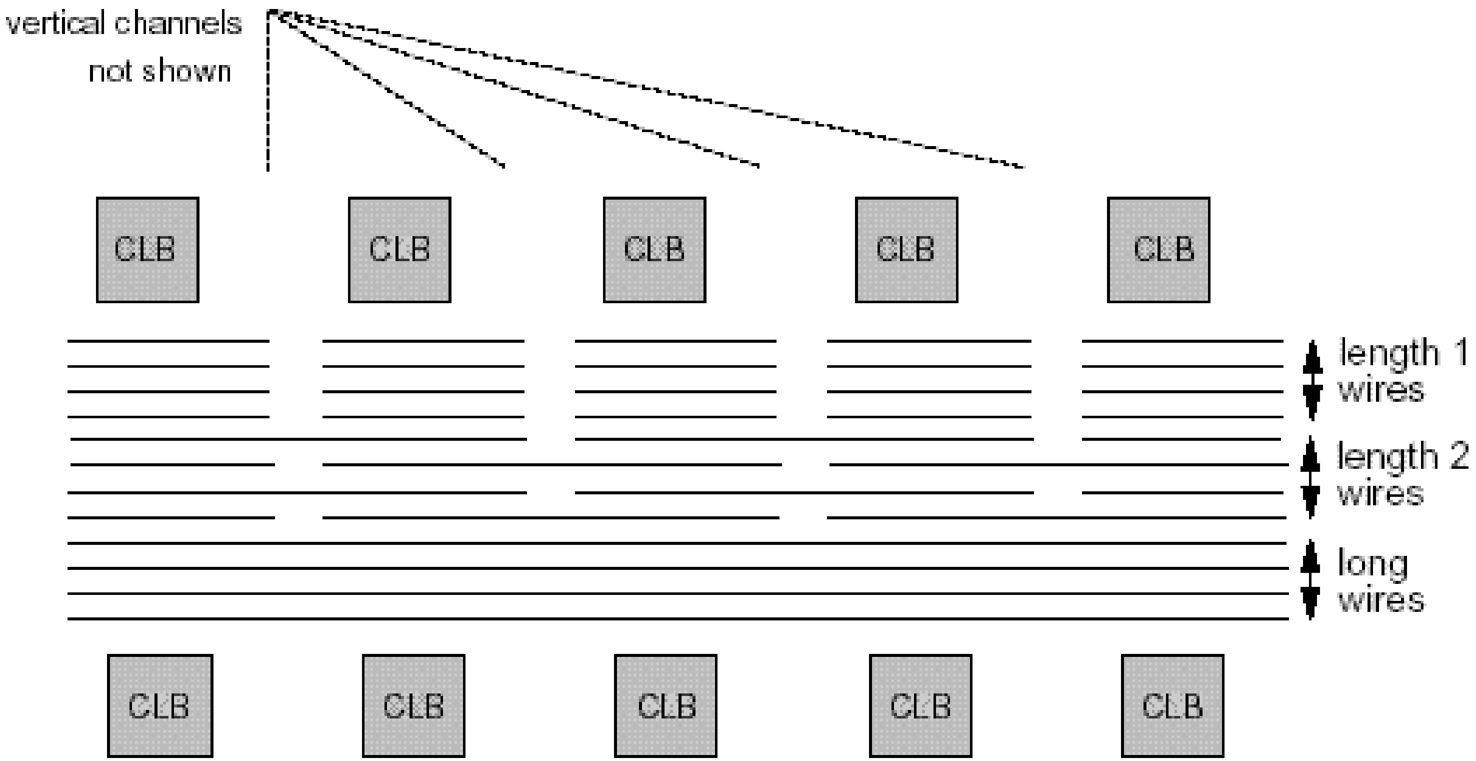
- Some wires will not be utilized.
- Congestion will not be same throughout the chip.
- Types of wires:
  - Short wires: local LE connections.
  - Global wires: long-distance, buffered communication.
  - Special wires: clocks, etc.

Paths in interconnect

- Connection may be long, complex:

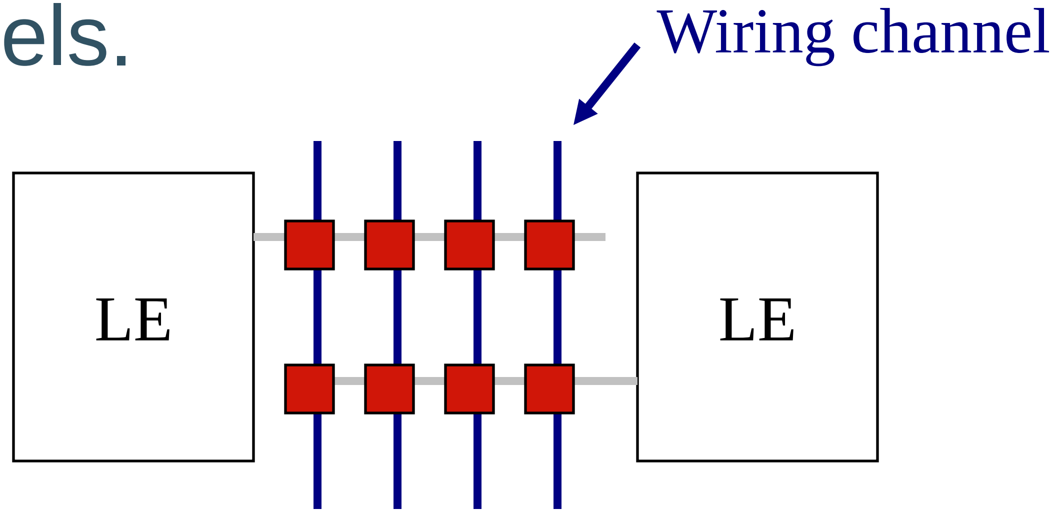


XC4000 Interconnect

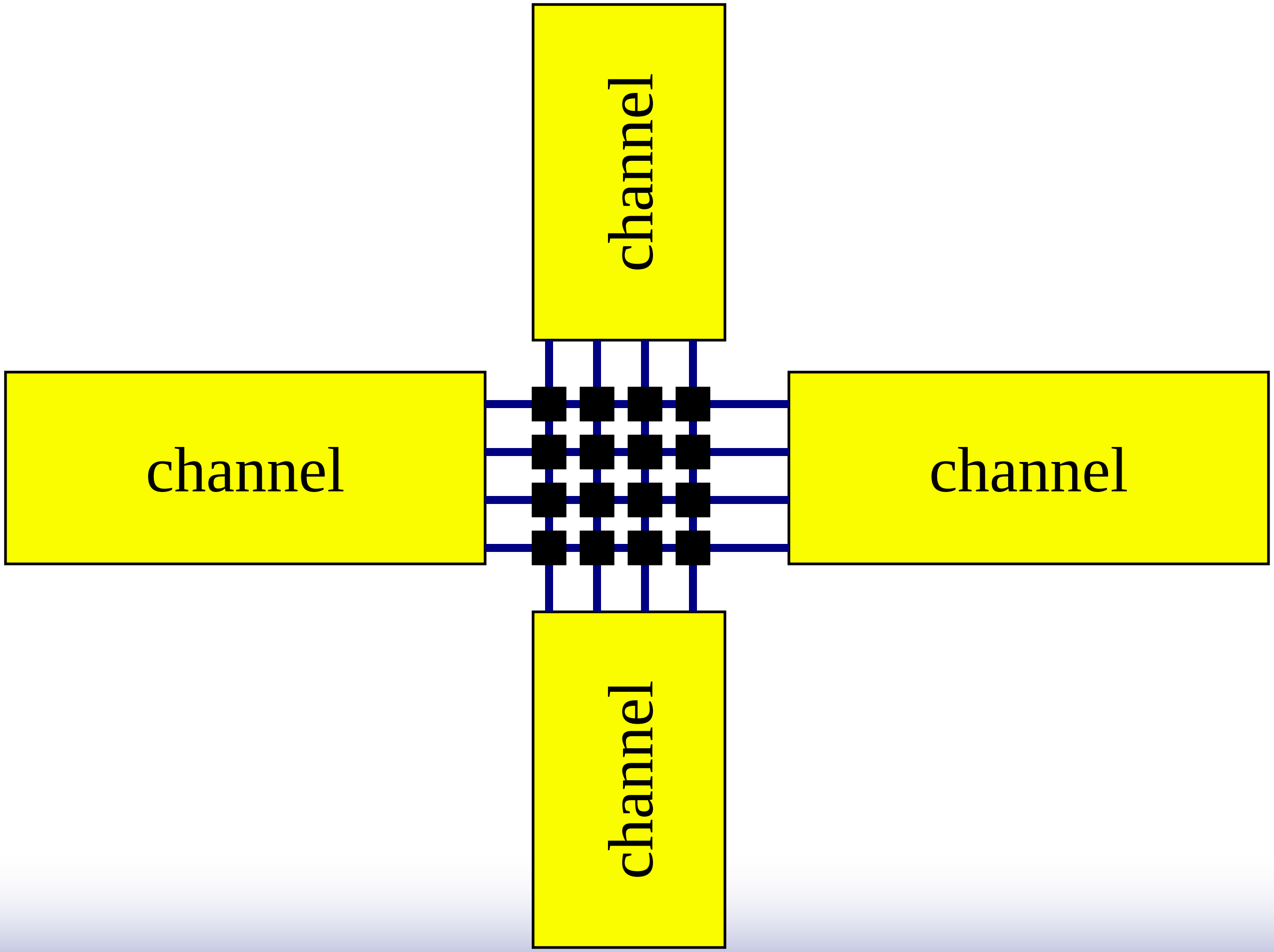


Interconnect architecture

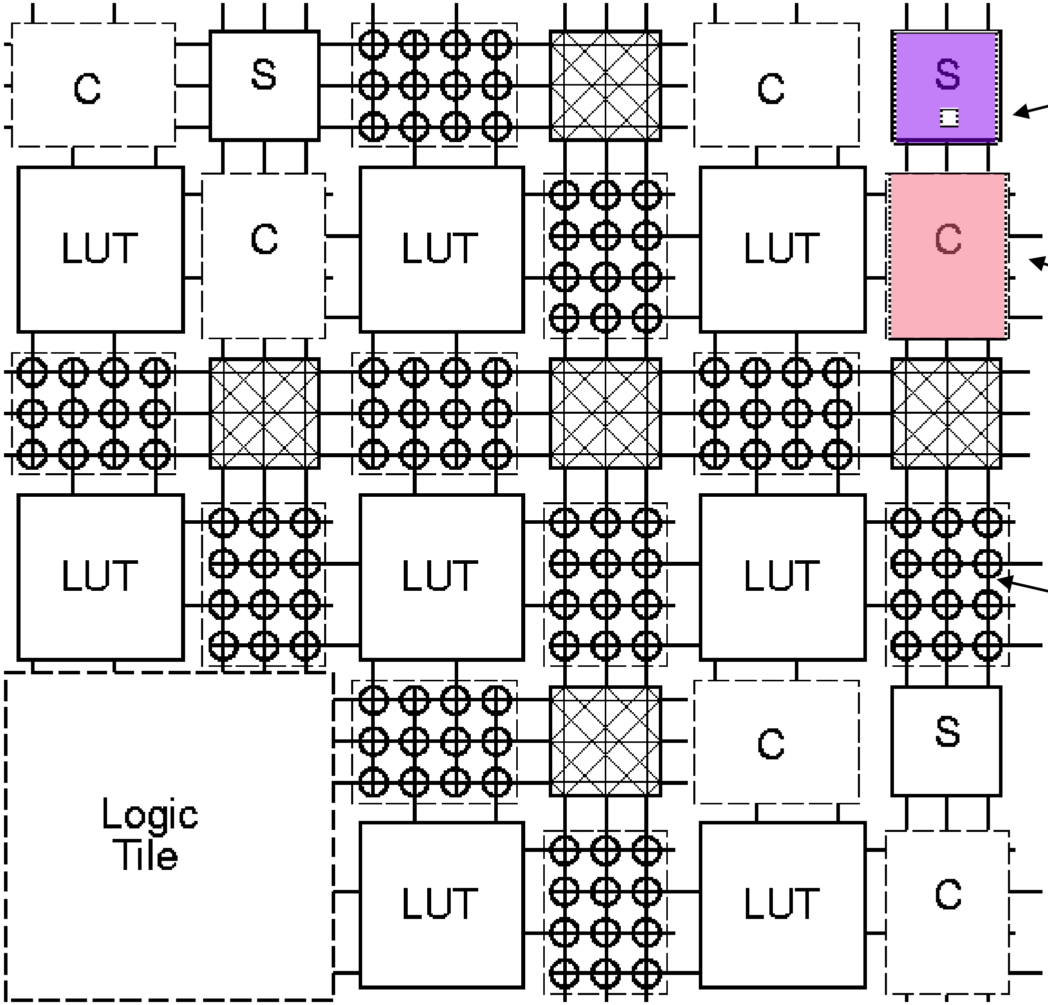
- ❑ Connections from wiring channels to LEs.
- ❑ Connections between wires in the wiring channels.



Switchbox



Mesh-based Interconnect Network



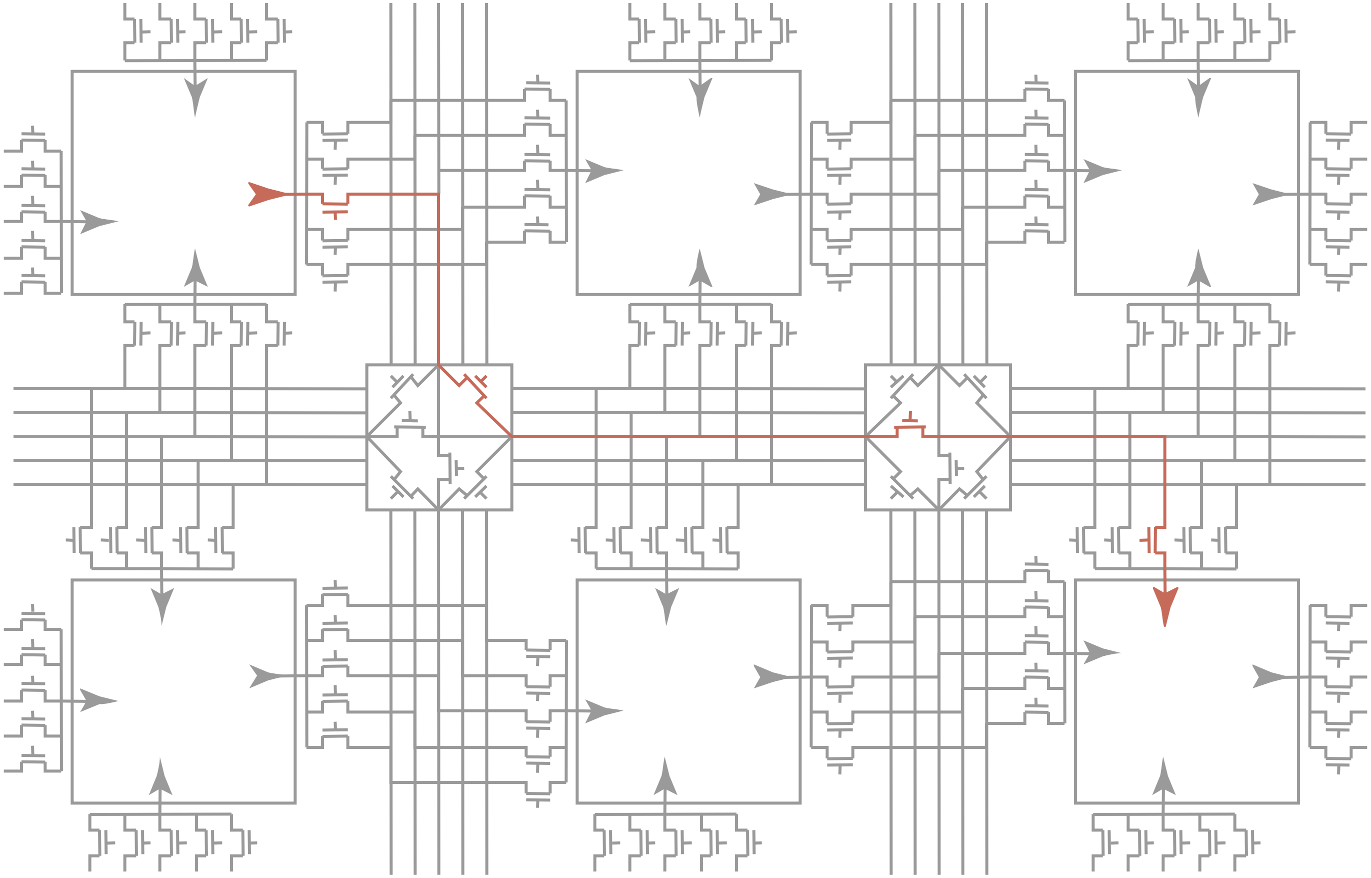
Switch Box

Connect Box

Interconnect Point

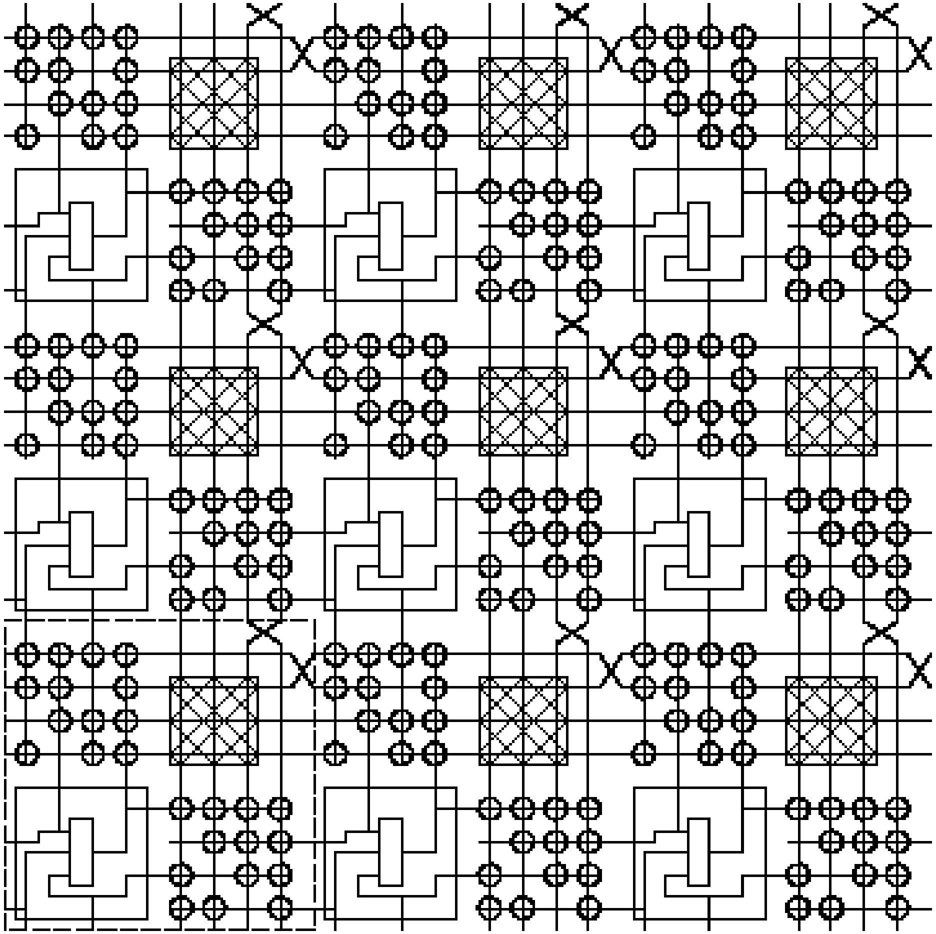
Courtesy Dehon and Wawrzyniek

Transistor Implementation of Mesh



Courtesy Dehon and Wawrzyniek

Hierarchical Mesh Network

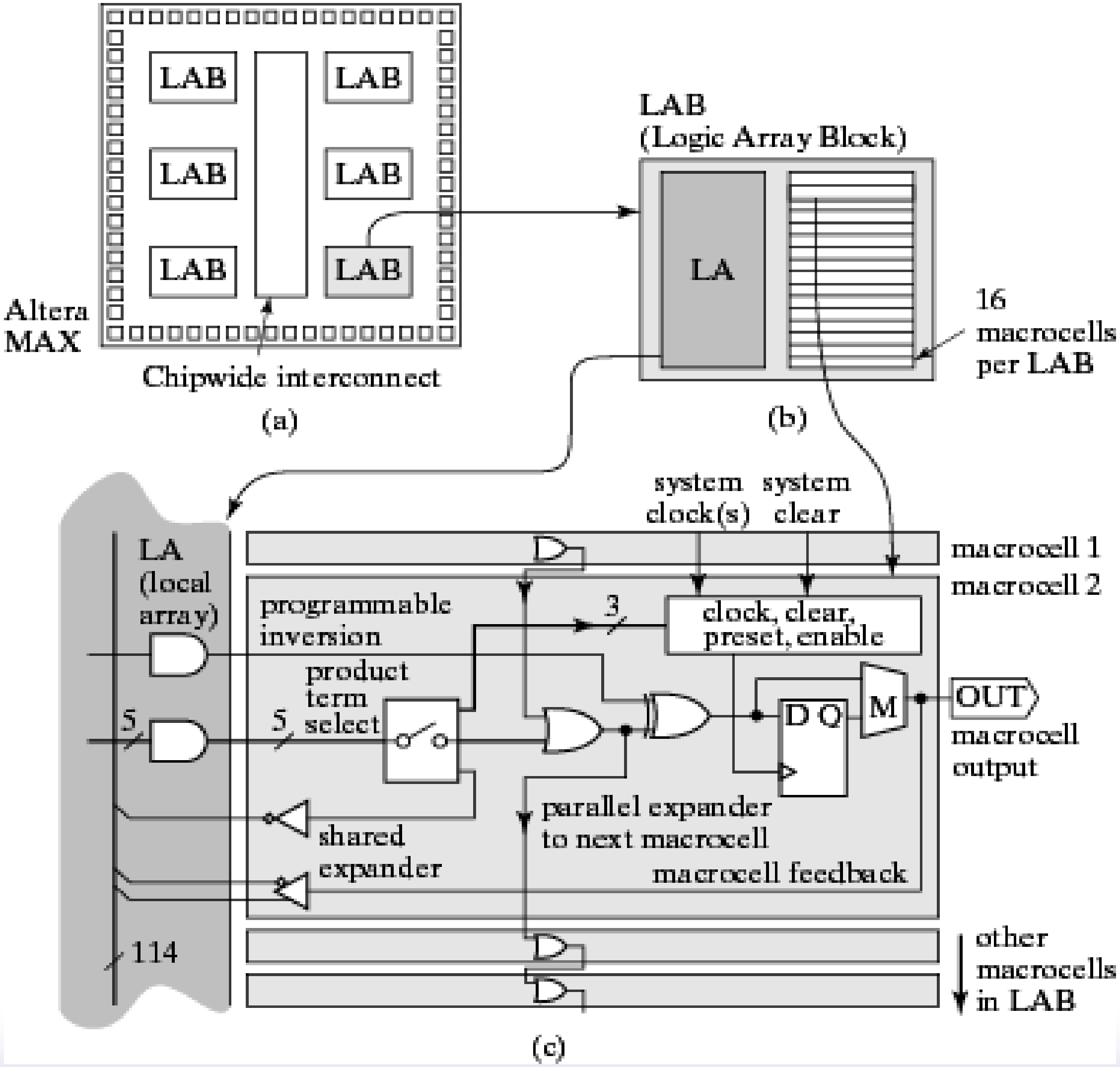


Use overlayed mesh
to support longer connections

Reduced fanout and reduced resistance

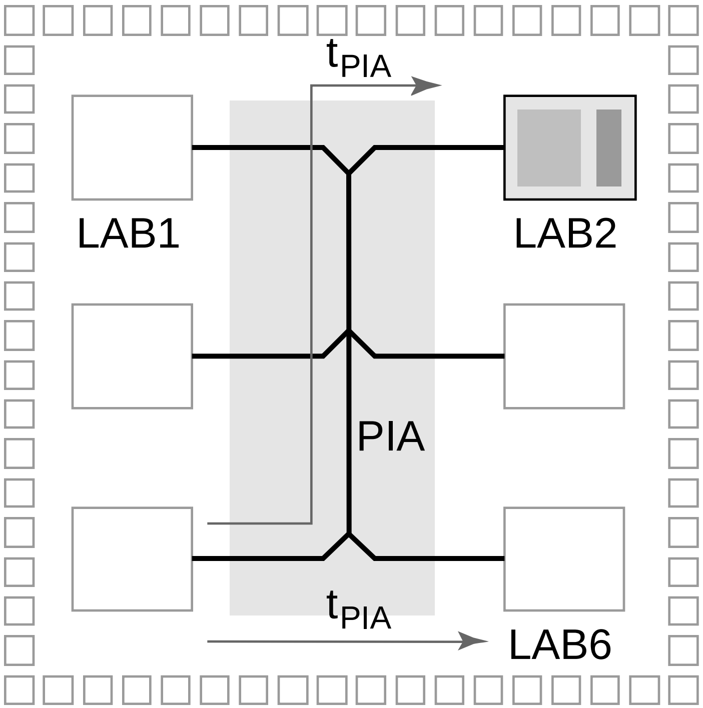
Courtesy Dehon and Wawrzyniek

Altera MAX

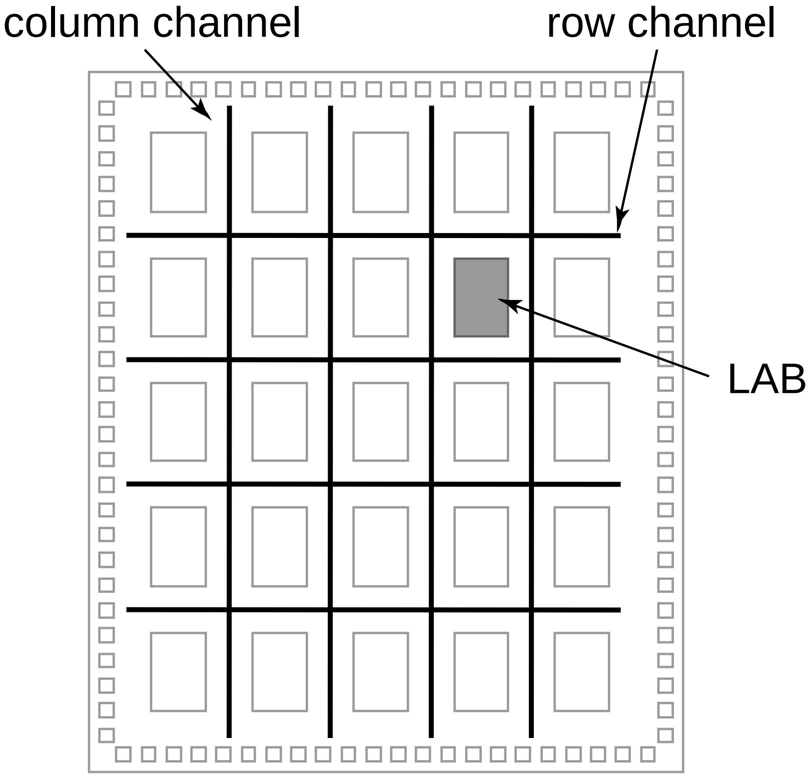


From Smith97

Altera MAX Interconnect Architecture



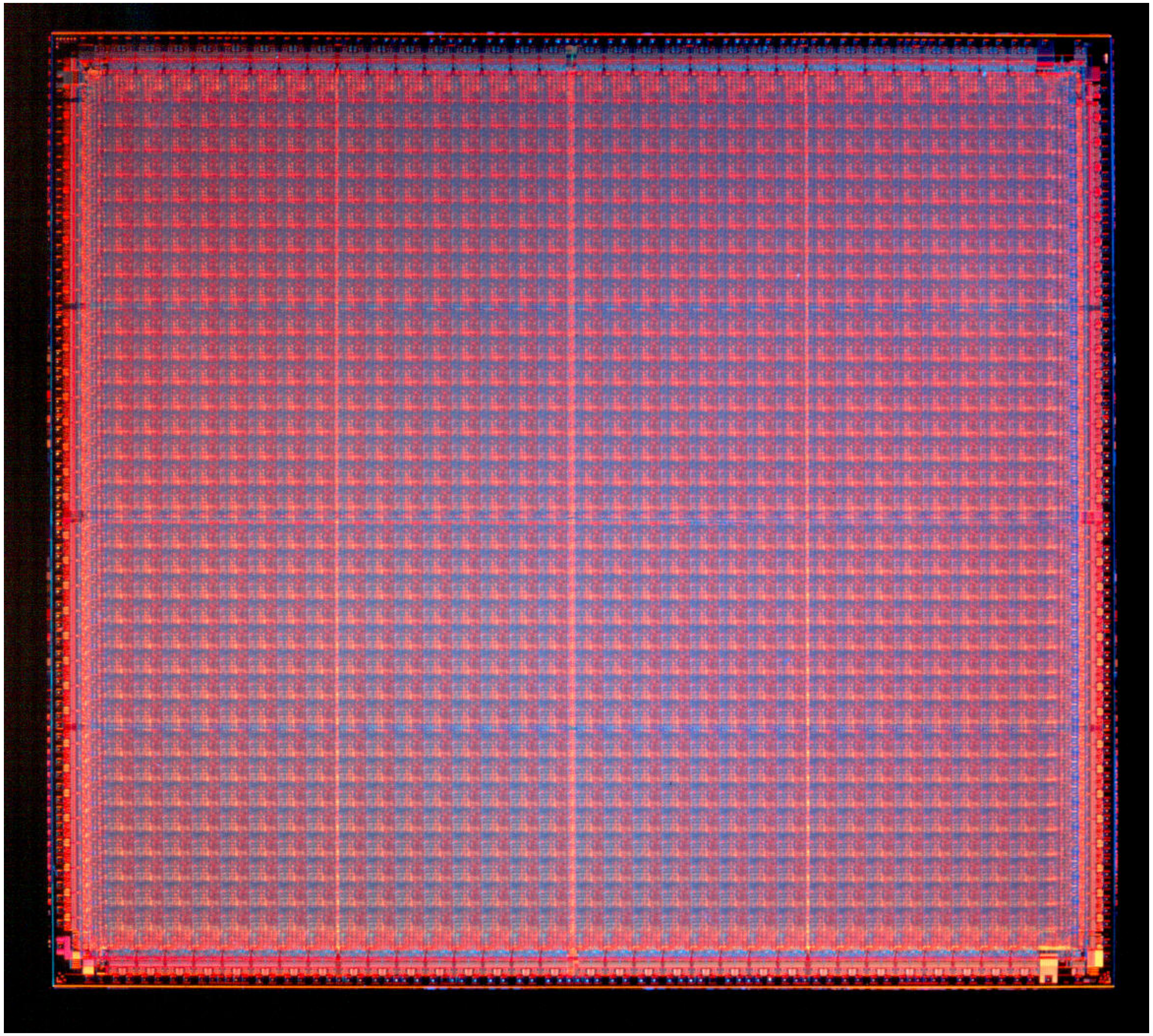
Array-based (MAX 3000-7000)



Mesh-based (MAX 9000)

Courtesy Altera

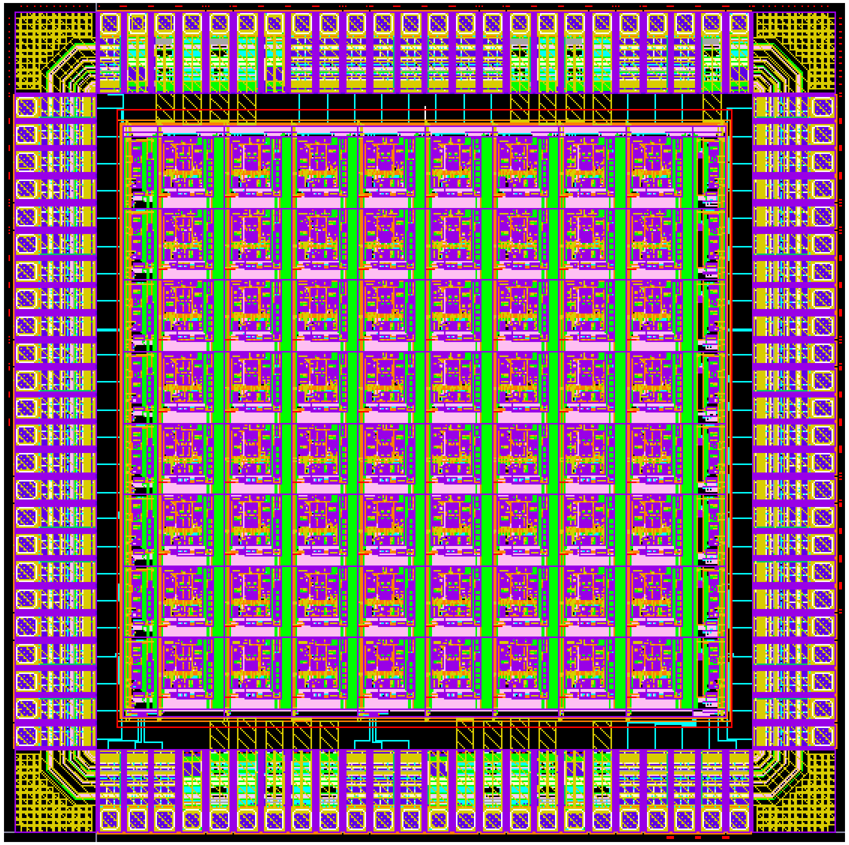
RAM-based FPGA



Xilinx XC4000ex

Courtesy Xilinx

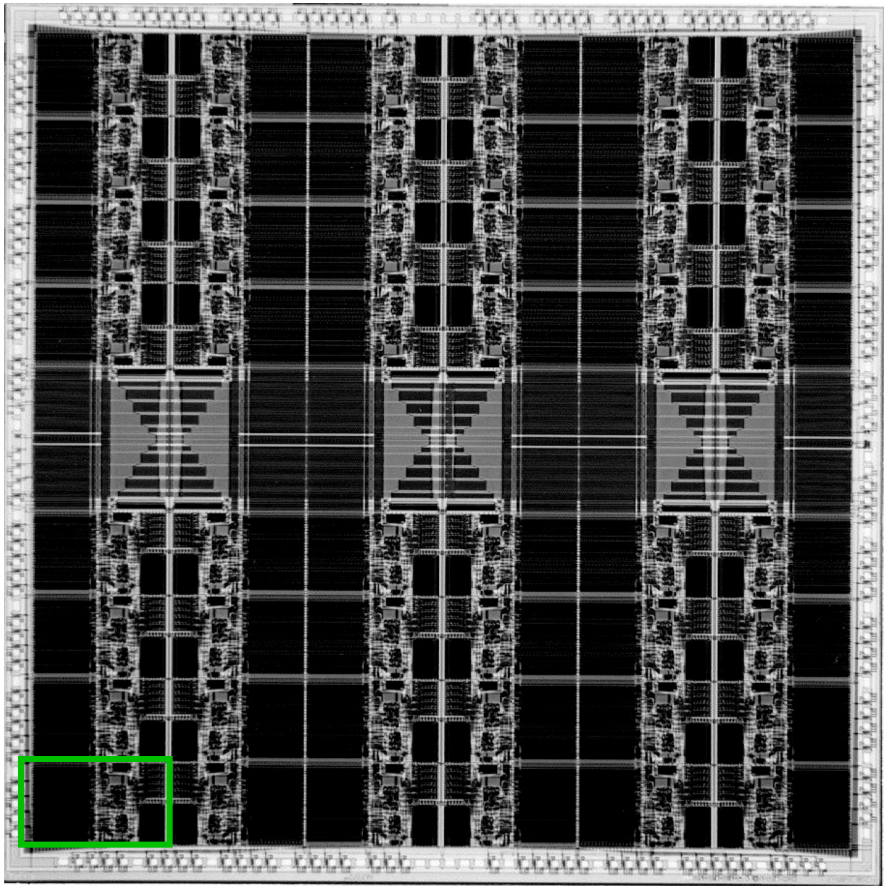
A Low-Energy FPGA (UC Berkeley)



- Array Size: 8x8 (2 x 4 LUT)
- Power Supply: 1.5V & 0.8V
- Configuration: Mapped as RAM
- Toggle Frequency: 125MHz
- Area: 3mm x 3mm

Larger Granularity FPGAs

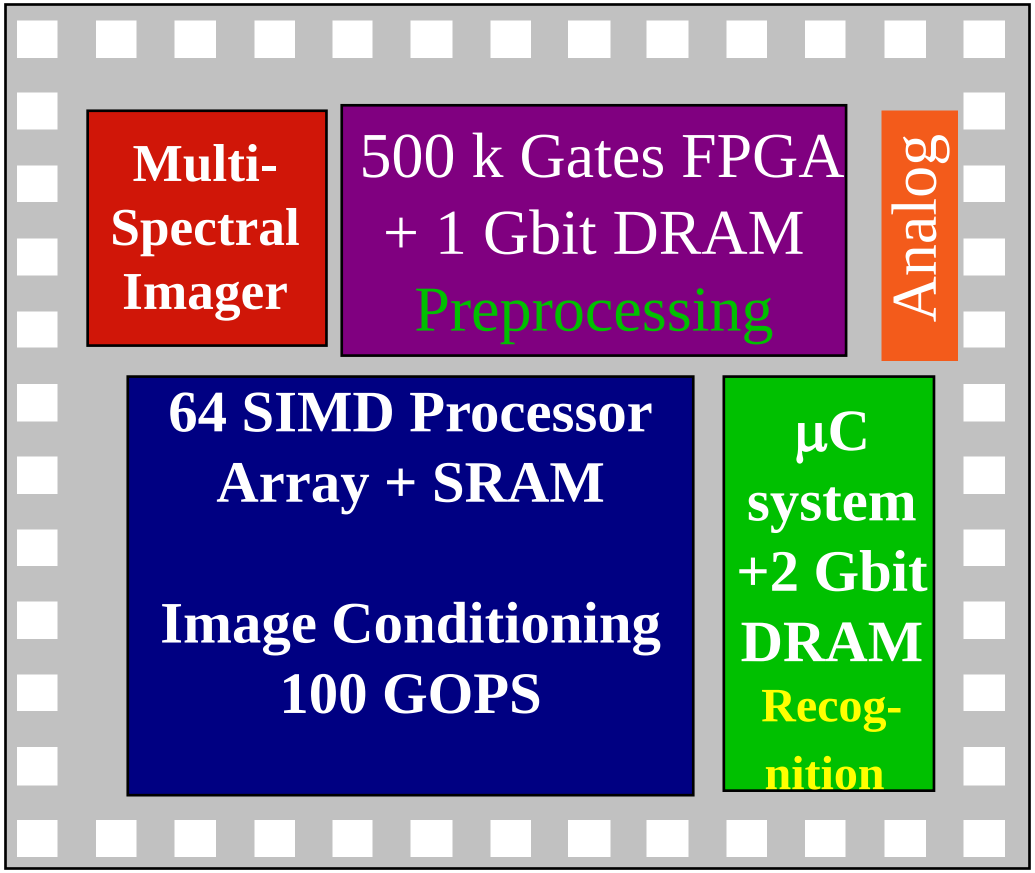
PADDI-2 (UC Berkeley)



- 1-**m**m 2-metal CMOS tech
- 1.2 x 1.2 mm^2
- 600k transistors
- 208-pin PGA
- fclock = 50 MHz
- P_{av} = 3.6 W @ 5V
- Basic Module: Datapath

Design at a crossroad

System-on-a-Chip



- Embedded applications where cost, performance, and energy are the real issues!
- DSP and control intensive
- Mixed-mode
- Combines programmable and application-specific modules
- Software plays crucial role

Addressing the Design Complexity Issue

Architecture Reuse

Reuse comes in generations

Generation	*Reuse element*	*Status*
1st	**Standard cells**	**Well established**
2nd	**IP blocks**	**Being introduced**
3rd	**Architecture**	**Emerging**
4th	**IC**	**Early research**

Source: Theo Claasen (Philips) – DAC 00

Architecture ReUse

- Silicon System Platform
  - Flexible architecture for hardware and software
  - Specific (programmable) components
  - Network architecture
  - Software modules
  - Rules and guidelines for design of HW and SW
- Has been successful in PC's
  - Dominance of a few players who specify and control architecture
- Application-domain specific (difference in constraints)
  - Speed (compute power)
  - Dissipation
  - Costs
  - Real / non-real time data

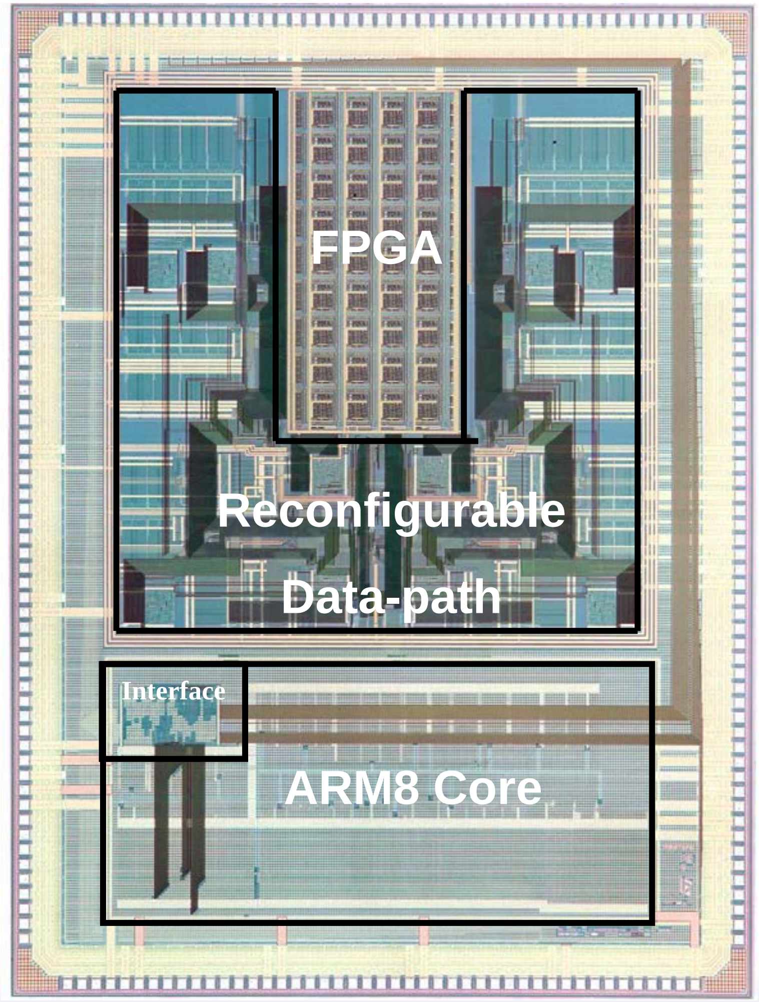
Platform-Based Design

“Only the consumer gets freedom of choice;
designers need freedom *from* choice”
(Orfali, et al, 1996, p.522)

- A platform is a restriction on the space of possible implementation choices, providing a well-defined abstraction of the underlying technology for the application developer
- New platforms will be defined at the architecture-micro-architecture boundary
- They will be component-based, and will provide a range of choices from structured-custom to fully programmable implementations
- Key to such approaches is the representation of communication in the platform model

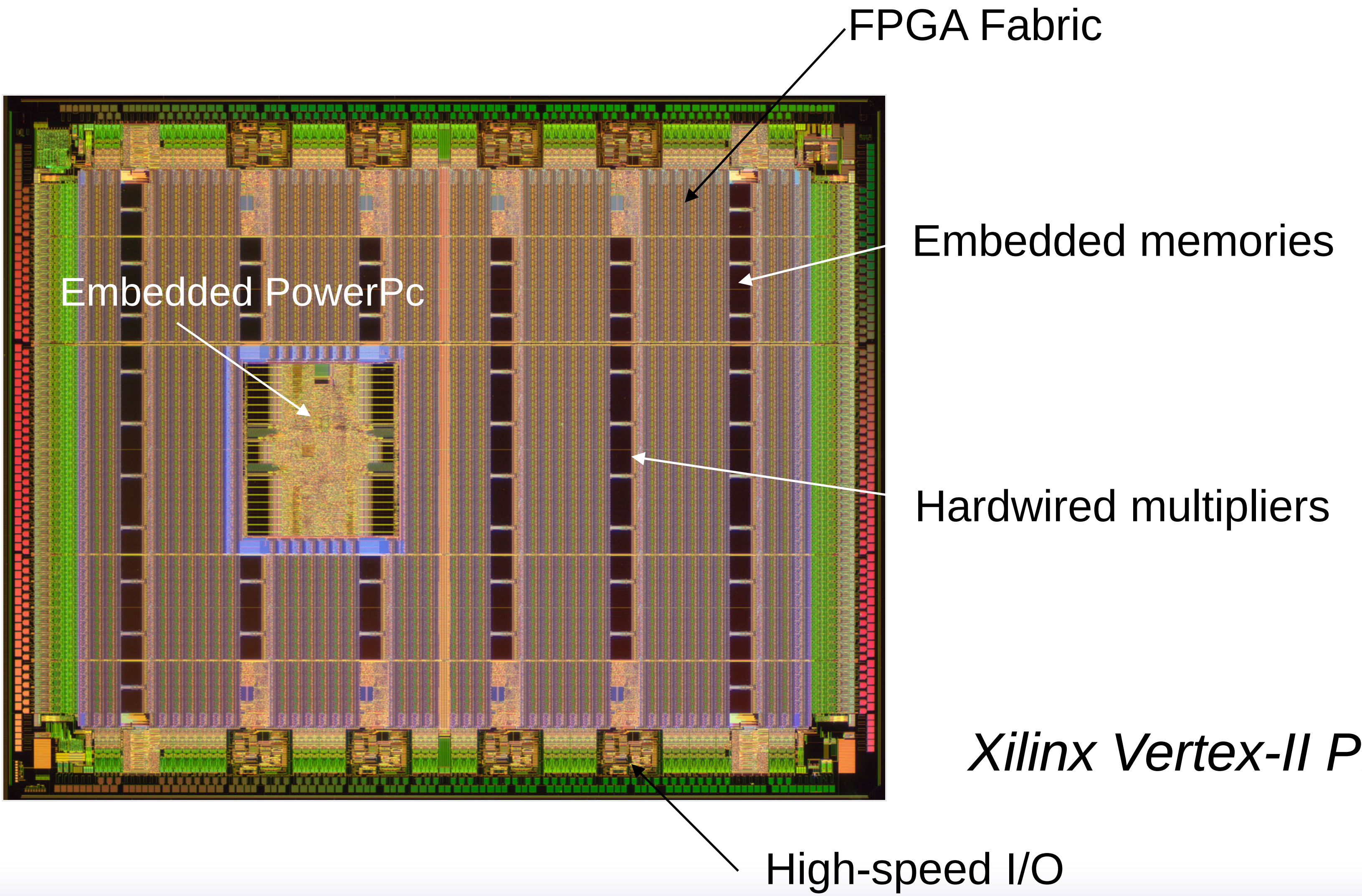
Source:R.Newton

Berkeley Pleiades Processor



- 0.25um 6-level metal CMOS
- 5.2mm x 6.7mm
- 1.2 Million transistors
- 40 MHz at 1V
- 2 extra supplies: 0.4V, 1.5V
- 1.5~2 mW power dissipation

Heterogeneous Programmable Platforms



Xilinx Vertex-II Pro

Courtesy Xilinx

Summary

- ❑ Digital CMOS Design is kicking and healthy
- ❑ Some major challenges down the road caused by Deep Sub-micron
  - ▪ Super GHz design
  - ▪ Power consumption!!!!
  - ▪ Reliability – making it work

  Some new circuit solutions are bound to emerge
- ❑ Who can afford design in the years to come? Some major design methodology change in the making!