EE 466/586
VLSI Design

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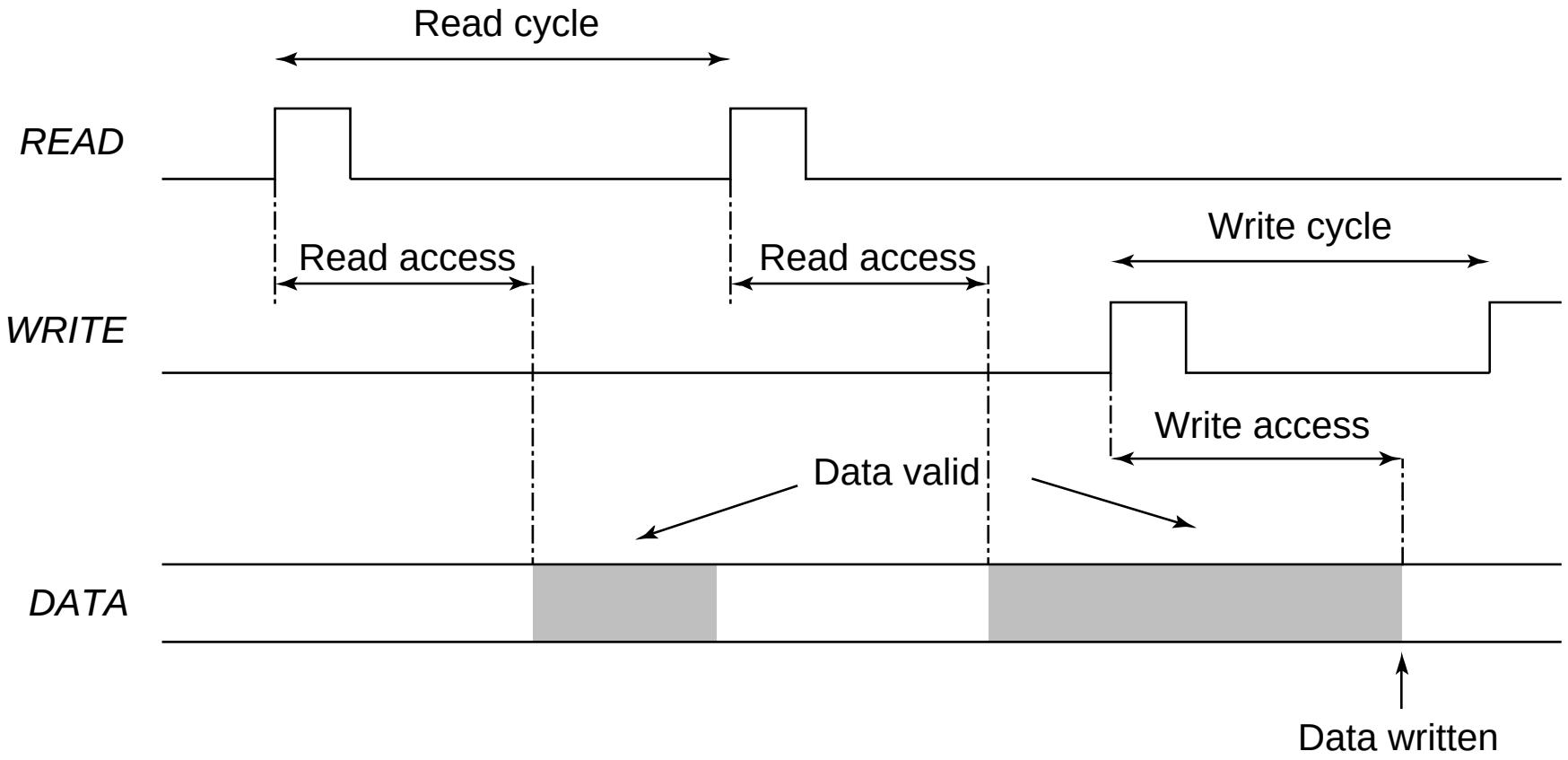
Lecture 26

Semiconductor Memories

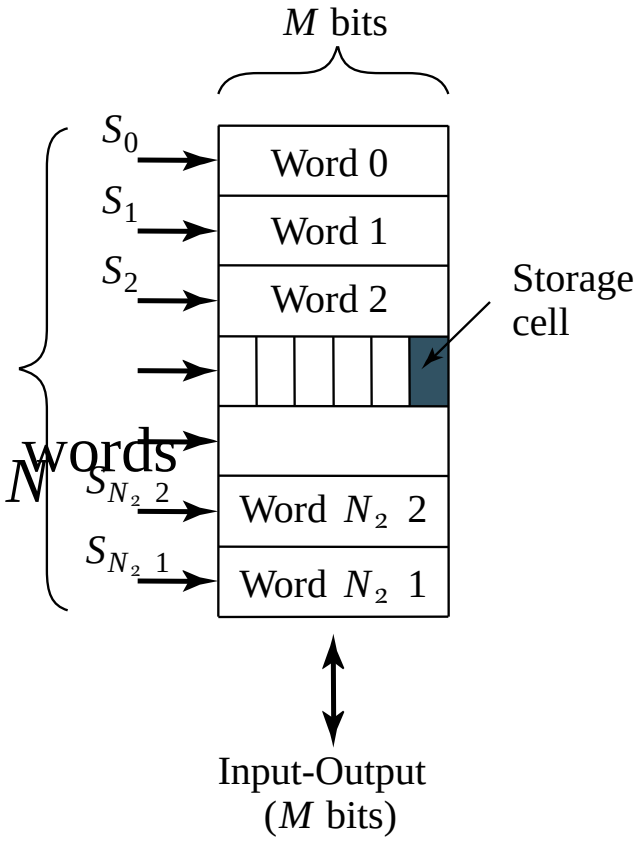
Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	Non-Random Access	EPROM	Mask-Programmed
		E^2PROM	Programmable (PROM)
SRAM	FIFO	FLASH	
DRAM	LIFO		
	Shift Register		
	CAM		

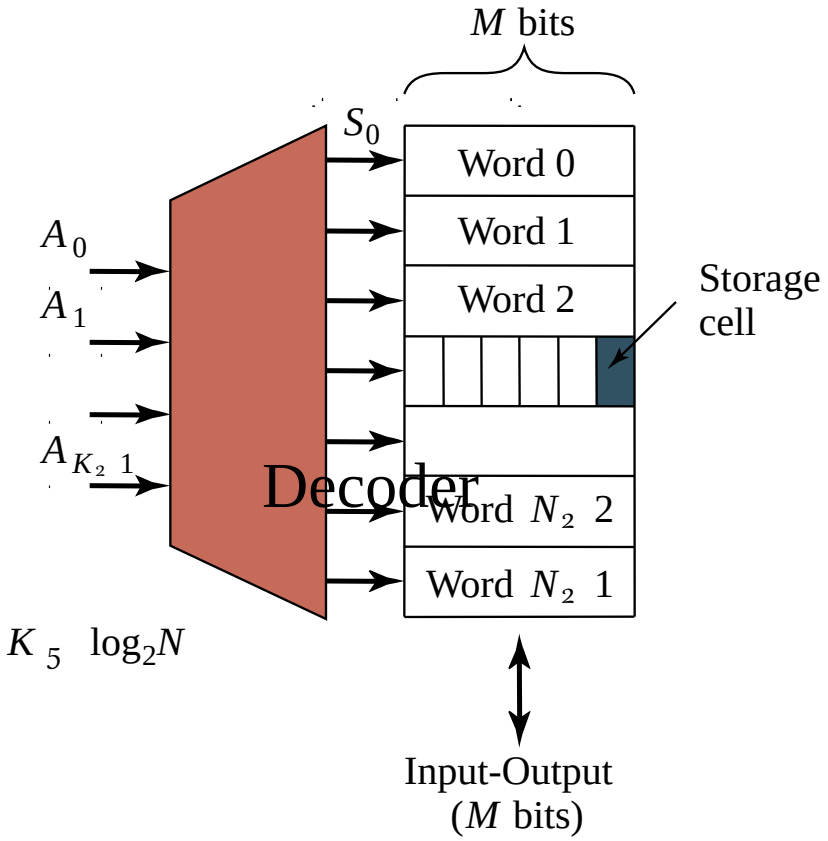
Memory Timing: Definitions



Memory Architecture: Decoders



Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

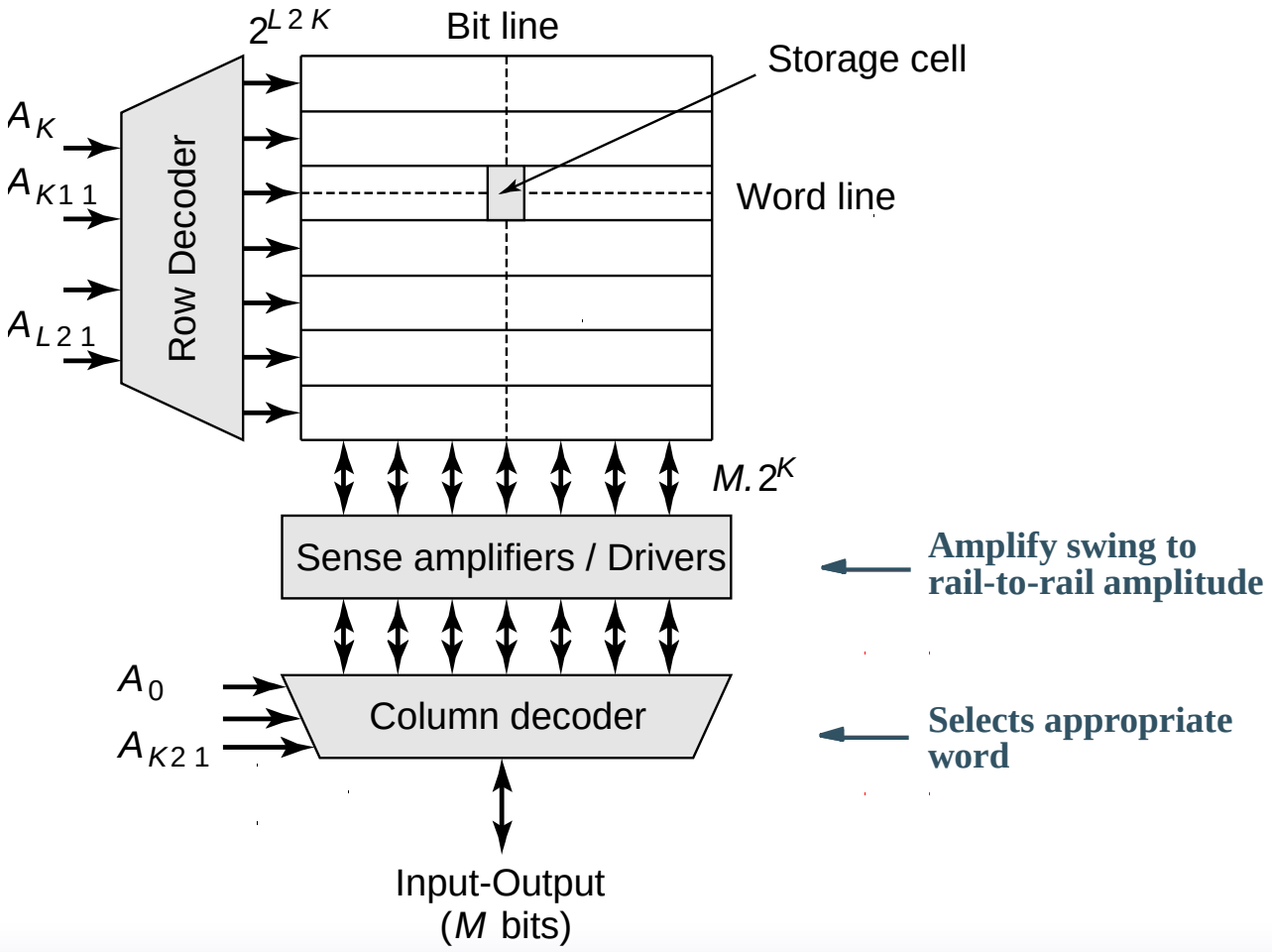


Decoder reduces the number of select signals

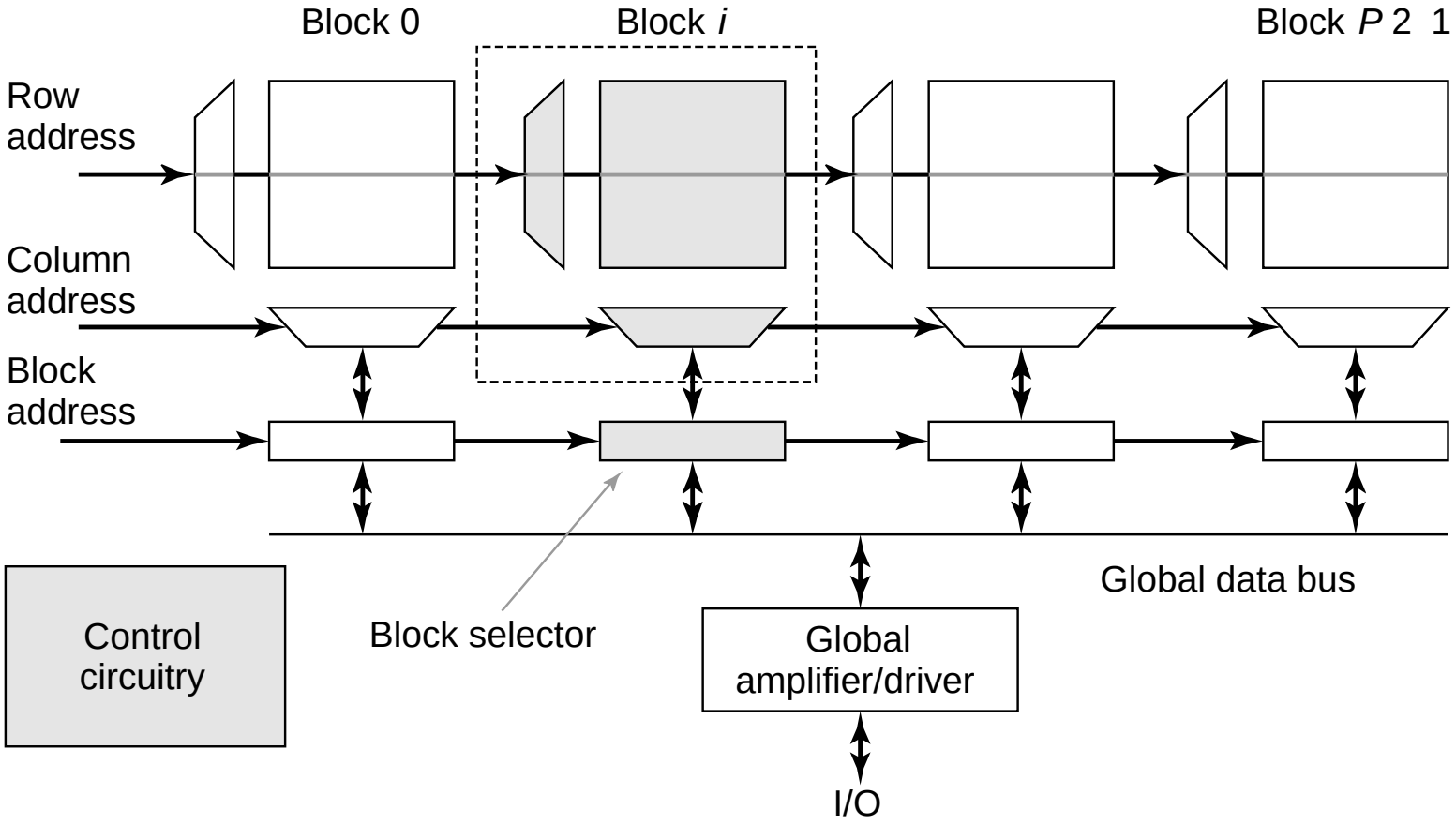
$K = log_2 N$

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH



Hierarchical Memory Architecture



Advantages:

1. Shorter wires within blocks

2. Block address activates only 1 block => power savings

Row Decoders

Collection of 2^M complex logic gates
Organized in regular and dense fashion

(N)AND Decoder

$$WL_0 = A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

$$WL_{511} = \bar{A}_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

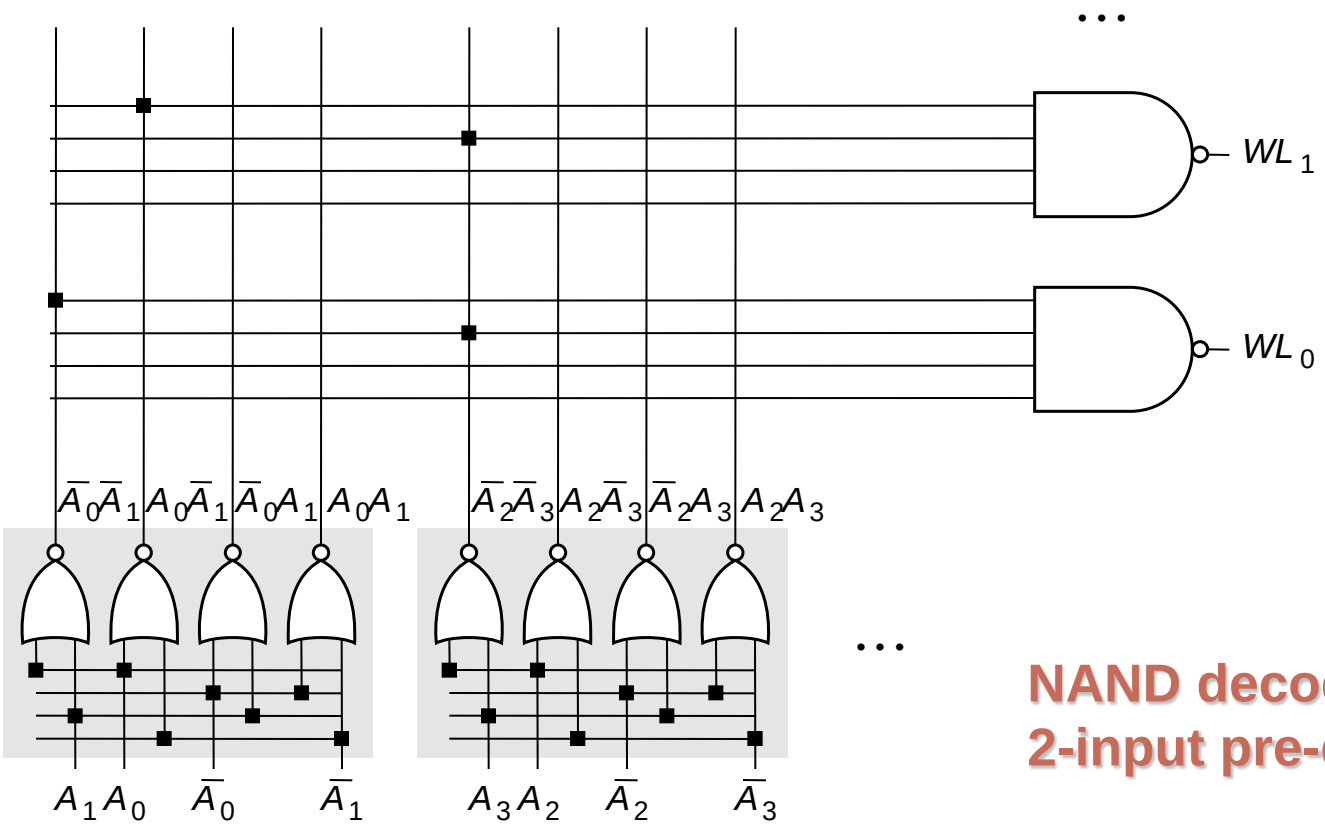
NOR Decoder

$$WL_0 = \overline{A_0 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 + A_8 + A_9}$$

$$WL_{511} = \overline{A_0 + \bar{A}_1 + \bar{A}_2 + \bar{A}_3 + \bar{A}_4 + \bar{A}_5 + \bar{A}_6 + \bar{A}_7 + \bar{A}_8 + \bar{A}_9}$$

Hierarchical Decoders

Multi-stage implementation improves performance



NAND decoder using 2-input pre-decoders

Read-Write Memories (RAM)

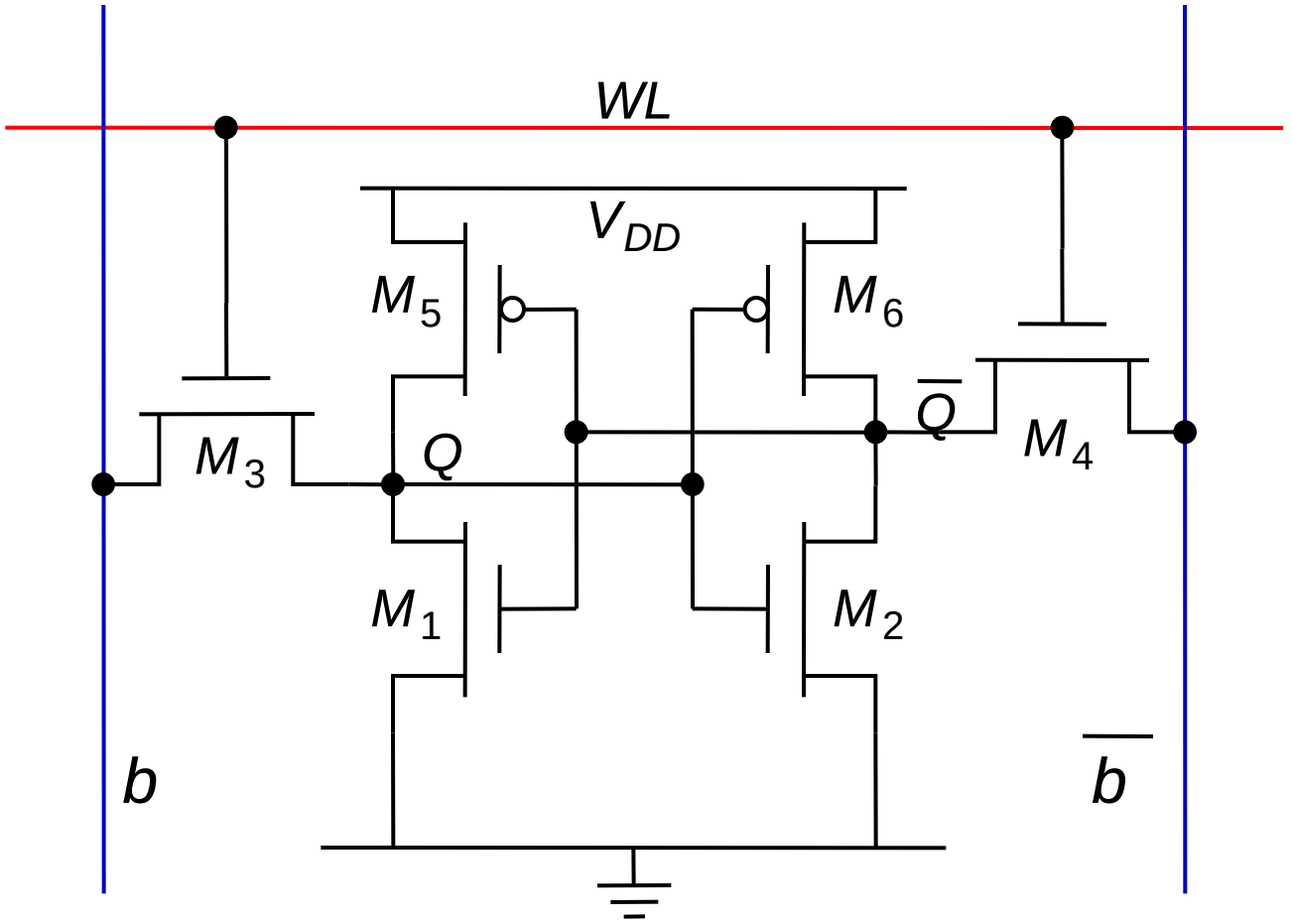
- STATIC (SRAM)

  Data stored as long as supply is applied
  Large (6 transistors/cell)
  Fast
  Differential

- DYNAMIC (DRAM)

  Periodic refresh required
  Small (1-3 transistors/cell)
  Slower
  Single Ended

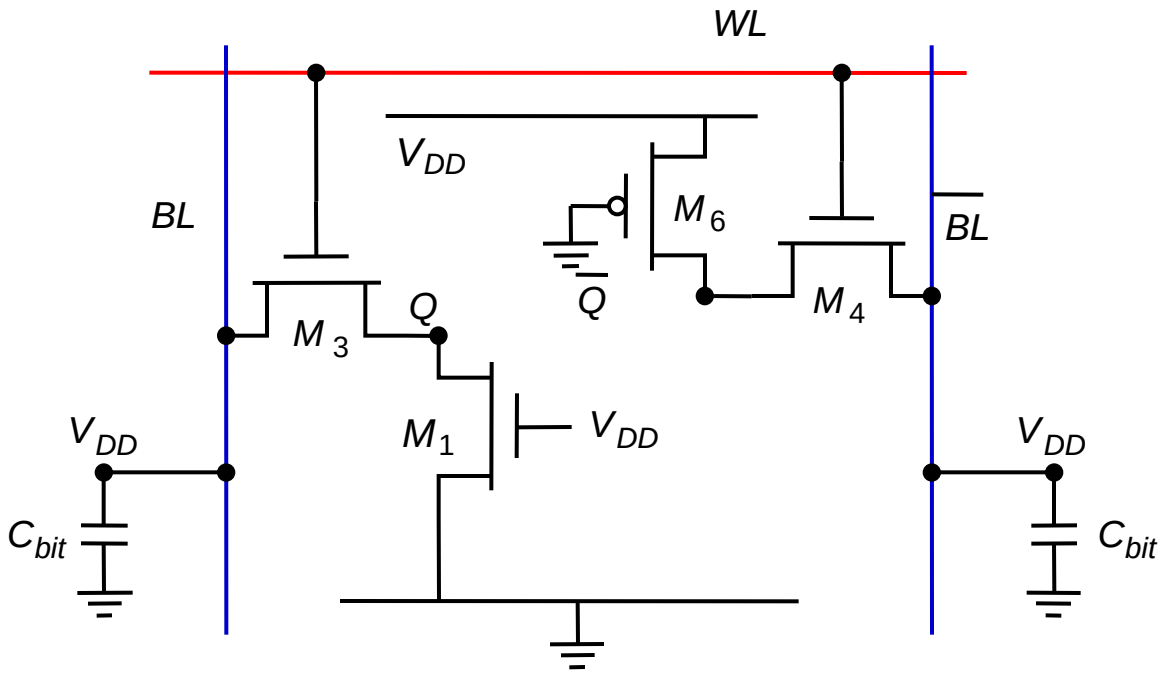
6-transistor CMOS SRAM Cell



Wordline and Bitline

- Follow board notes

CMOS SRAM Analysis (Read)



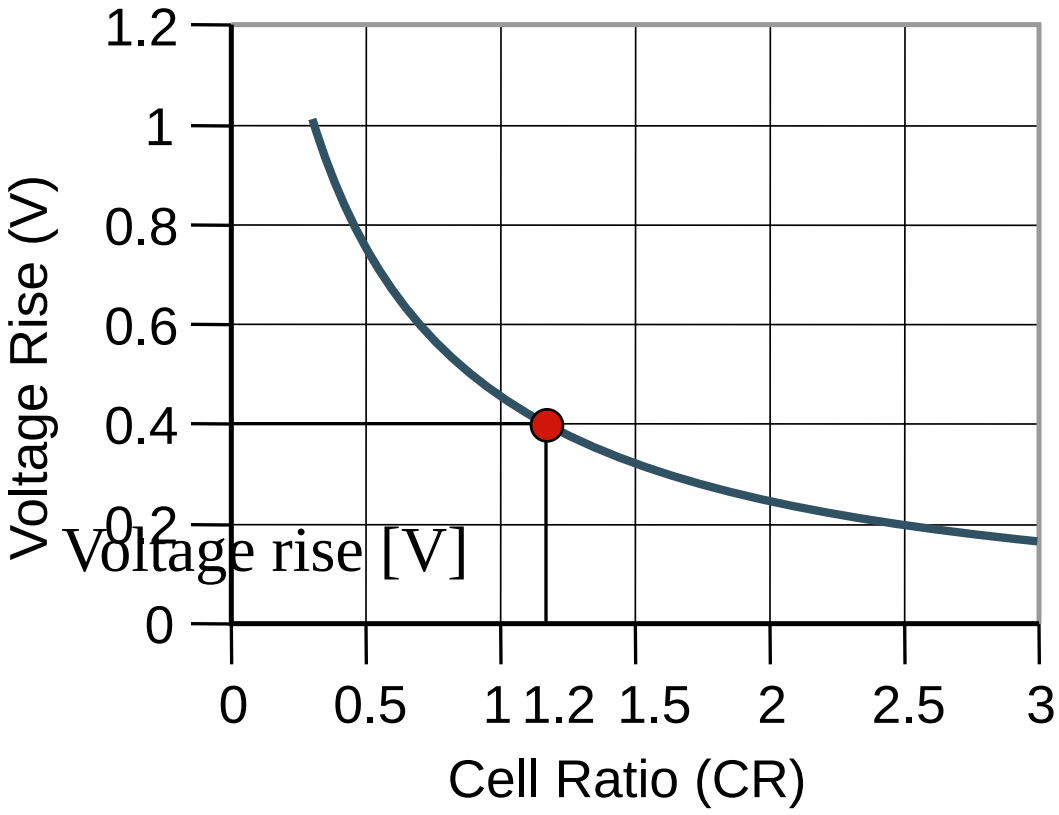
Read Operation

- Assume a “0” is stored on the left side of the cell, and a “1” on the right side.
- M_1 is on and M_2 is off.
- The row selection line is raised to V_{dd} which turns on the access transistors
- Current begins to flow through M_3 and $M_1$to ground.
- The resulting cell current slowly discharges the capacitance C_{bit}.
- On the other side of the cell, voltage on $\overline{b}$ remains high since there is no path to ground through M_2.
- The difference between b and $\overline{b}$ is fed to a sense amplifier

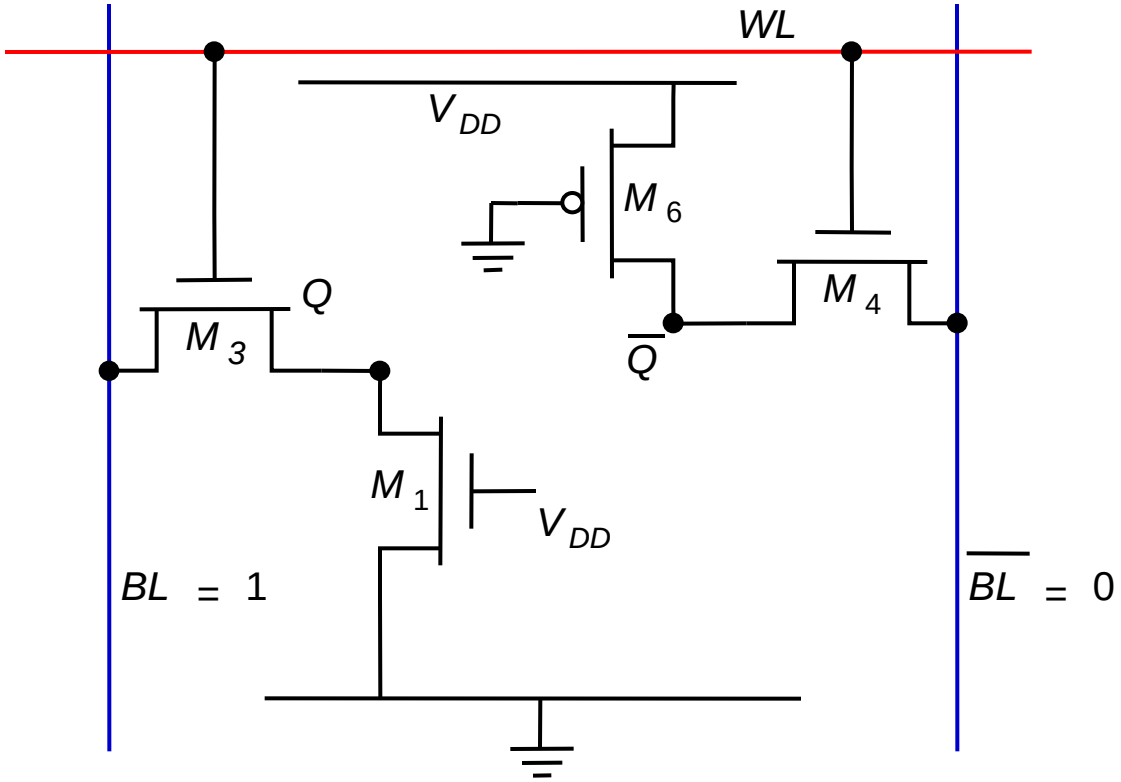
Read Operation

- Current flowing through M_3 and M_1raises the output voltage at node q which could turn on M_2 and bring down the voltage at node $\overline{q}$
  - It should not fall below V_S
  - Size M_3 and M_1appropriately.
  - Make conductance of $M_1$3 to 4 times that of M_3 so that the drain voltage of M_1does not rise above V_{TN}
- Cell discharge current
  - Follow board notes

CMOS SRAM Analysis (Read)



CMOS SRAM Analysis (Write)



Write Operation

- The operation of writing 0 or 1 is accomplished by forcing one bit line low while the other bit line remains at about $V_{dd.}$
- To write 1, $\overline{b}$ is forced low, and to write 0, b is forced low
- Conditions for writing 1
  - Conductance of M_4 is several times larger than M_6 so that the drain of M_2 is pulled below V_S.
  - M_1 turns off and its drain voltage rises to V_{DD} due to the pull up action of M_5 and M_3.
  - M_2 turns on and assists M_4 in pulling output $\overline{q}$ to its intended low value.

Write Operation

- Size transistor pair M_6 and M_4
- When the cell is first turned on for the write operation, M_6 and M_4 form a pseudo-NMOS inverter.
- Current flows through the two devices and lowers the voltage at node $\overline{q}$ from its starting value of V_{dd}
- The design of device sizes is based on pulling the node below V_s

CMOS SRAM Analysis (Write)