EE 466/586
VLSI Design

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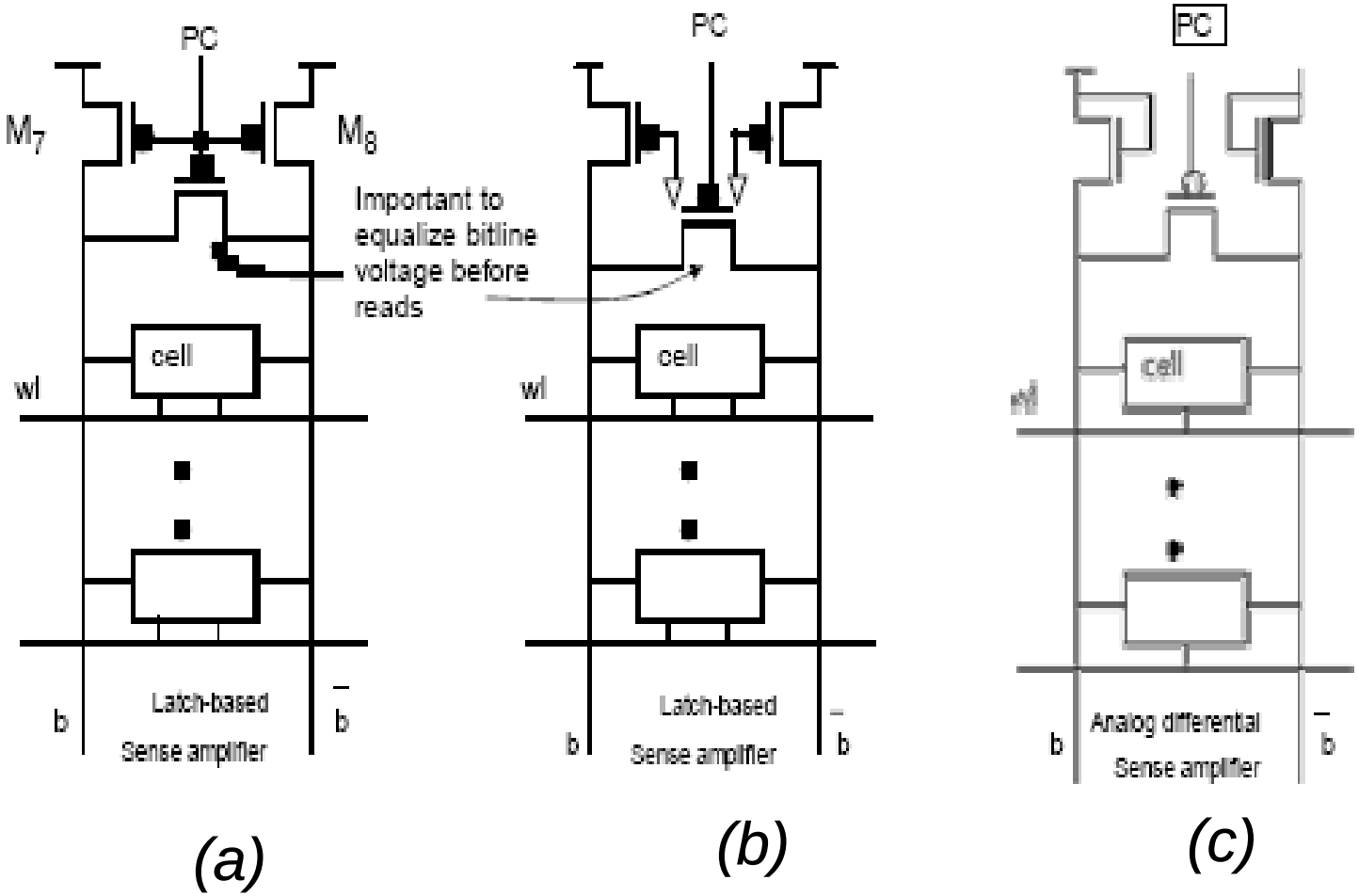
Lecture 25
SRAM Design

Column I/O Operation

- *Circuits that perform read and write on the array are column I/O*
  - *Bitline load*
    - *Can be static or precharged to around Vdd*
    - *Proper configuration depends on amplifier design*
    - *For write*
      - *– Bit lines must start at around Vdd*
      - *- Need to drive one of the bit lines to Gnd*
      - *– Mux and write driver design*
    - *For read*
      - *– Bit lines must start at around Vdd*
      - *– Swings should be small for fast operation*
      - *– Involves Mux and sense amplifier design*
      - *– Often use different I/O lines for read and write*

Bit Line load options



Column Pull-Ups

- Circuit (a)
  - The precharge signal PC, is applied to the two pull-ups and to a third transistor, called the balance transistor, connected between the two bit lines to equalize their voltage levels.
  - When the wordline (*wl)* signal goes high, one bit line remains high and the other falls at a linear rate until *wl* goes low
  - The difference between the bit lines is feed into a voltage-sensing latch-based amplifier that is triggered when the differential voltage exceeds a certain threshold

Column Pull-Ups

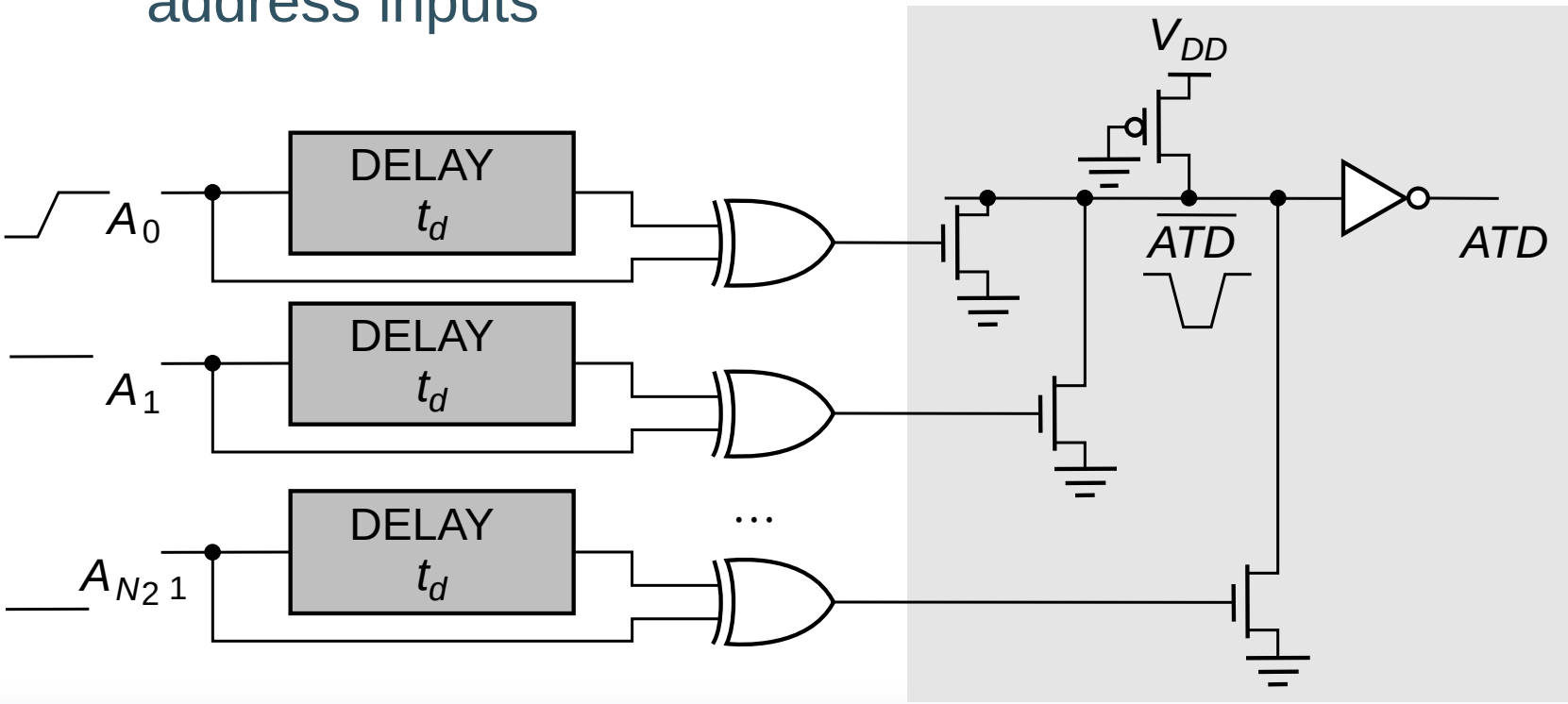
- Circuit (b)
  - Pseudo-NMOS circuits
  - Two static loads and a balance transistor form the precharge circuit
  - When PC is applied to the balance transistor, it equalizes the two voltage levels.
  - Once the bit lines are precharged, the PC signal is turned off
  - At this point the wordline can be activated
  - Suitable for current sensing amplifiers since there is continuous current flow

Column Pull-Ups

- Circuit (c)
  - NMOS saturated enhancement load
  - Maximum possible voltage on the bit line V_{DD}-V_T.
  - Suitable for differential voltage sensing amplifiers

Generation of PC signal

- Address Transition Detection (ATD) circuit.
- The ATD signal is triggered by any transition on the address inputs



Write Circuitry

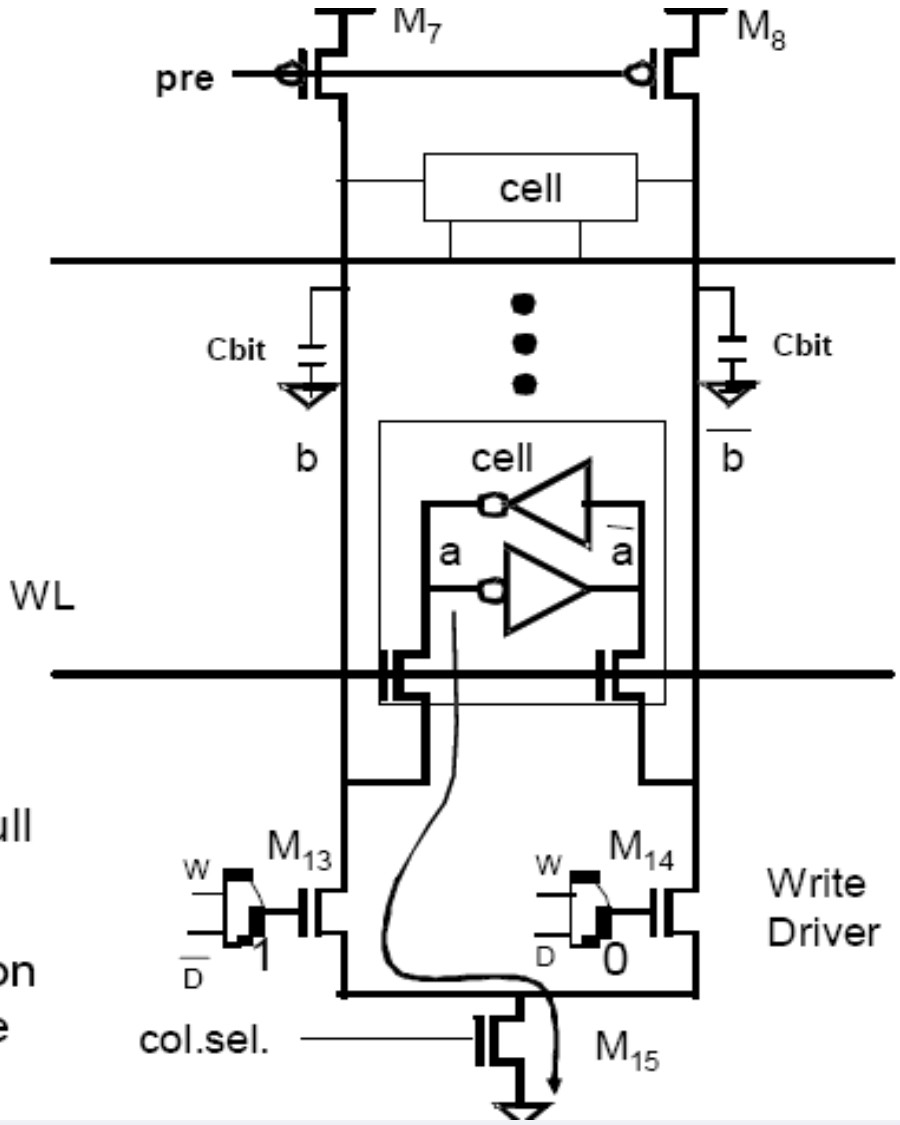
- Precharge bitlines high
- Pull one column line low
- Turn on word line
- Wait until internal values

of cell are established

- Turn off word line
- Design precharge transistors

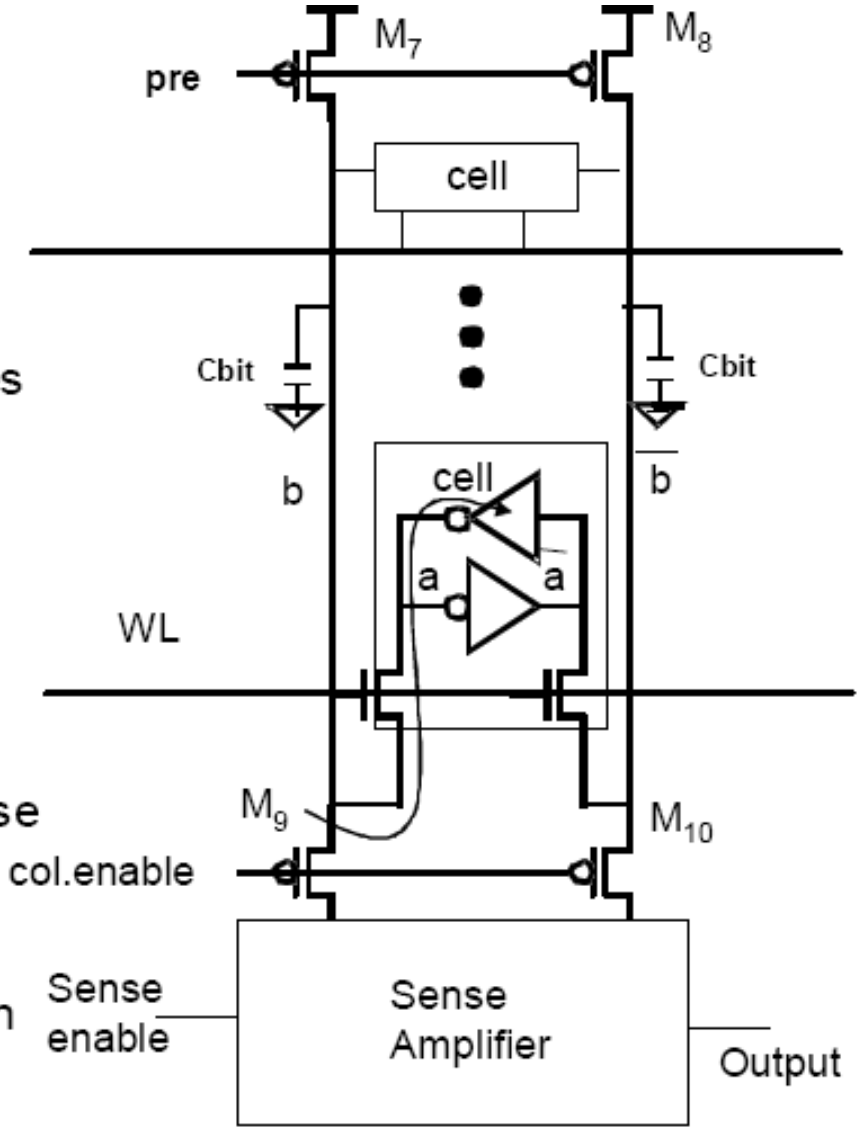
to pull bit lines high

- Design write drivers to pull one
- side going low depends on data value (in this case the left side, b, is pulling low)



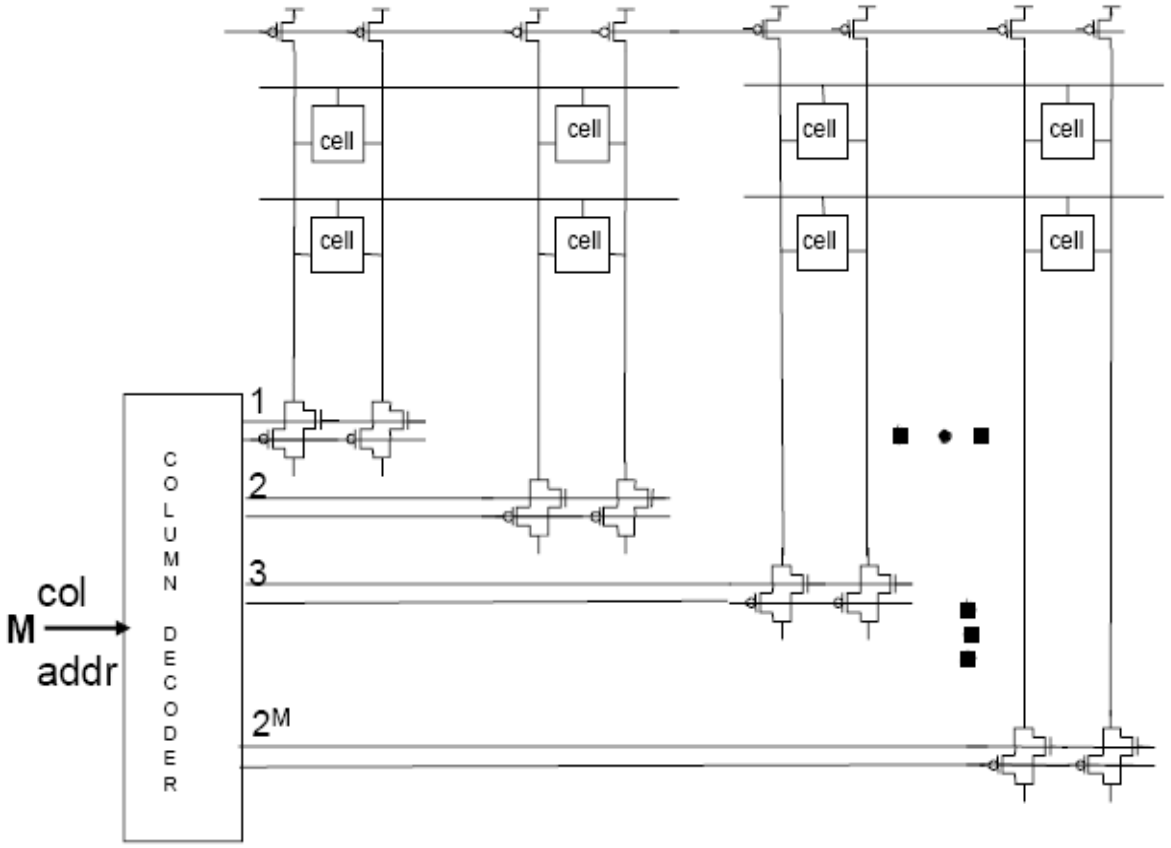
Read Circuitry

- Precharge bitlines high
- Turn on word line
- One line will slowly discharge
- Wait until bit line reaches required low voltage level
- Turn on column select
- Amplify difference with sense amplifier
- Design sense amplifier based on desired response time and power requirements
- Use precharge based on type of sense amp used.

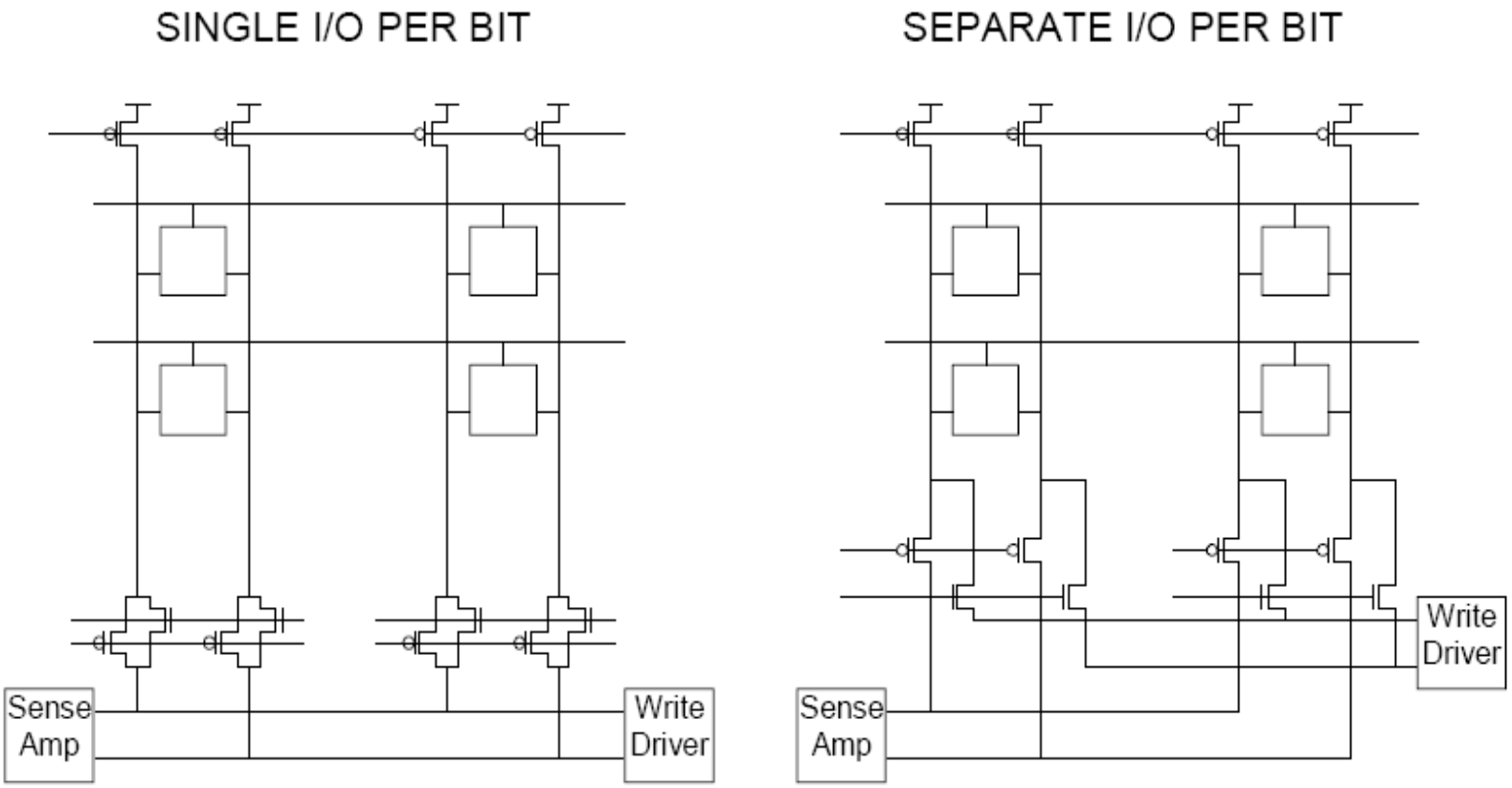


Column Decoder

- Need decoder for column address followed by a mux to select column for input or output operations
- Require two outputs to drive complementary pass gates
- Since the requirements for read and write are different can use separate read and write IO lines
- Have PMOS access for the read IO lines, since the read happens near Vdd
- Have NMOS devices for the write IO lines, since you need to drive bitlines to Gnd (see next slide)



Column Muxing



Multi-Level Column Decoding

•Alternatives for column selection are tree decoder, regular decoder + pass transistor, or some combination of the two

•Shown on the right is a tree decoder

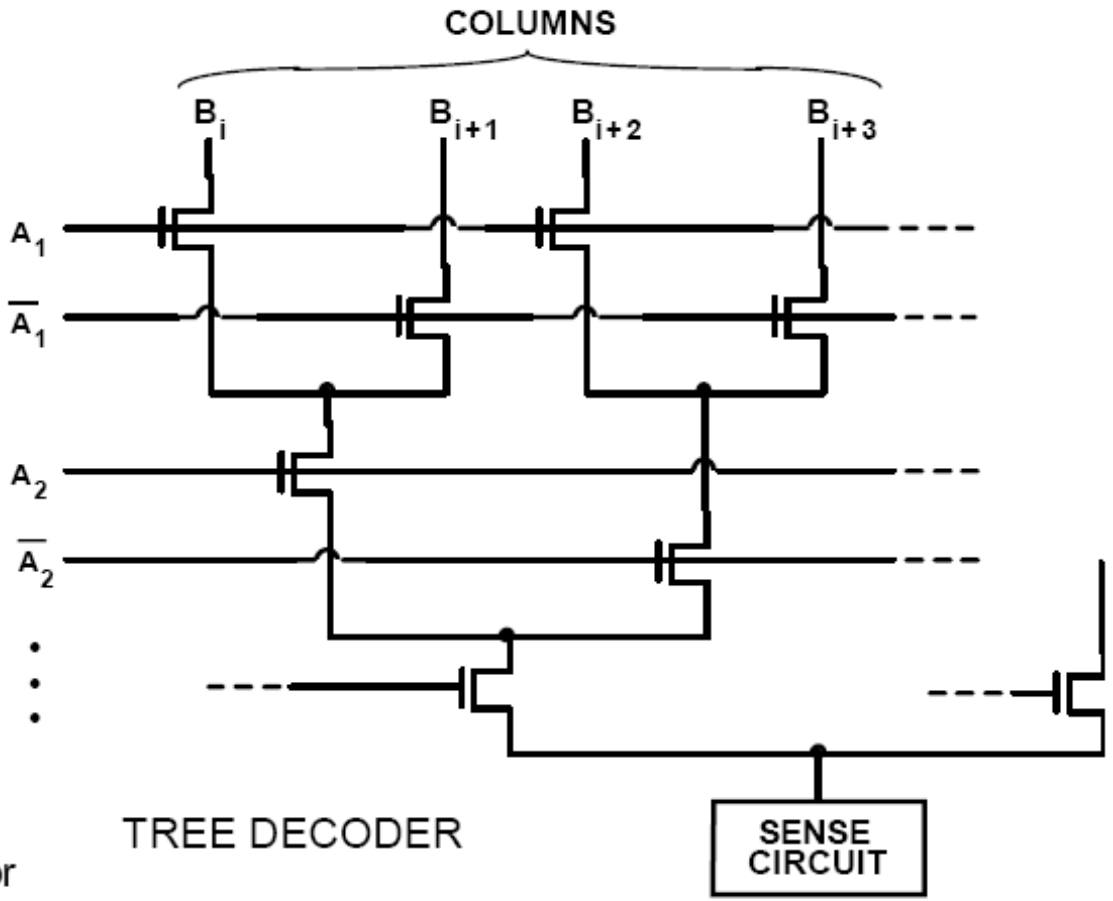
– switches driven directly by address bits and their complements

–total of 2^{M+1} devices

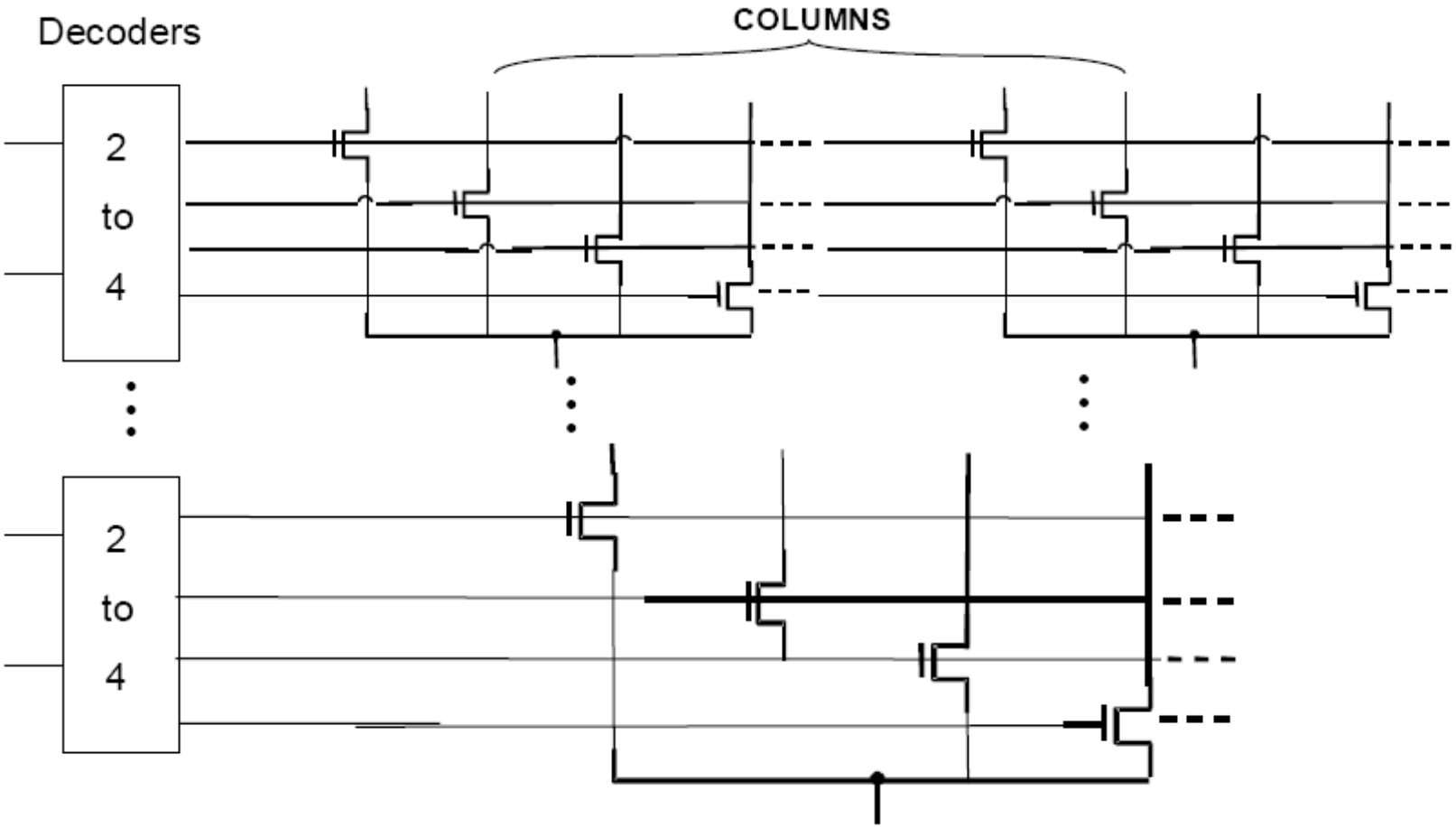
–large devices to reduce resistance

–long paths -> large C -> SLOW

• To speed up, add buffers or use adjust sizing of devices



Other Options for Column Decoder

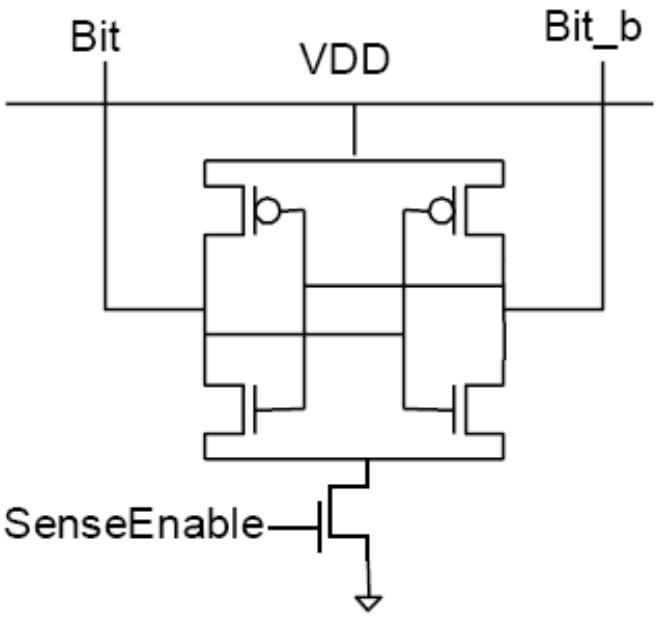


Sense Amplifiers

- We need a sense amplifier to handle small voltage swings on the bit lines for fast operation
- Normally you need to choose between
  - Drawing DC power (analog differential sense amplifier)
  - Using a clock edge (latch-based amplifier)
- For Analog Sense Amplifier
  - All devices in high-gain saturation region – fast switching
- For Latch-based Amplifier
  - Nothing can happen until an enable transistor turns on
  - And even then you need to wait some more for gate to switch
  - low gain region of transfer curve (slow)
- We will use latch-based amplifier for lower power

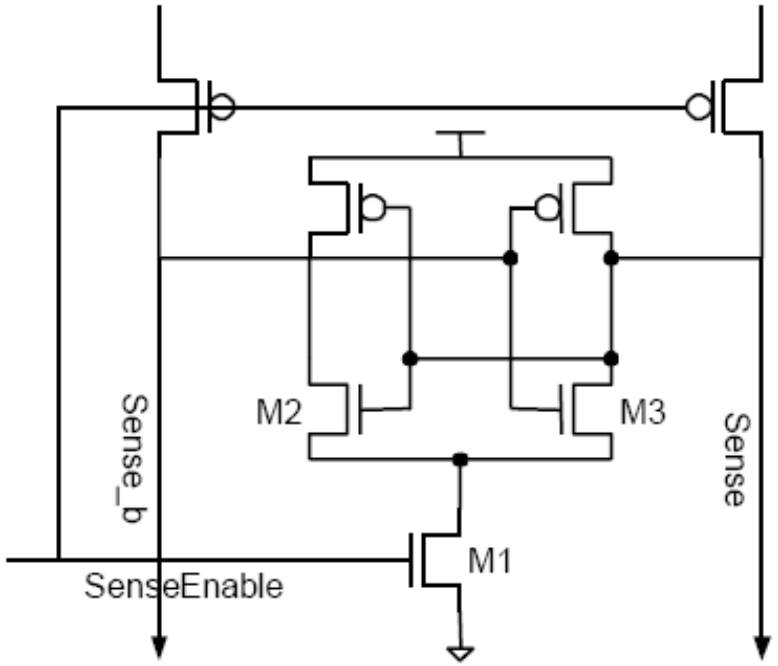
Latch-Based Sense Amplifier

- It must sense a very small signal
- It must consume a small area
  - Need one for each bitline
  - Or sets of bitline (4 or 8)
- Simplest design:
  - Two back-to-back inverters
  - Add a clocked pulldown
- Once Bit and Bit_b are established, turn on pulldown device to activate inverters
- Side with lower voltage will drop to 0V while the other side stays high

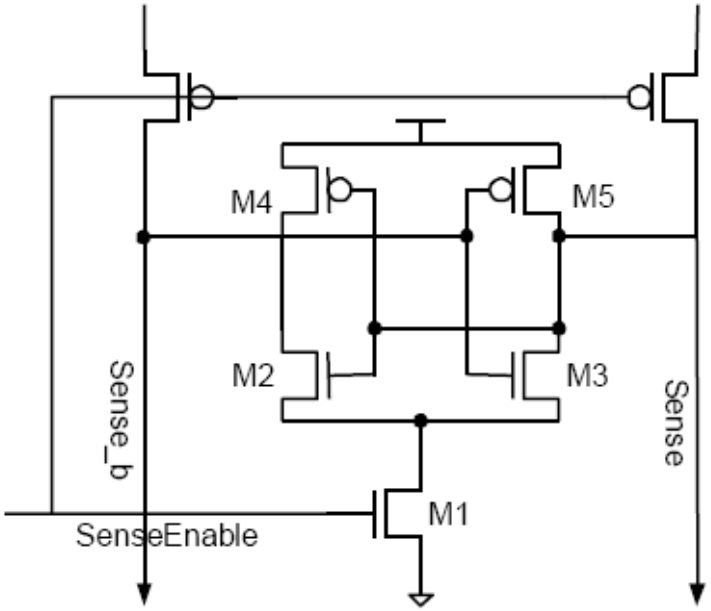


Latch-Based Sense Amplifier

- Three stages of operation
  - Precharge
  - Sample
  - Regenerate
- At the end of sample
  - Small bitline voltage on sense and sense_b
- Regenerate
  - M2 and M3 turn on
  - Voltage difference causes current difference
  - Which causes larger voltage difference

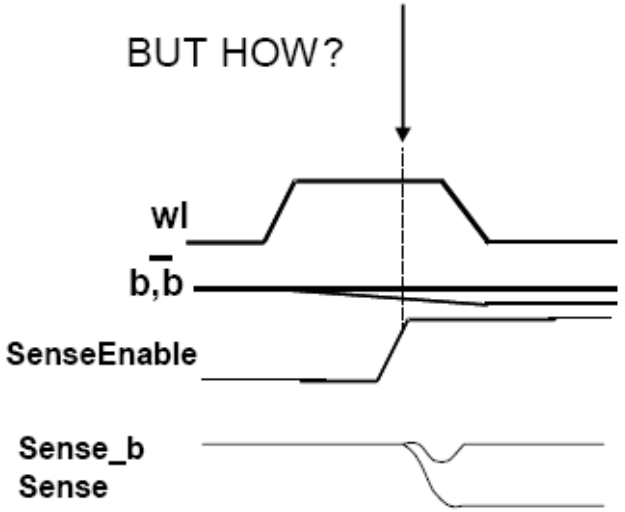


Timing Issues

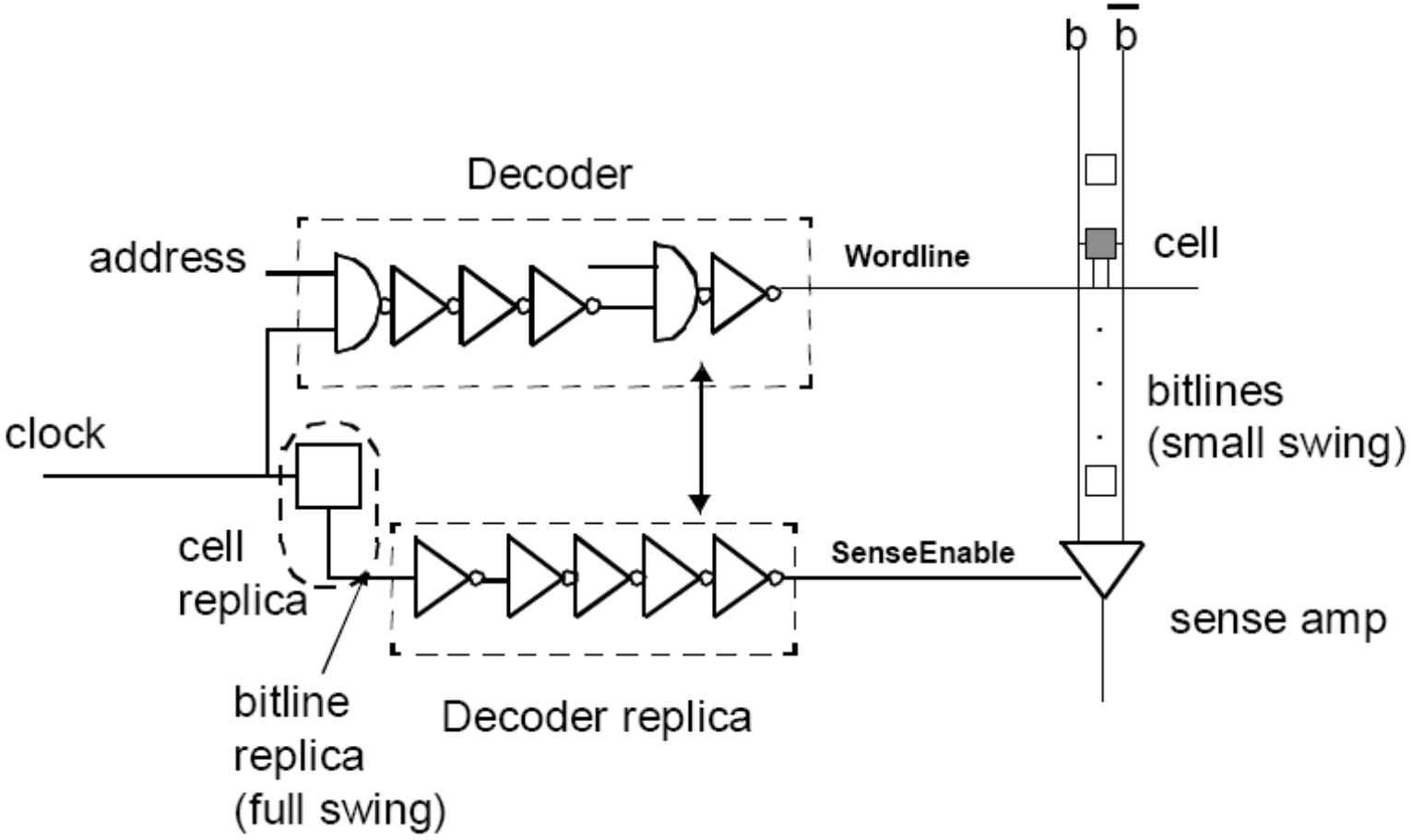


Need to guarantee that signal arrives at this point even with process variations.

BUT HOW?



Replica Circuit



Bit Line Replica