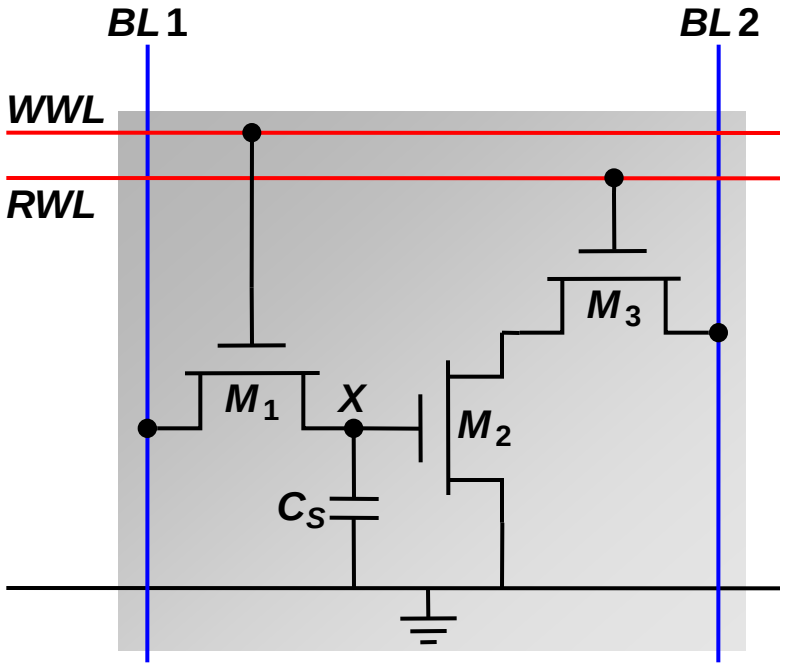
EE466/586
VLSI Design

Partha Pande
School of EECS
Washington State University
pande@eecs.wsu.edu

Lecture 26
Memory Design (Cont'd)

3-Transistor DRAM Cell



No constraints on device ratios

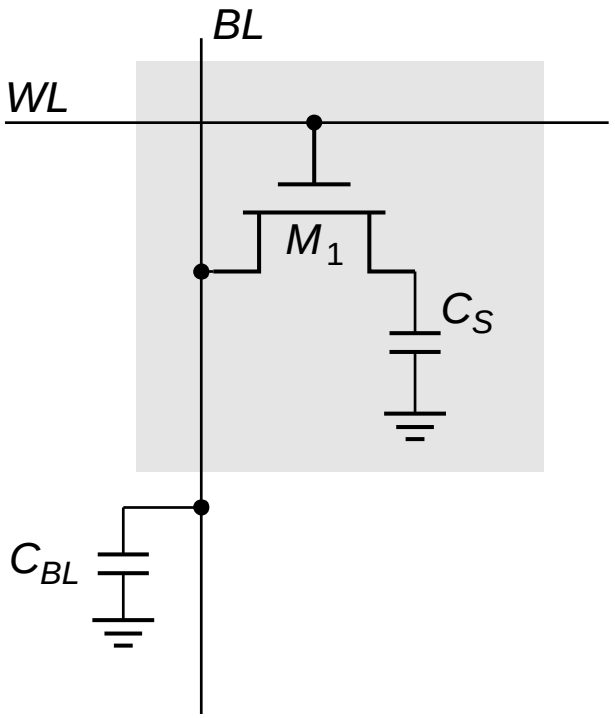
Reads are non-destructive

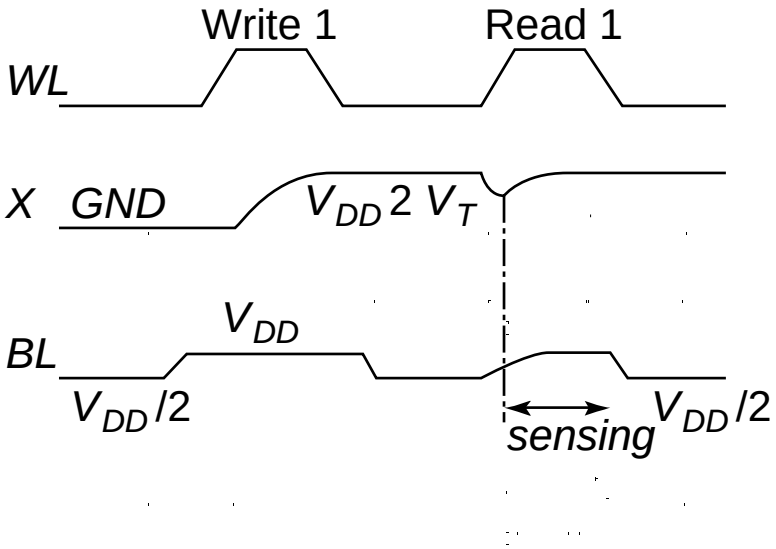
Value stored at node X when writing a “1” = V_{WWL}-V_{Tn}

3-Transistor DRAM Cell

- Precharge both the columns
- Assert the *write word line* (WWL)
- The data is retained as charge on capacitance C_S once WWL is lowered
- When reading the cell, the *read-word line (RWL)* is raised
- If “1” is stored then BL_2 will be discharged through M_3 and M_2
- If “0” is stored then there will be no conducting path,, so the precharged high level of BL_2 will not change significantly.

1-Transistor DRAM Cell





Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

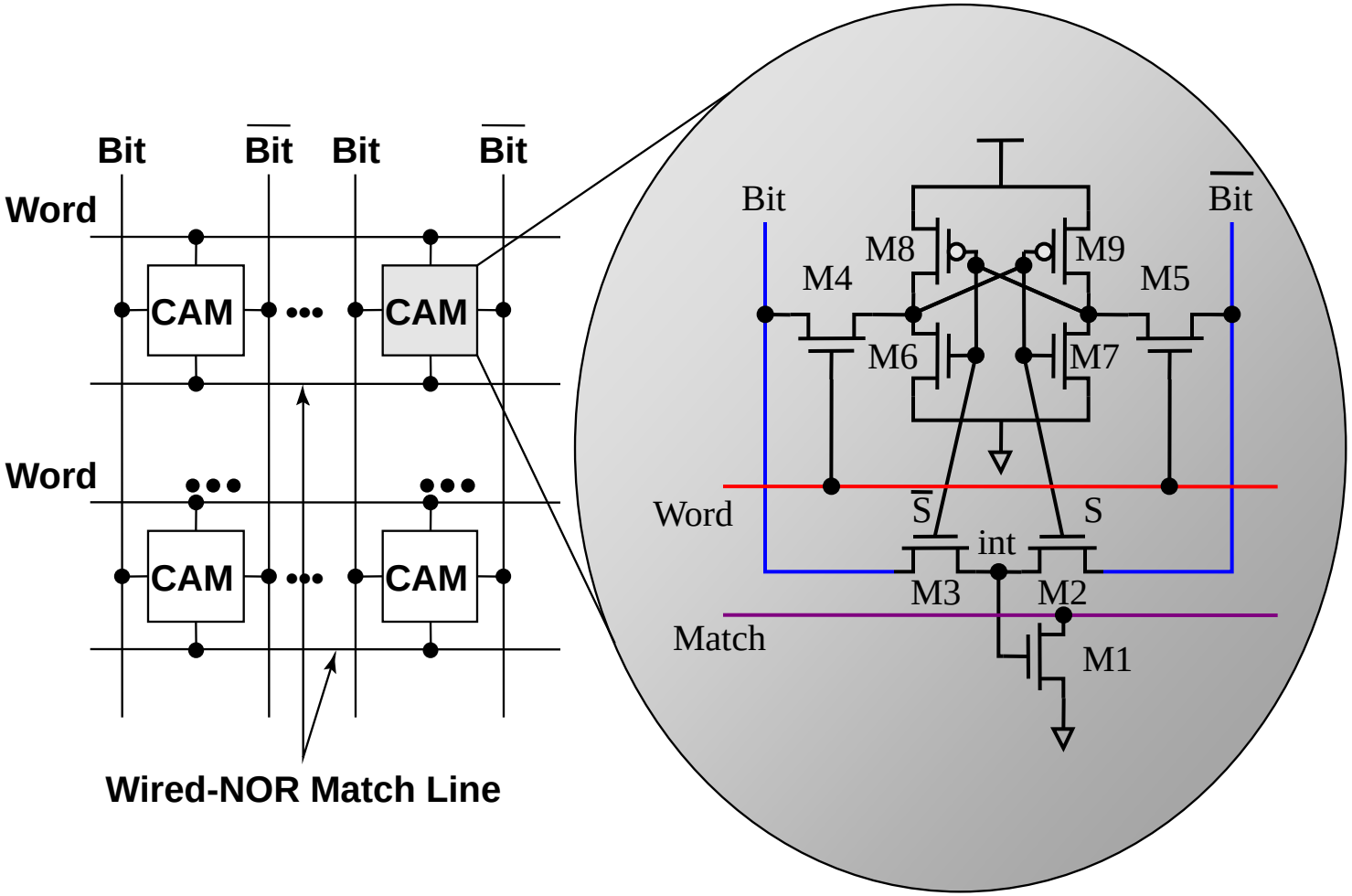
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

Content-Addressable Memories (CAMs)

- In SRAMs the access mechanism is based on known address.
- But there are applications where the data we seek is associated with a known binary keyword rather than a known binary address.
- The known keyword is compared against previously stored keywords, called tags, that reference the actual data we seek
- The tags are not stored in any particular order so we must match the address keyword with the tags that are already stored to access the desired data.

Static CAM Memory Cell



Principle

- The array contains n-bit stored tags that are to be compared with the incoming n-bit keyword.
- Each row holds a different tag
- Each bit of the tag is stored in a separate 6T SRAM cell.
- Match lines are pre charged high
- If there is a match, the match line remains high
- If the keyword and stored tag do not match, the NMOS device discharges the match line.

CAM in Cache Memory