

Homework Assignment 2

(Due 4:15pm, Sep. 12)

Submission: Email to daehyun@eecs.wsu.edu

(1) [**Static CMOS, 20 points**] Draw a transistor-level schematic for the following Boolean function (Available input: A, B, C). $F = \overline{A + B \cdot C}$. # TRs should be 6.

(2) [**SPICE, 20 points**] Use HSpice to simulate the design. Use 45nm for the transistor length, 150nm for the width of the NFETs, and 225nm for the width of the PFETs. Output load cap: 10fF. Create an input waveform and simulate it. Use the following bitstream for the input. ABC = (000) → (100) → (000) → (011) → (000) → (111) → (000). **Submit** a screenshot of the input and output waveforms.