Homework Assignment 3
(Due 4:15pm, Sep. 26)
Submission: Email to daehyun@eecs.wsu.edu

(1) **[Power, 20 points]** Download hw03.zip and unzip the file. Open inv.sp and see the measurement line at the end of the file. It measures the average power consumption from 0ns to 2ns. Run HSpice for the input file and see the log. You will see something like this:

******** transient analysis tnom= 25.000 temp= 25.000 ********

vavg_power= 5.1660e-06 from= 0.0000e+00 to= 2.0000e-09

This means that the average power consumption from time 0 to time 2ns is 5.166uW.

Notice that the actual switching occurs from 0.2ns to 0.5ns (falling) and from 1ns to 1.3ns (rising). Modify the SPICE input file to measure the two power values separately. **Submit**: The average power consumption values for the falling and rising. Estimate the total capacitance of the two transistors.

(2) [**Power, 20 points**] Increase the width of the NFET and PFET as follows. NFET: 50nm → 200nm, PFET: 75nm → 300nm. Simulate it again.

Submit: The average power consumption values for the falling and rising. Add a short statement about why the power consumption goes up (compared to the first part).

(3) **[Power, 20 points]** Create a two-input NAND gate. Set the lengths of the transistors to 45nm. Set the widths of the NFETs to 150nm. Set the widths of the PFETs to 225nm.

Submit: Estimate the total capacitance of the four transistors. The average power consumption values for the falling and rising obtained from HSpice.