Homework Assignment 4
(Due 4:15pm, Nov. 7)
Submission: Email to daehyun@eecs.wsu.edu

(1) **[Domino Logic, 50 points]** Design the following function using a domino logic. Clock frequency: 3GHz (clock duty cycle: 50%).

$$\boldsymbol{F = \{x_0 \cdot (x_1 + x_2) + x_3 \cdot x_4 \cdot x_5\} \cdot x_6 \cdot (x_7 + x_8 + x_9) \cdot x_{10} \cdot (x_{11} + x_{12} + x_{13} + x_{14} + x_{15}) \cdot (x_{16} + x_{17} \cdot x_{18})}$$

If you cannot satisfy the target clock frequency, try to minimize the negative slack.