EE 466/586
VLSI Design

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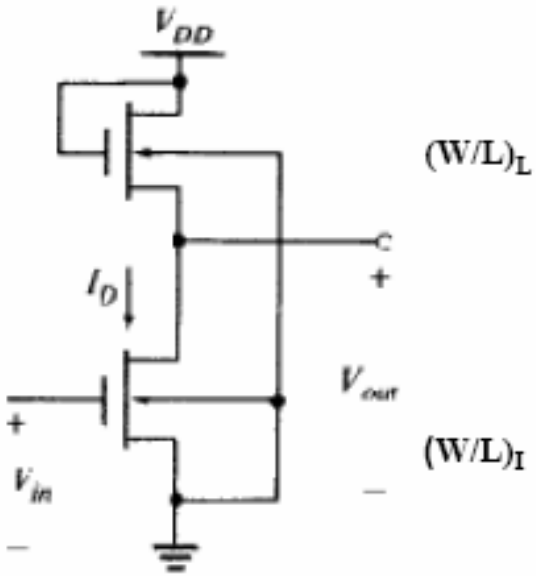
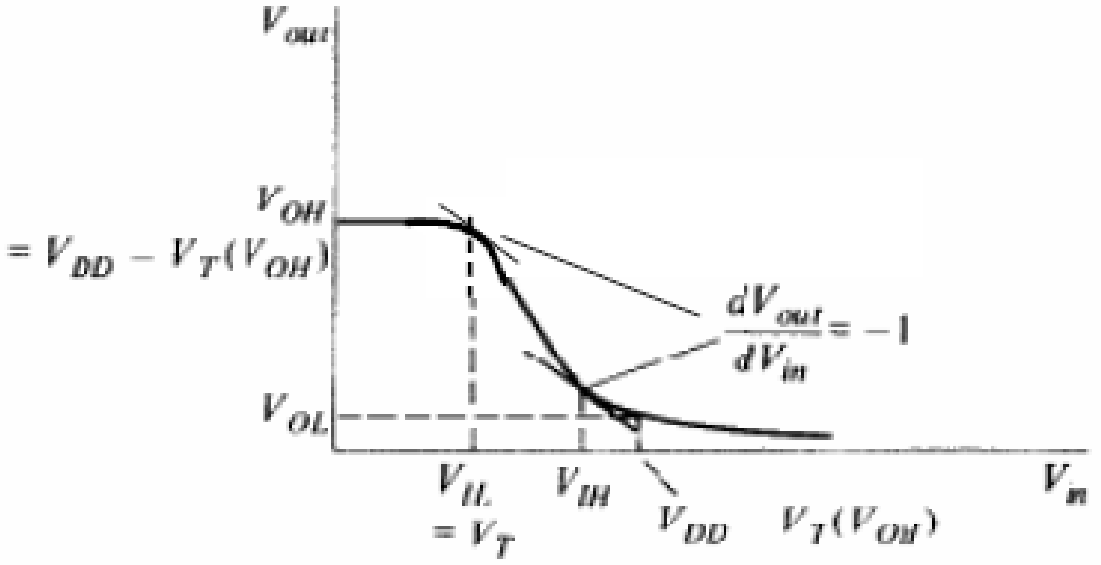
Lecture 5

MOS Inverter Circuits

Saturated Enhancement Load

- A single NMOS transistor with the gate connected to the drain can be used as a load device.





Saturated Enhancement Load (Cont'd)

- The load transistor can operate only in saturation or cutoff ($V_{GS} = V_{DS}$)
- The other NMOS device pulls down the output node
- The relative sizes of the two transistors determine the output voltage

Saturated Enhancement Load (cont'd)

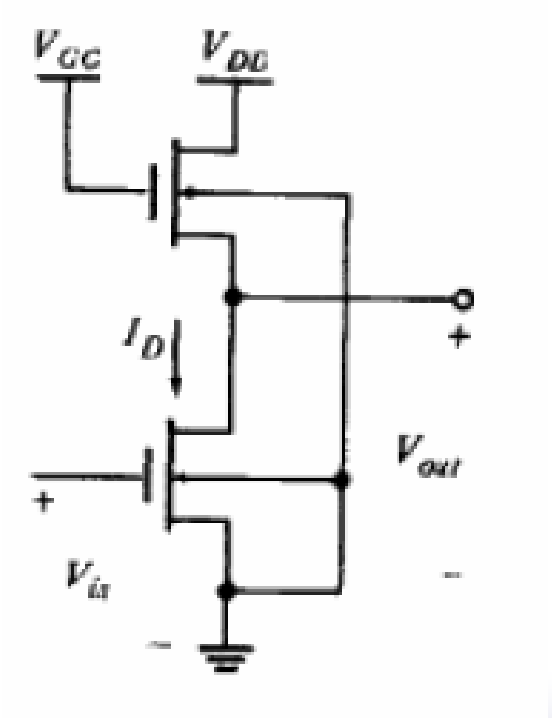
- The output high level V_{OH} is not equal to V_{DD}
- The pull-up transistor ceases to conduct after its gate-source voltage decreases to the threshold voltage.
  - The output node never rises above V_{DD}-V_{TL}
  - V_{TL} is no longer V_{T0}
  - Output voltage appears as a body bias
  - Follow board notes

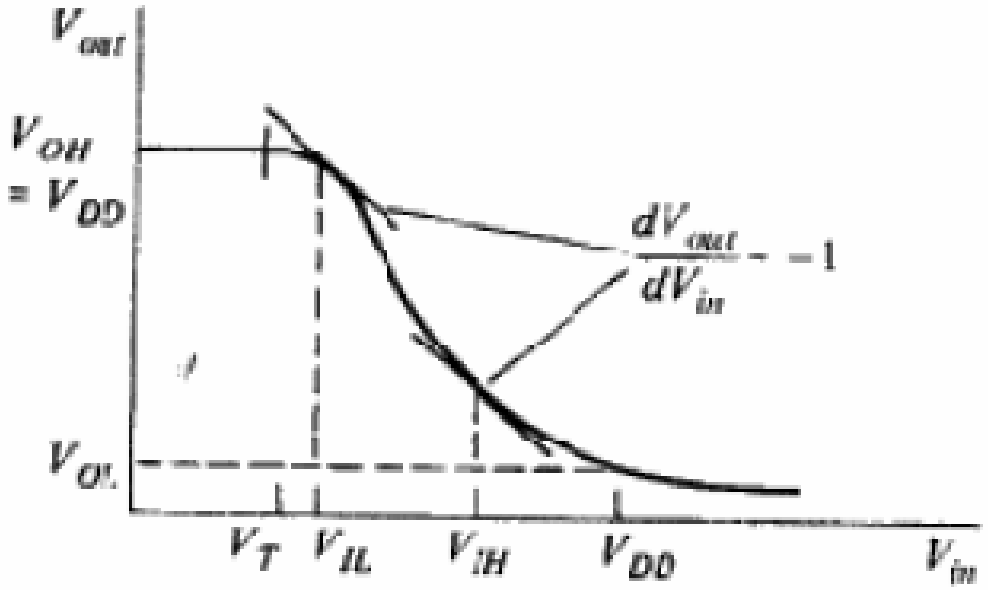
Saturated Enhancement Load (Cont'd)

- How to find V_{OL}?
- For the inverting transistor, with $V_{GS}=V_{OH}$ the output voltage should be lower than V_{T0}
- Pull down transistor is in the linear region $V_{DS}<V_{GS} - V_{TI}$
- $I_{DI}(lin)= I_{DL}(Sat)$
- Follow board notes

Linear Enhancement load

- The output high level of the saturated enhancement load configuration is not sufficient





Linear Enhancement Load (Cont'd)

- The load device can pull the output all the way to V_{DD}
- For the pull up device $V_{DS}<V_{GS}-V_{TL}$
- The pull-up device, operates in the linear region