EE 466/586
VLSI Design

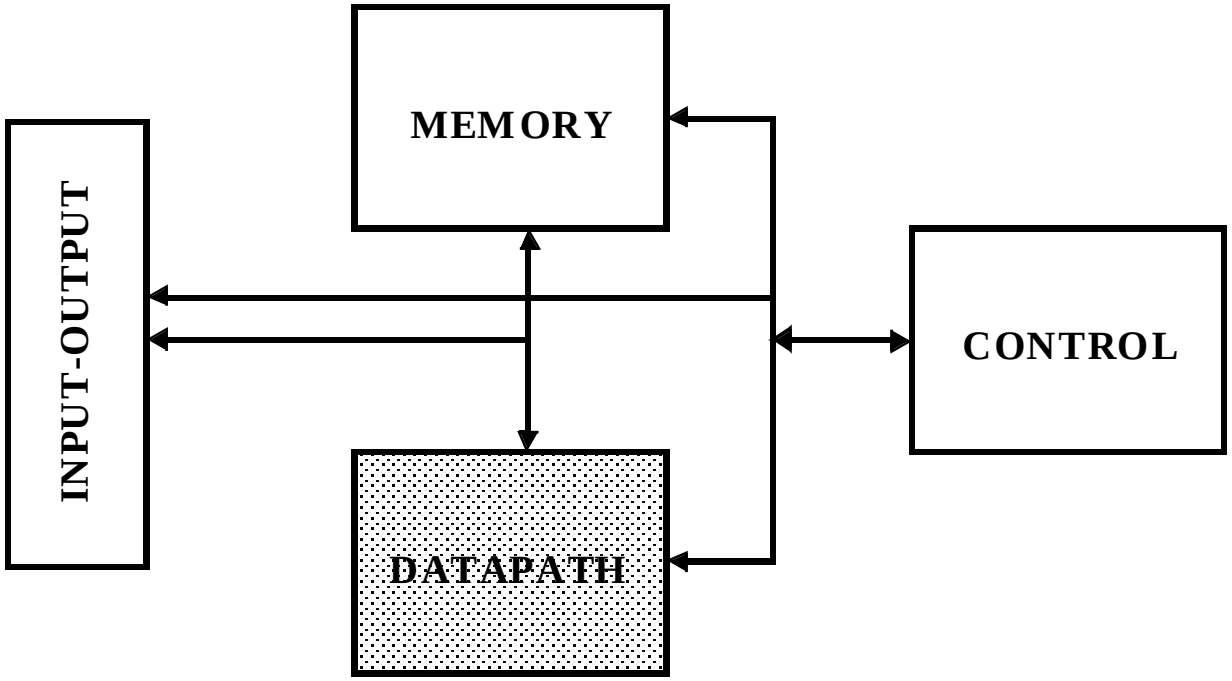
Partha Pande
School of EECS
Washington State University
pande@eecs.wsu.edu

Lecture 21

Arithmetic circuits

Adopted from Digital Integrated Circuits by Jan M Rabaey

A Generic Digital Processor



Building Blocks for Digital Architectures

Arithmetic unit

- Bit-sliced datapath (adder, multiplier, shifter, comparator, etc.)

Memory

- RAM, ROM, Buffers, Shift registers

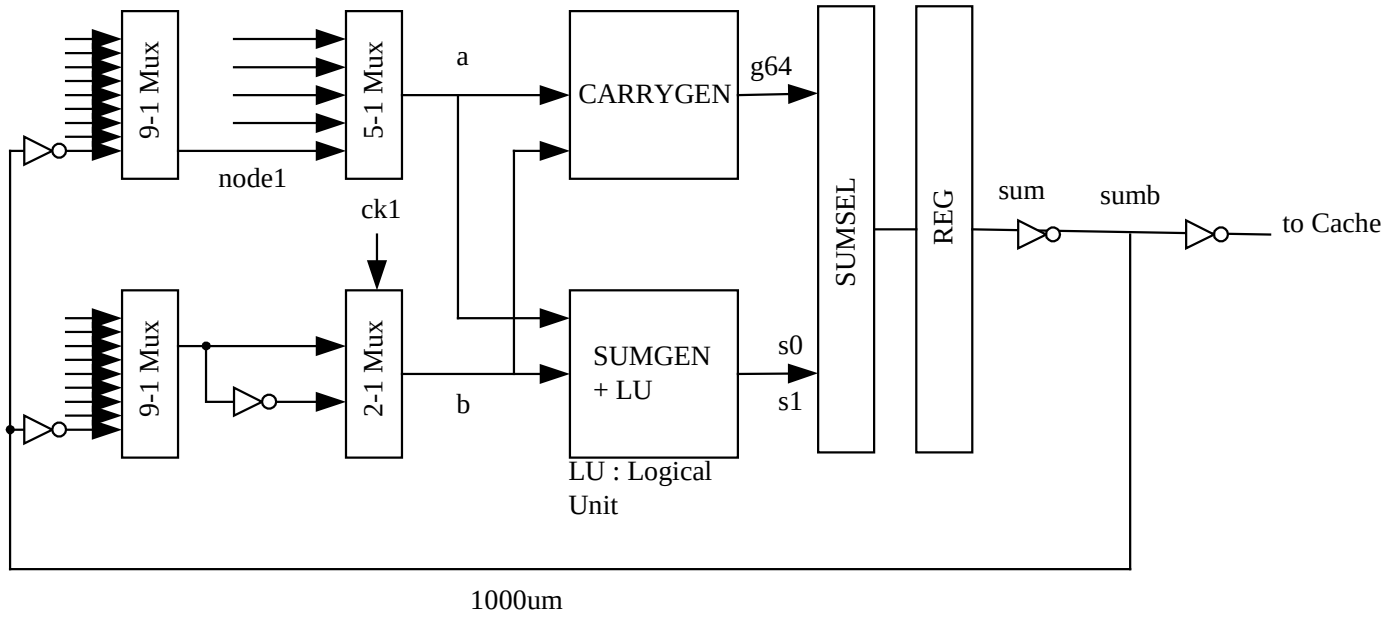
Control

- Finite state machine (PLA, random logic.)
- Counters

Interconnect

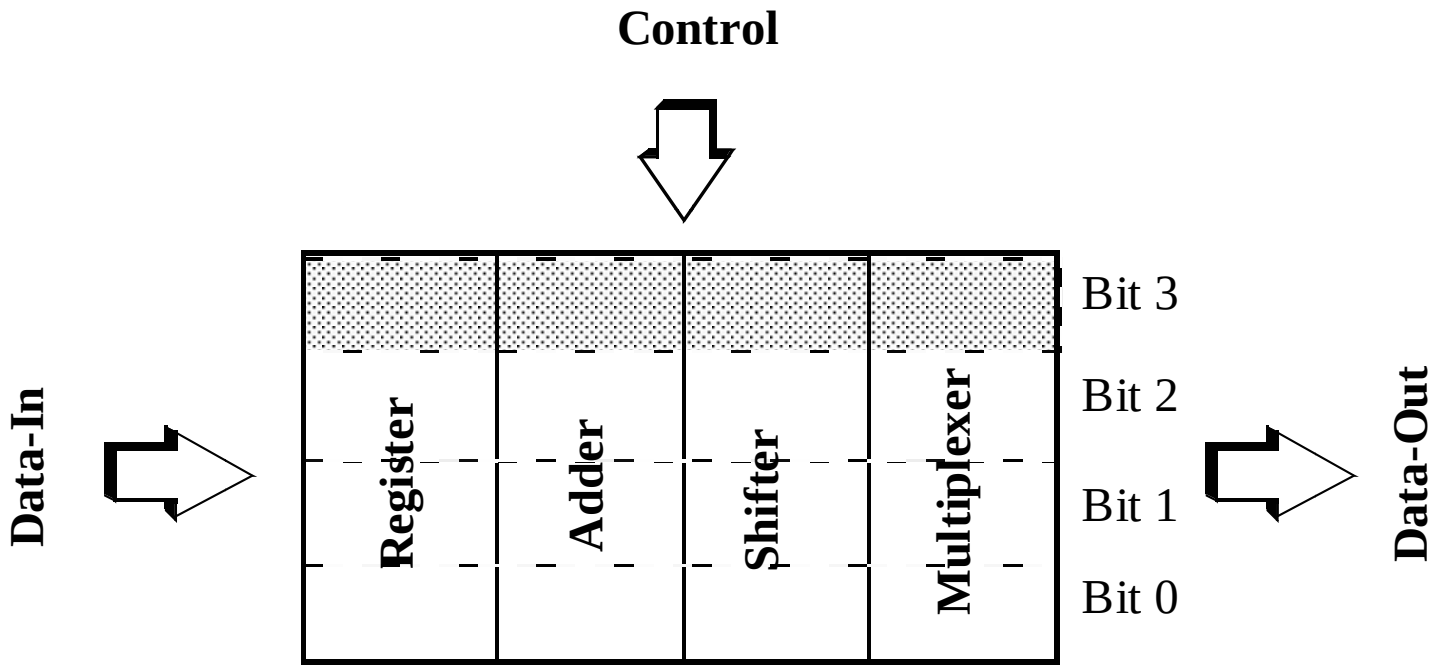
- Switches
- Arbiters
- Bus

An Intel Microprocessor



Itanium has 6 integer execution units like this

Bit-Sliced Design



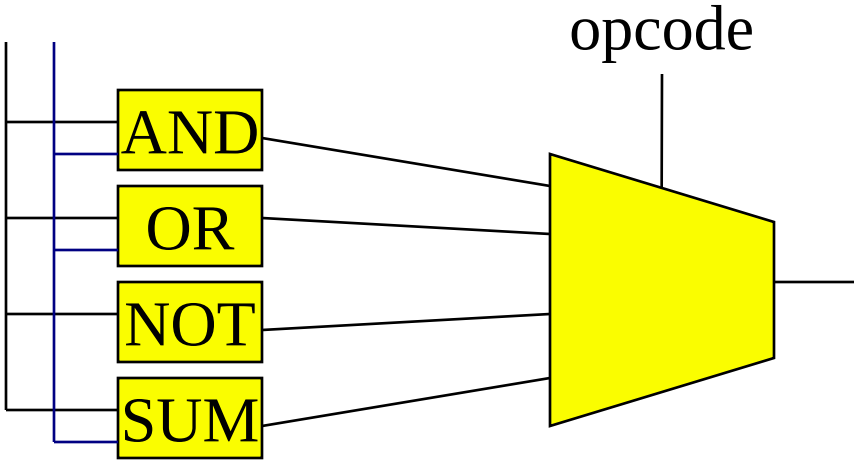
Tile identical processing elements

ALU

- ALU computes a variety of logical and arithmetic functions based on **opcode**.
- May offer complete set of functions of two variables or a subset.
- ALU built around adder, since carry chain determines delay.

ALU as multiplexer

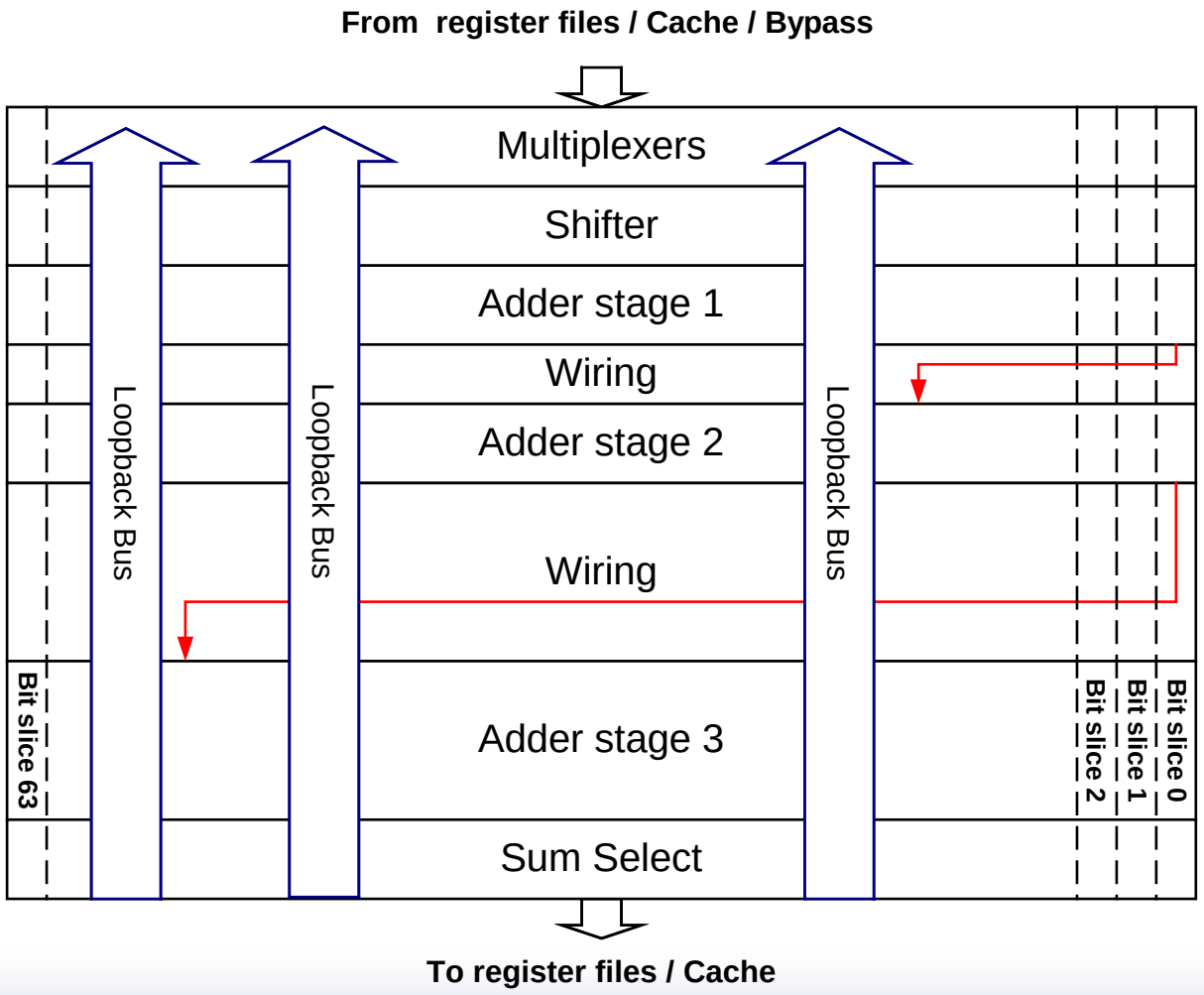
- Compute functions then select desired one:



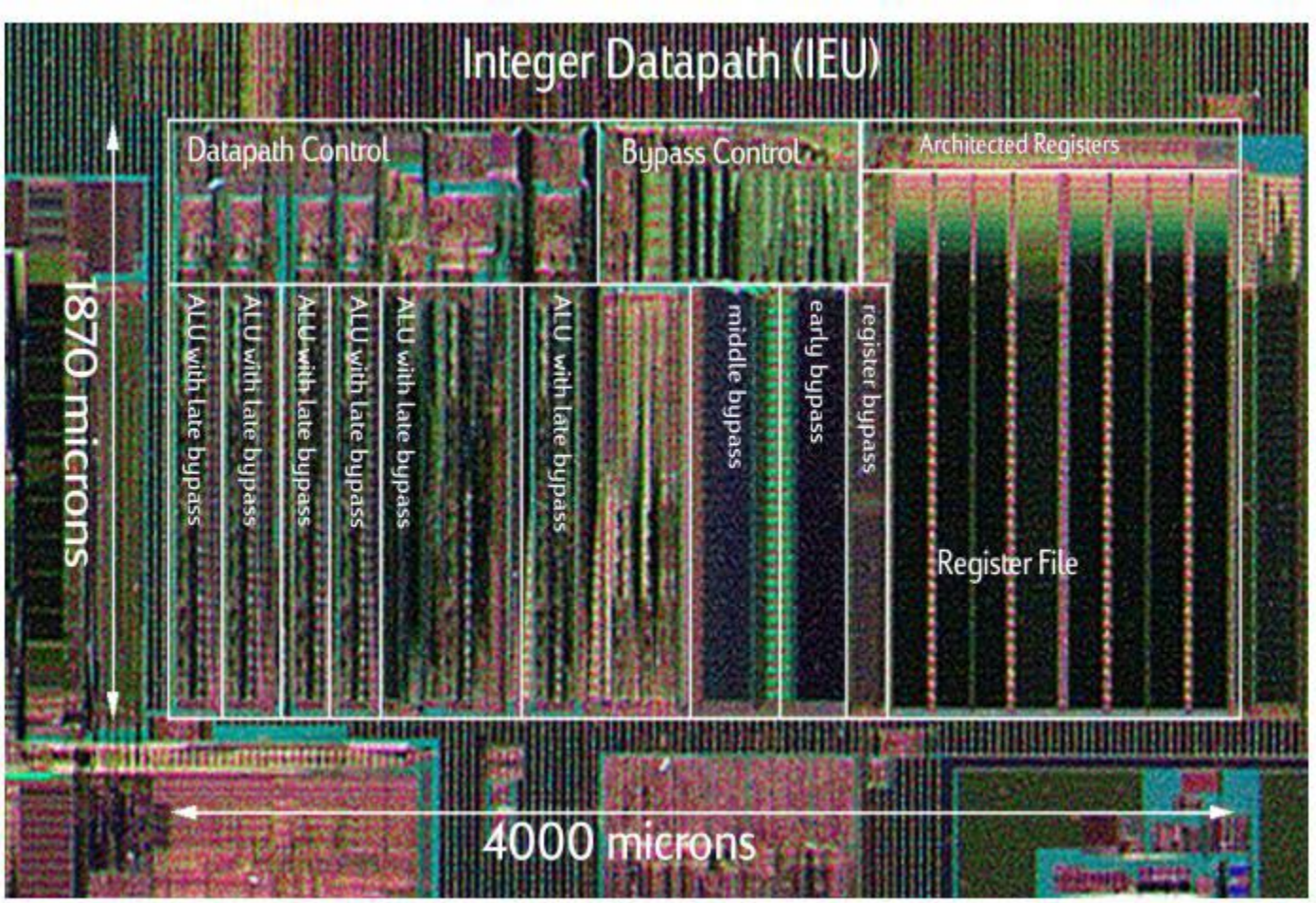
Verilog for ALU

```
‘define PLUS 0
‘define MINUS 1
‘define AND 2
‘define OR 3
‘define NOT 4

module alu(fcode,op0,op1,result,oflo);
      parameter n=16, flen=3; input [flen-1:0] fcode; [n-1:0] op0, op1; output [n-1:0] result; output
      oflo;

assign
      {oflo,result} =
            (fcode == ‘PLUS) ? (op0 + op1) :
              (fcode == ‘MINUS) ? (op0 - op1) :
                (fcode == ‘AND) ? (op0 & op1) :
                        (fcode == ‘OR) ? (op0 | op1) :
                          (fcode == ‘NOT) ? (~op0) : 0;
endmodule
```

Bit-Sliced Datapath

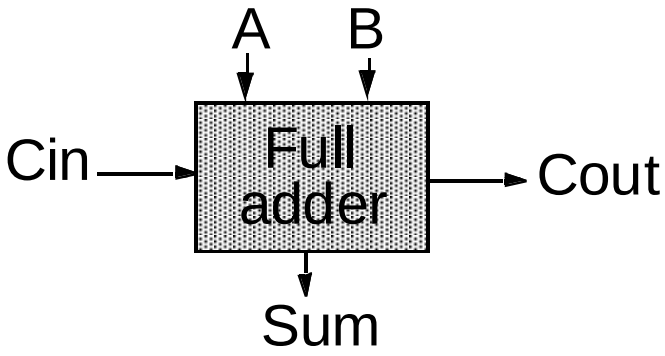


Itanium Integer Datapath



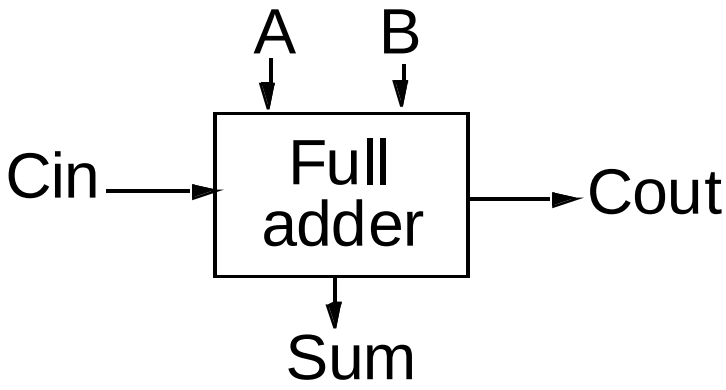
Fetzer, Orton, ISSCC'02

Full-Adder



A	B	C_i	S	C_o	*Carry status*
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

The Binary Adder



$$S = A \oplus B \oplus C_i$$

$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$

$$C_o = AB + BC_i + AC_i$$

Express Sum and Carry as a function of P, G, D

Define 3 new variable which ONLY depend on A, B

Generate (G) = AB

Propagate (P) = A ⊕ B

Delete = $\overline{A}\,\overline{B}$

$$C_o(G,P) = G + PC_i$$

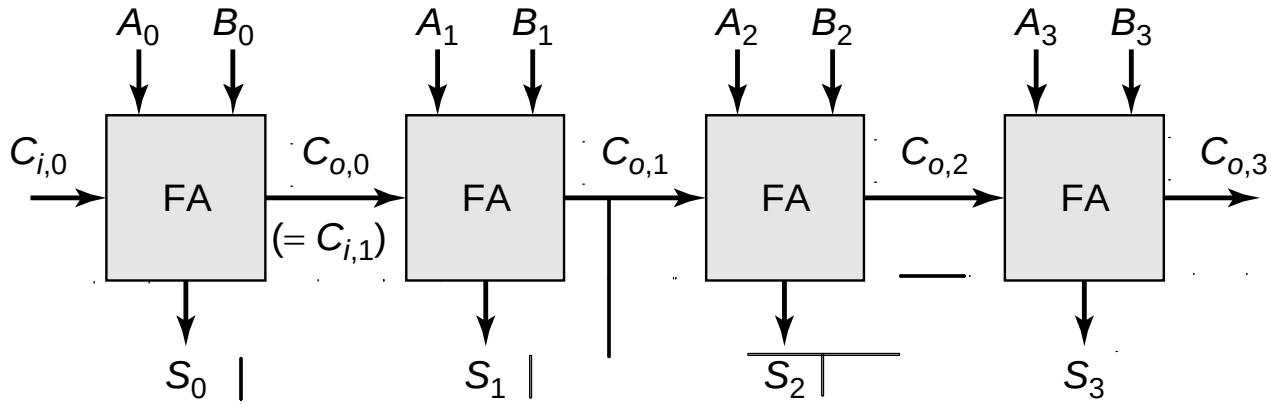
$$S(G,P) = P \oplus C_i$$

Can also derive expressions for *S* and C_o based on *D* and *P*

Note that we will be sometimes using an alternate definition for

Propagate (P) = A + B

The Ripple-Carry Adder



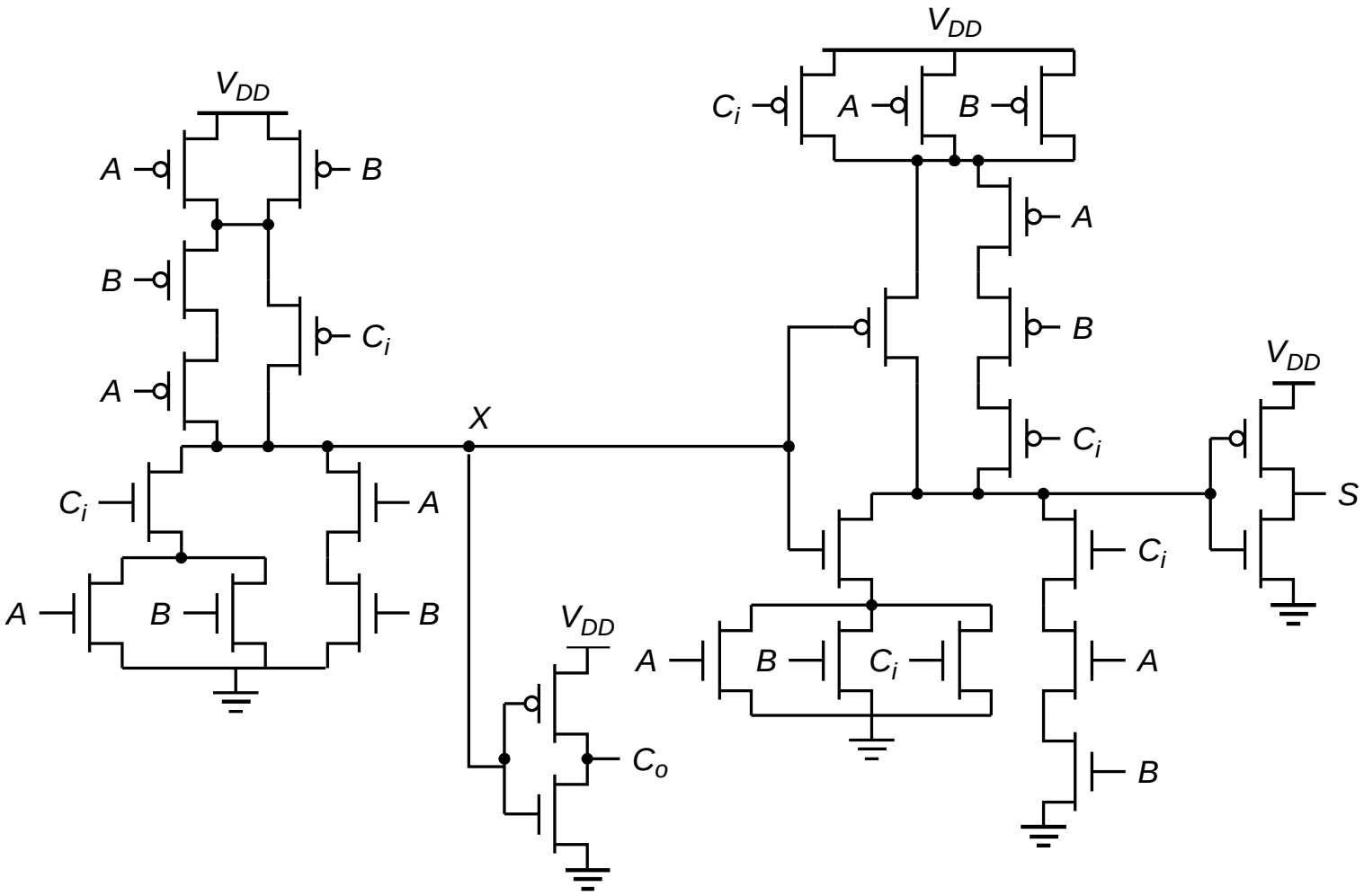
Worst case delay linear with the number of bits

$$t_d = O(N)$$

$$t_{adder} = (N\text{-}1)t_{carry} + t_{sum}$$

Goal: Make the fastest possible carry path circuit

Complimentary Static CMOS Full Adder



28 Transistors

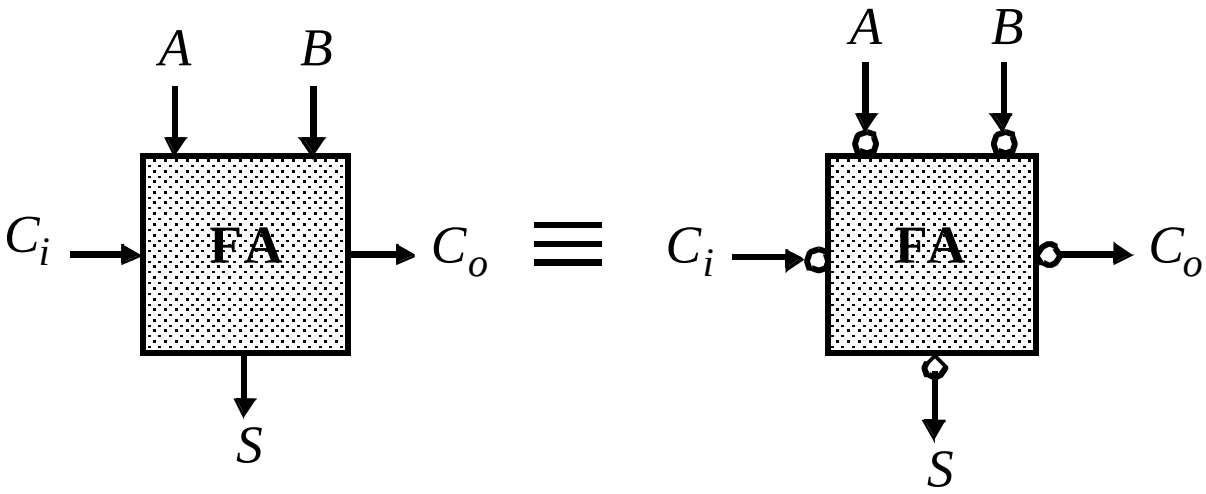
Limitations

- *Tall PMOS transistor stacks present in both carry- and sum-generation circuits.*
- *The intrinsic load capacitance of the C_0 signal is large and consists of two diffusion and six gate capacitances, plus the wiring capacitance*
- *The signal propagates through two inverting stages in the carry-generation circuit.*

Features

- The first gate of the carry-generation circuit is designed with the C_i signal on the smaller PMOS stack
- NMOS and PMOS transistors connected to C_i are placed as close as possible to the output of the gate.
  - In stage k of the adder, signals A_k and B_k are available and stable long before $C_{i,k}$
  - Capacitances of the internal nodes is the transistor chain are precharged or discharged in advance.

Inversion Property

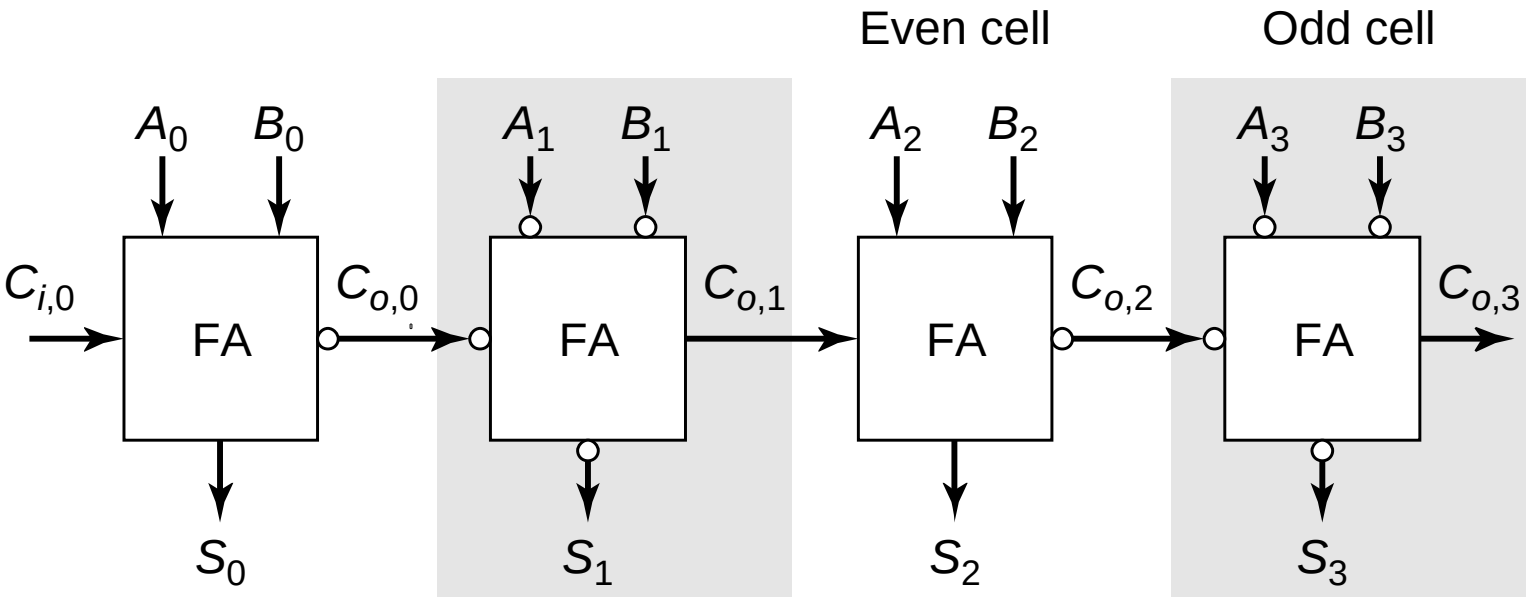


$$\bar{S}(A, B, C_i) = S(\bar{A}, \bar{B}, \overline{C_i})$$

$$\overline{C_o}(A, B, C_i) = C_o(\bar{A}, \bar{B}, \overline{C_i})$$

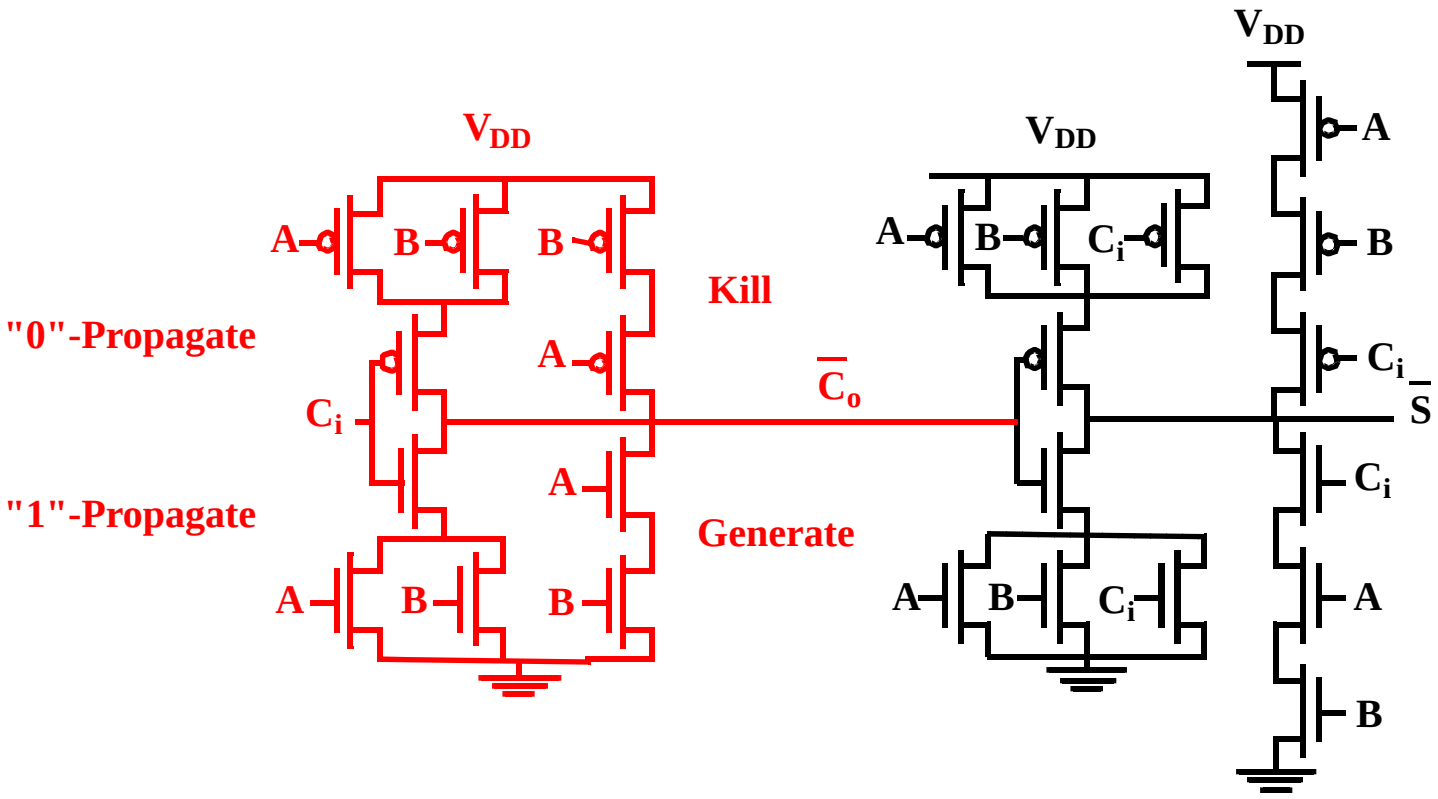
❖ *Inverting all inputs to a full adder results in inverted values for all outputs.*

Minimize Critical Path by Reducing Inverting Stages



Exploit Inversion Property

A Better Structure: The Mirror Adder

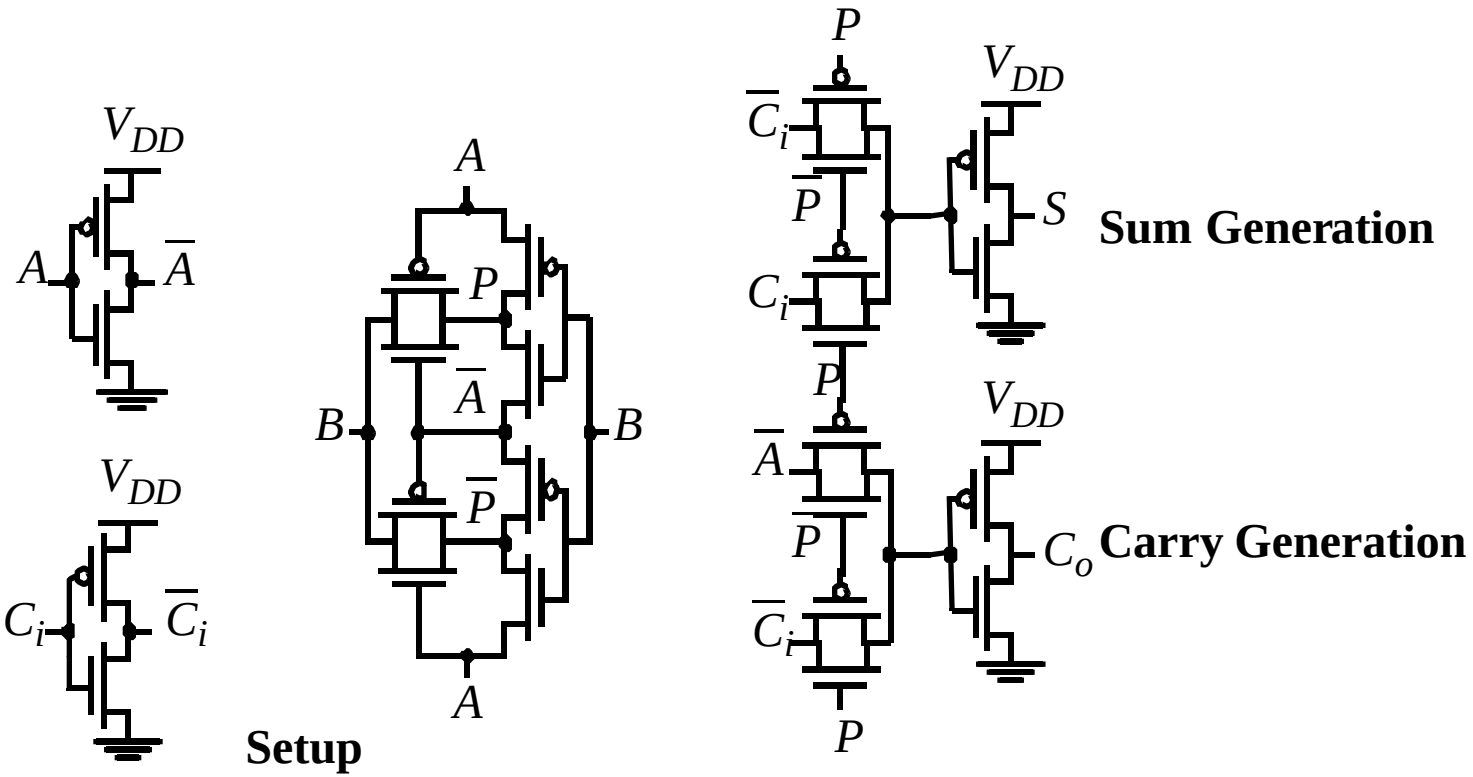


24 transistors

The Mirror Adder

- **The NMOS and PMOS chains are completely symmetrical.**
  A maximum of two series transistors can be observed in the carry-generation circuitry.
- **When laying out the cell, the most critical issue is the minimization of the capacitance at node C_o. The reduction of the diffusion capacitances is particularly important.**
- **The capacitance at node C_o is composed of four diffusion capacitances, two internal gate capacitances, and six gate capacitances in the connecting adder cell .**
- **The transistors connected to C_i are placed closest to the output.**
- **Only the transistors in the carry stage have to be optimized for optimal speed. All transistors in the sum stage can be minimal size.**

Transmission Gate Full Adder



The propagate signal, which is the XOR of inputs A and B, is used to select the true or complementary value of the input carry as the new sum output

Based on the propagate signal, the output carry is either set to the input carry, or either one of the inputs A or B.