EE 466/586
VLSI Design

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Lecture 23
Arithmetic circuits (Cont'd)

The Binary Multiplication

$$Z = X \times Y = \sum_{k=0}^{M+N-1} Z_k 2^k$$

$$= \left(\sum_{i=0}^{M-1} X_i 2^i \right) \left(\sum_{j=0}^{N-1} Y_j 2^j \right)$$

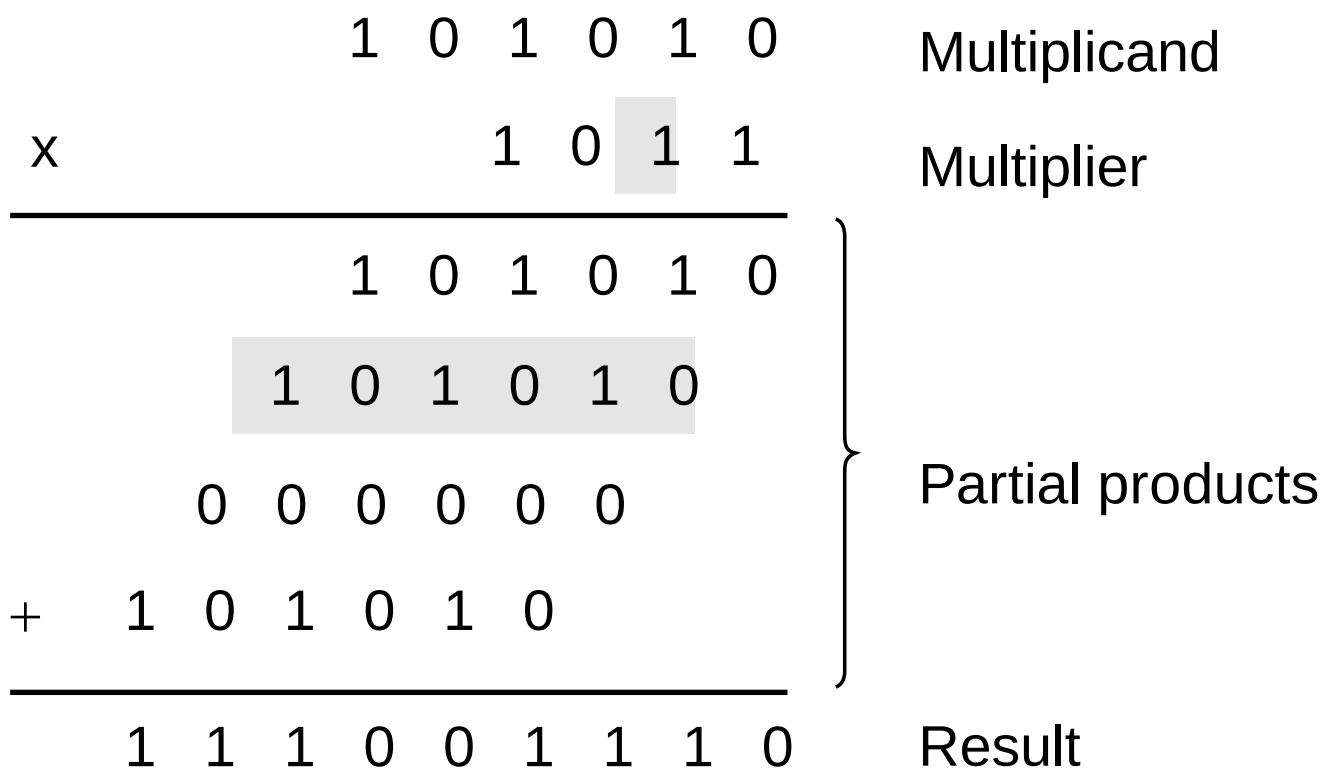
$$= \sum_{i=0}^{M-1} \left(\sum_{j=0}^{N-1} X_i Y_j 2^{i+j} \right)$$

with

$$X = \sum_{i=0}^{M-1} X_i 2^i$$

$$Y = \sum_{j=0}^{N-1} Y_j 2^j$$

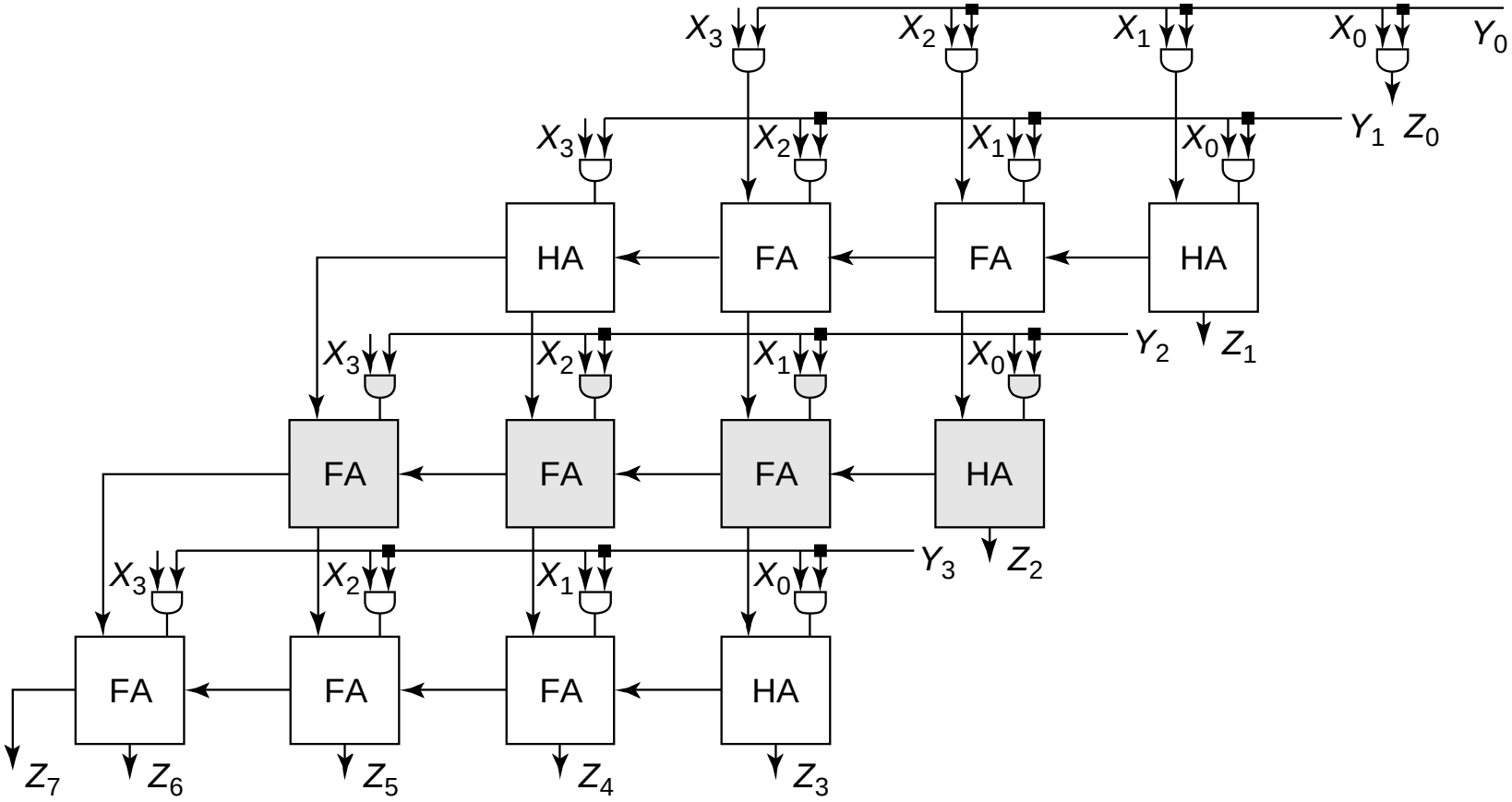
The Binary Multiplication



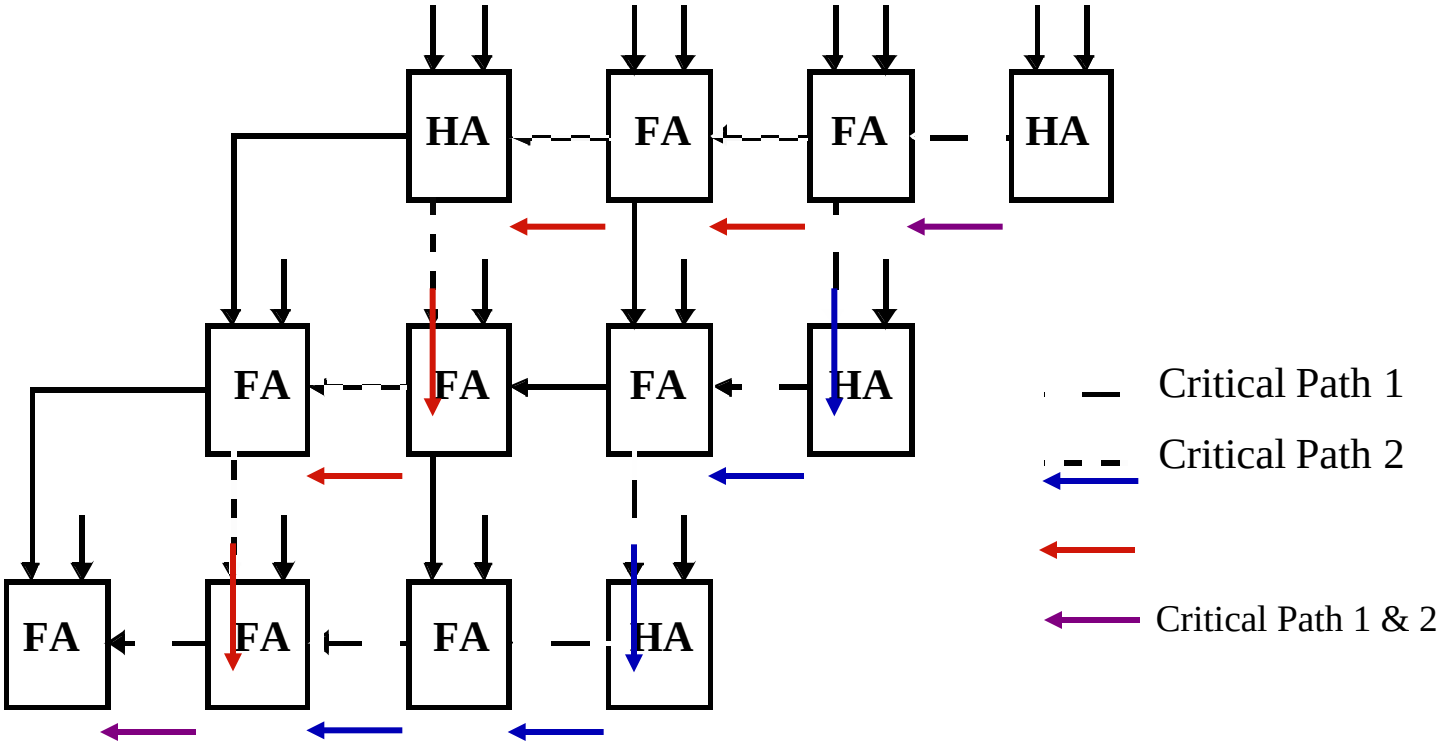
Partial-Product Generation

- Partial products result from the logical AND of multiplicand X with a multiplier bit Y_i
- Each row in the partial-product array is either a copy of the multiplicand or a row of zeros.
- Partial-product array has many zero rows that have no impact on the result.

The Array Multiplier



The MxN Array Multiplier — Critical Path

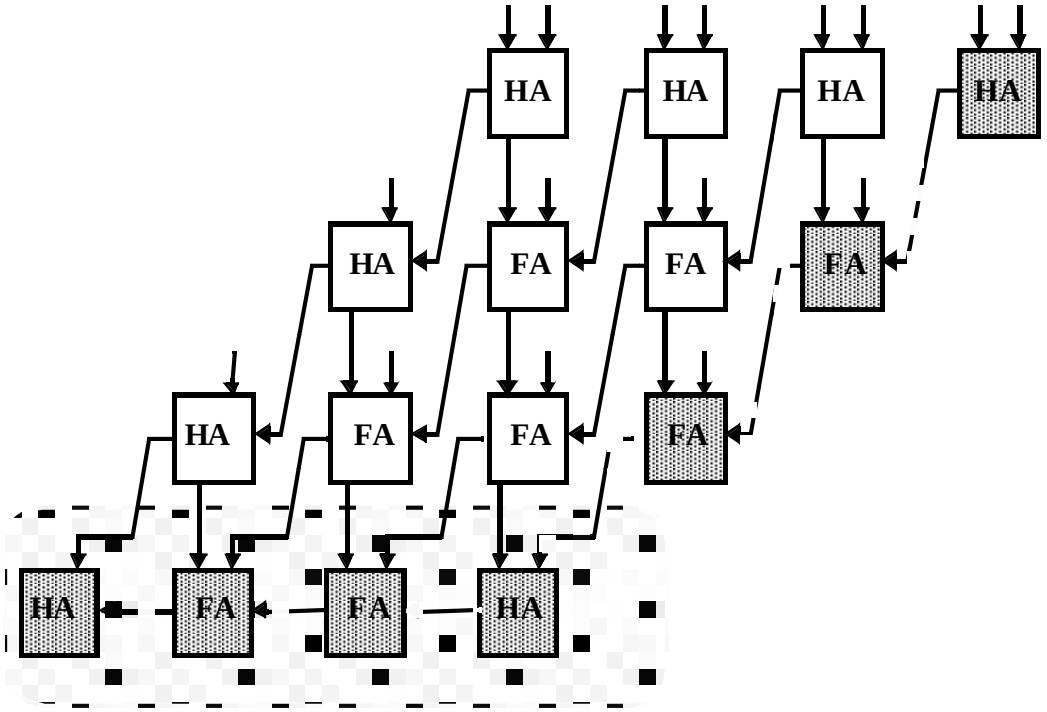


$$t_{mult} \approx [(M-1)+(N-2)]t_{carry} + (N-1)t_{sum} + (N-1)t_{and}$$

Carry-Save Multiplier

- Multiplication result does not change when the output carry bits are passed diagonally downwards instead of only to the right.
- Include an extra adder called a vector-merging adder to generate the final results

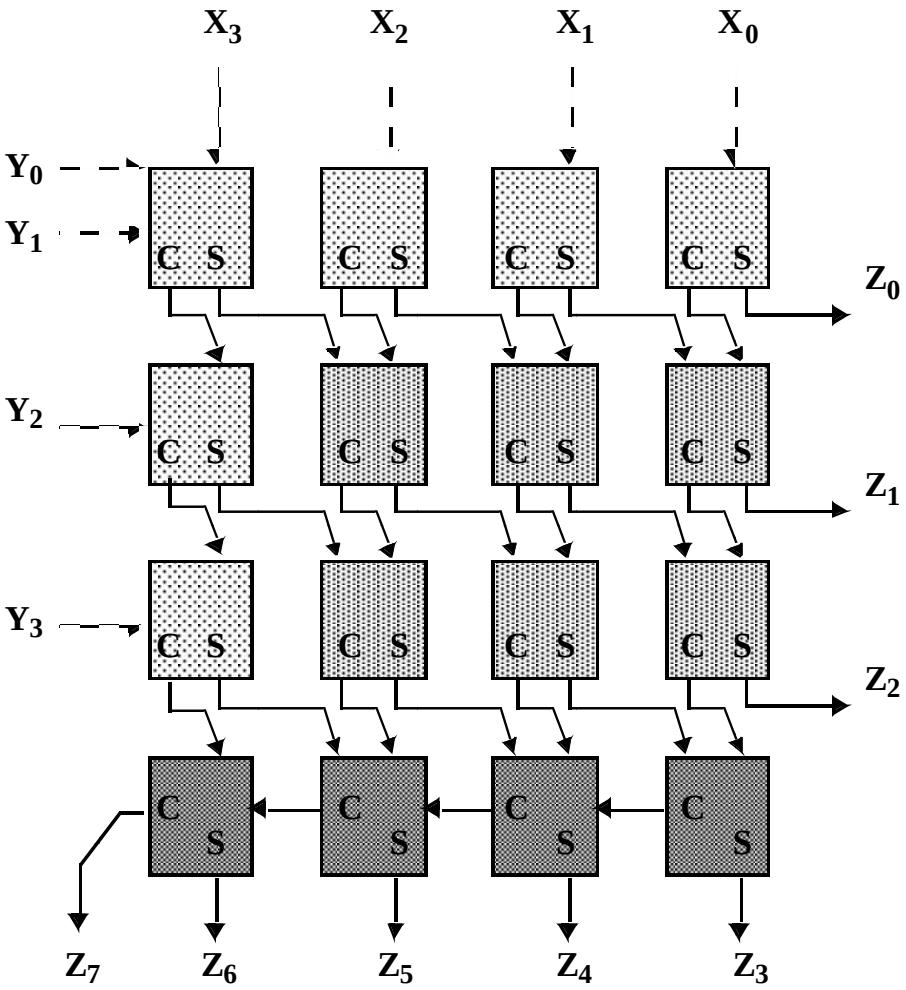
Carry-Save Multiplier



Vector Merging Adder

$$t_{mult} = (N-1)t_{carry} + (N-1)t_{and} + t_{merge}]$$

Multiplier Floorplan



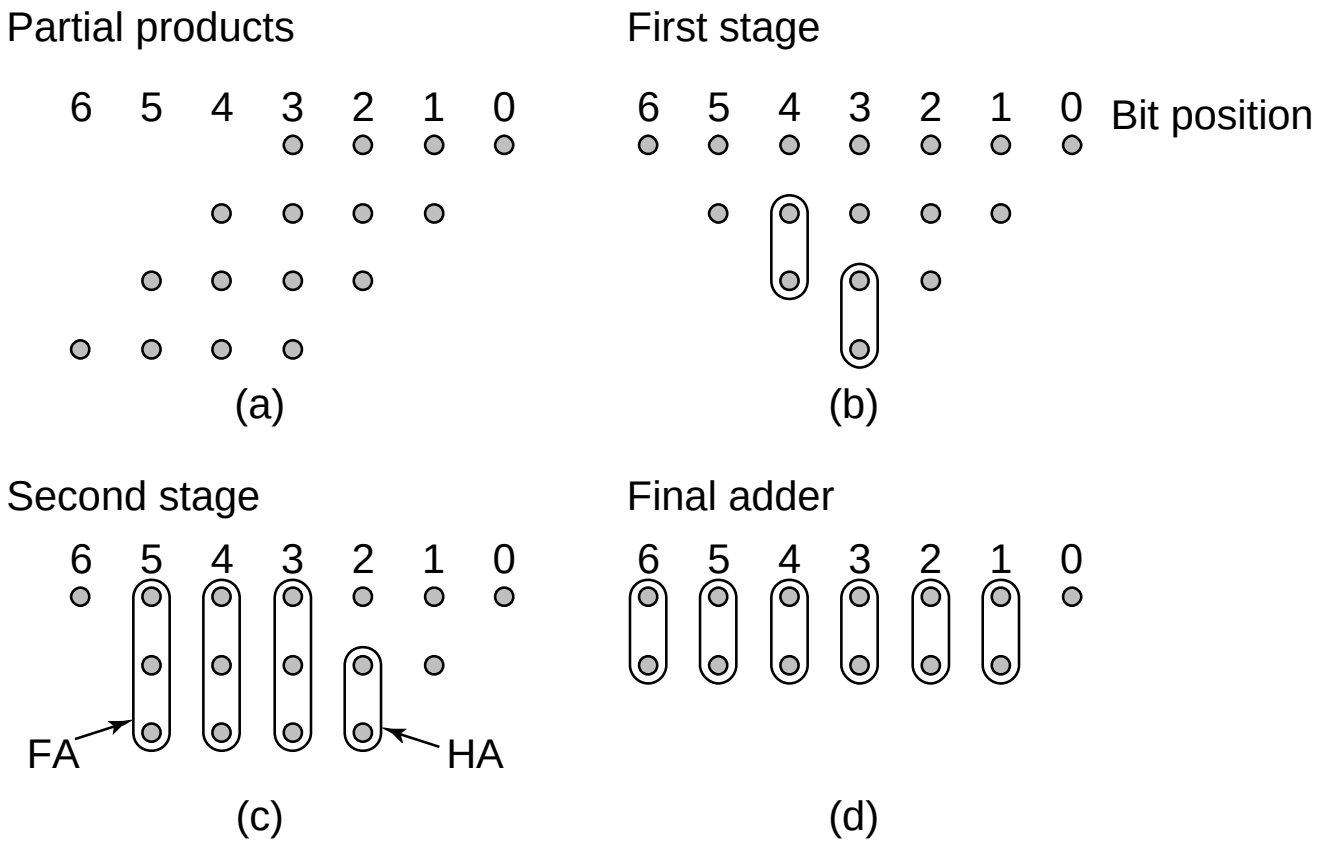
HA Multiplier Cell

FA Multiplier Cell

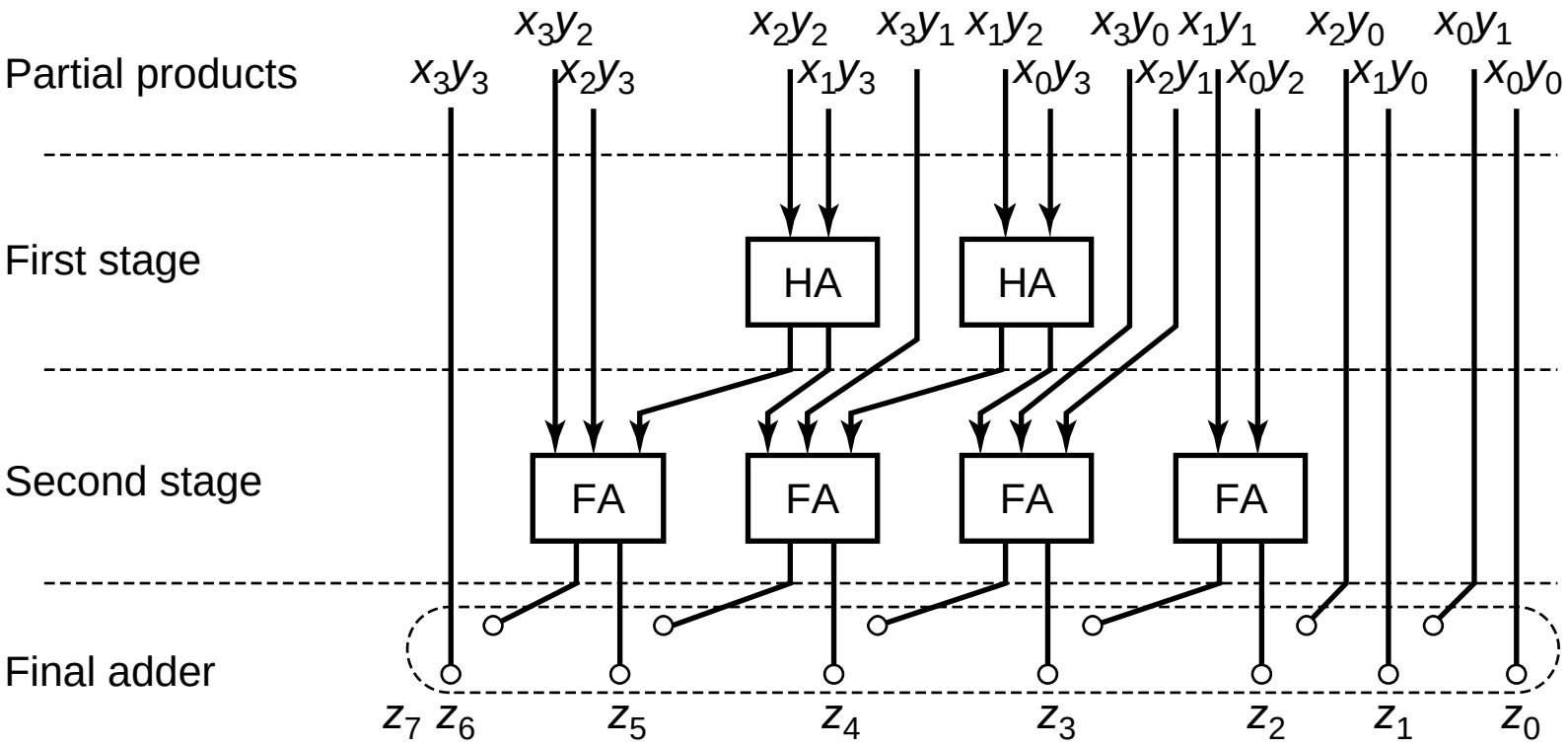
Vector Merging Cell

X and Y signals are broadcasted through the complete array. (– ▸)

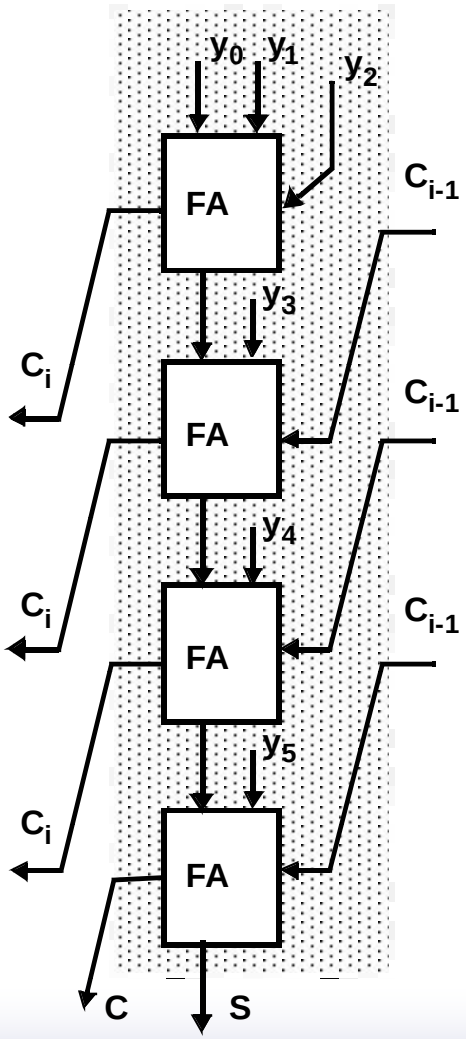
Wallace-Tree Multiplier

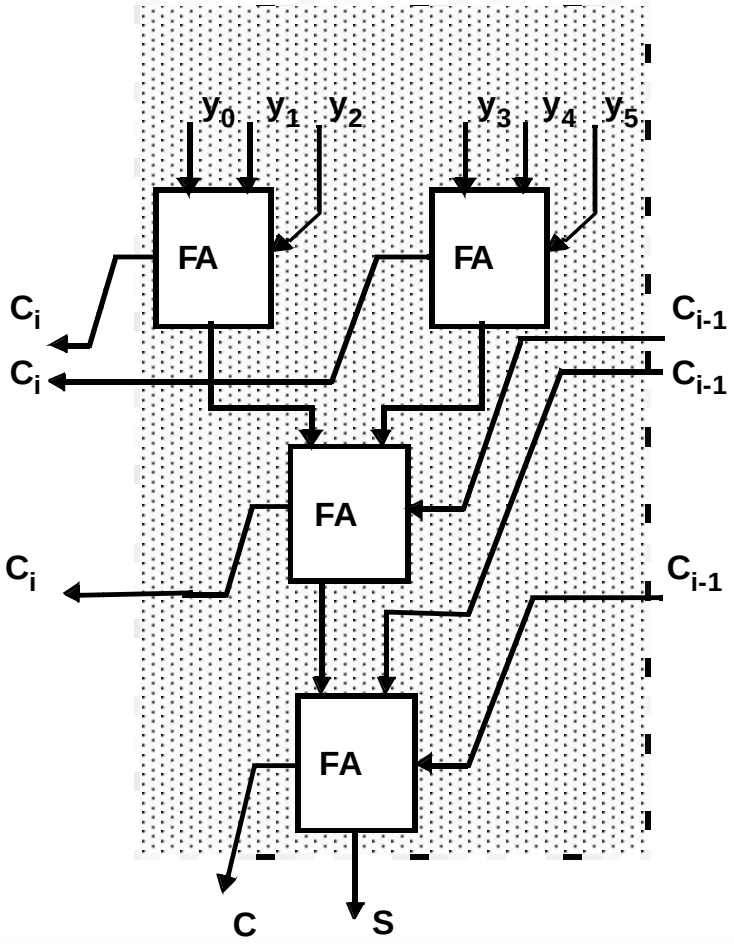


Wallace-Tree Multiplier

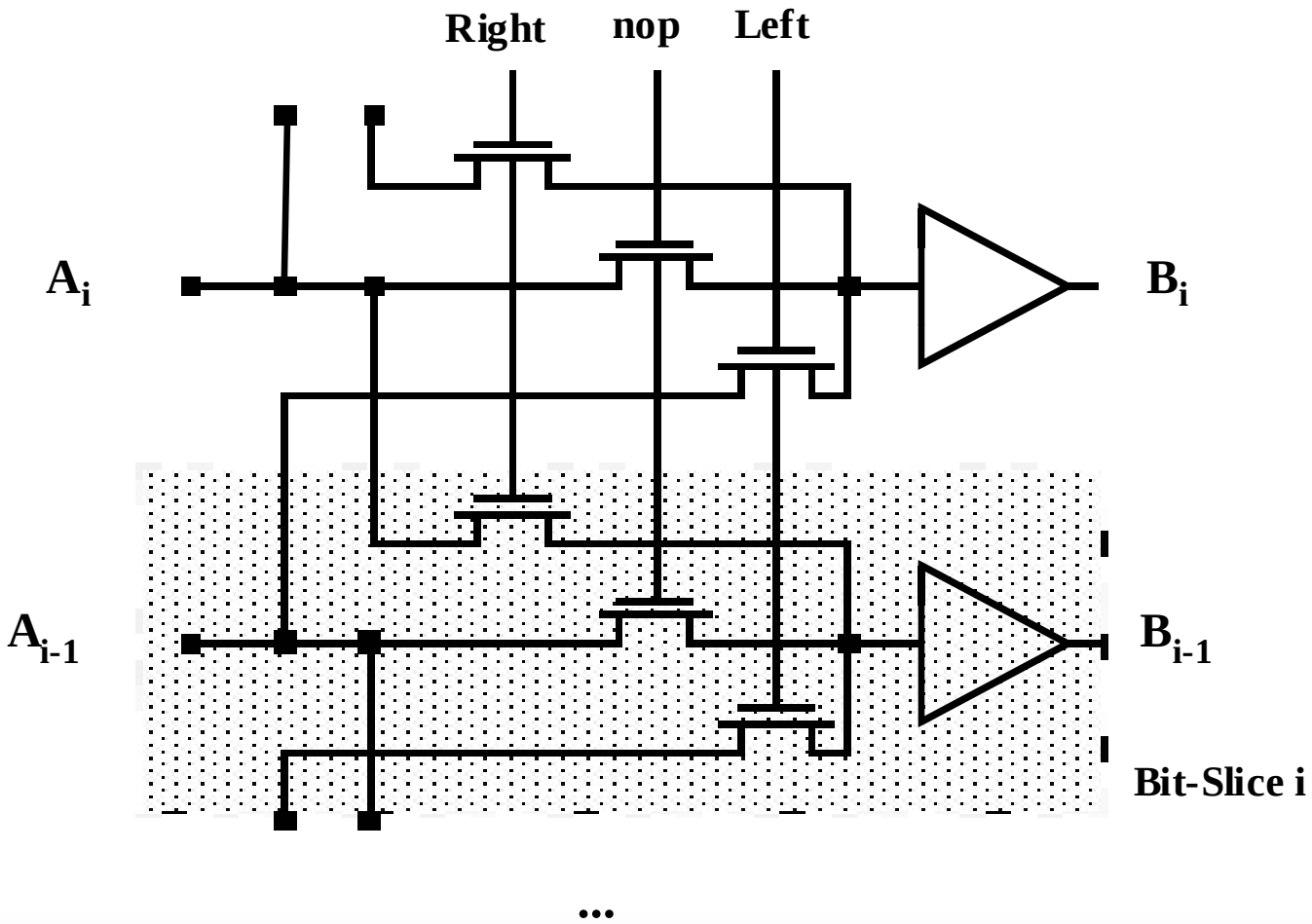


Wallace-Tree Multiplier

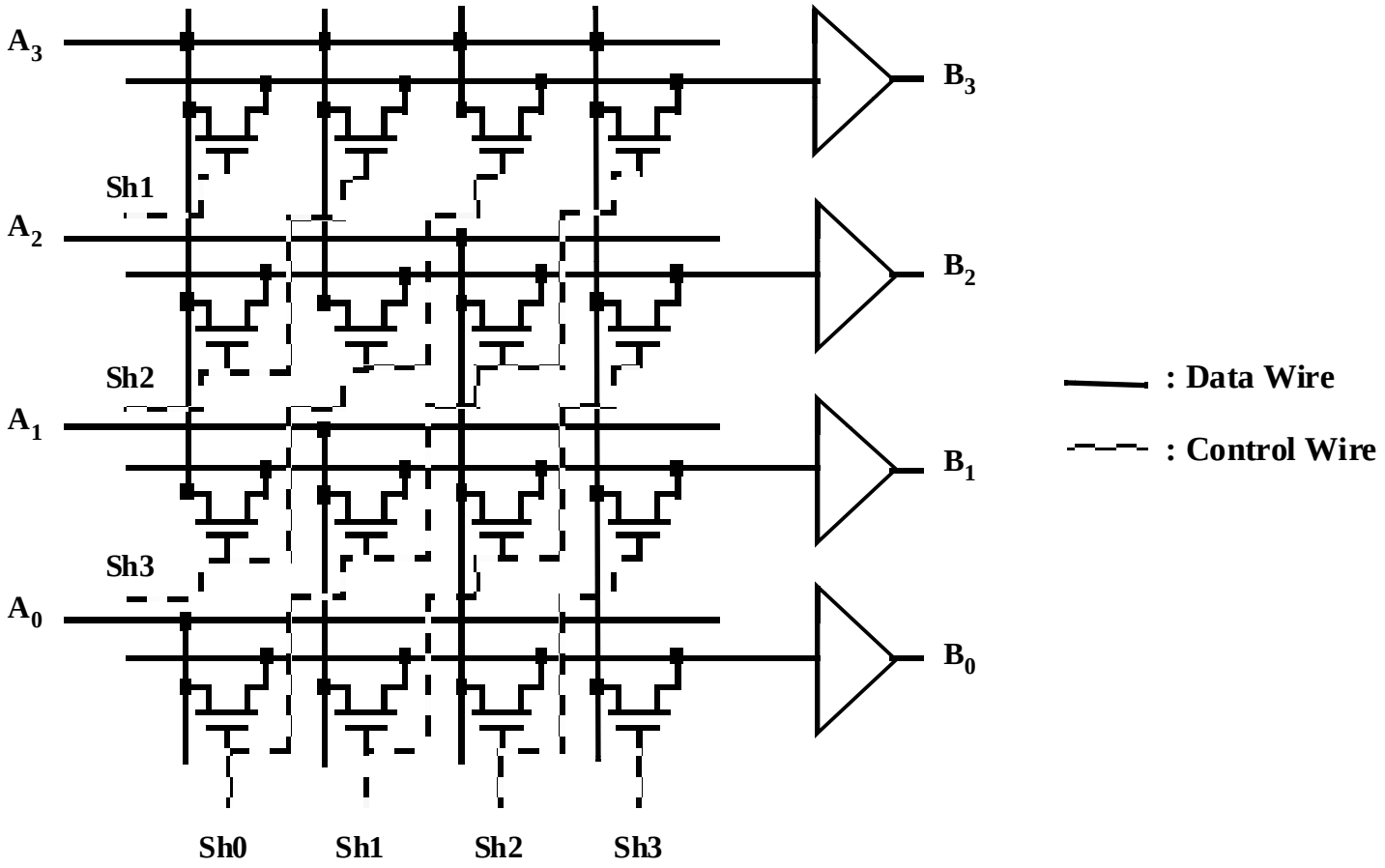




The Binary Shifter



The Barrel Shifter

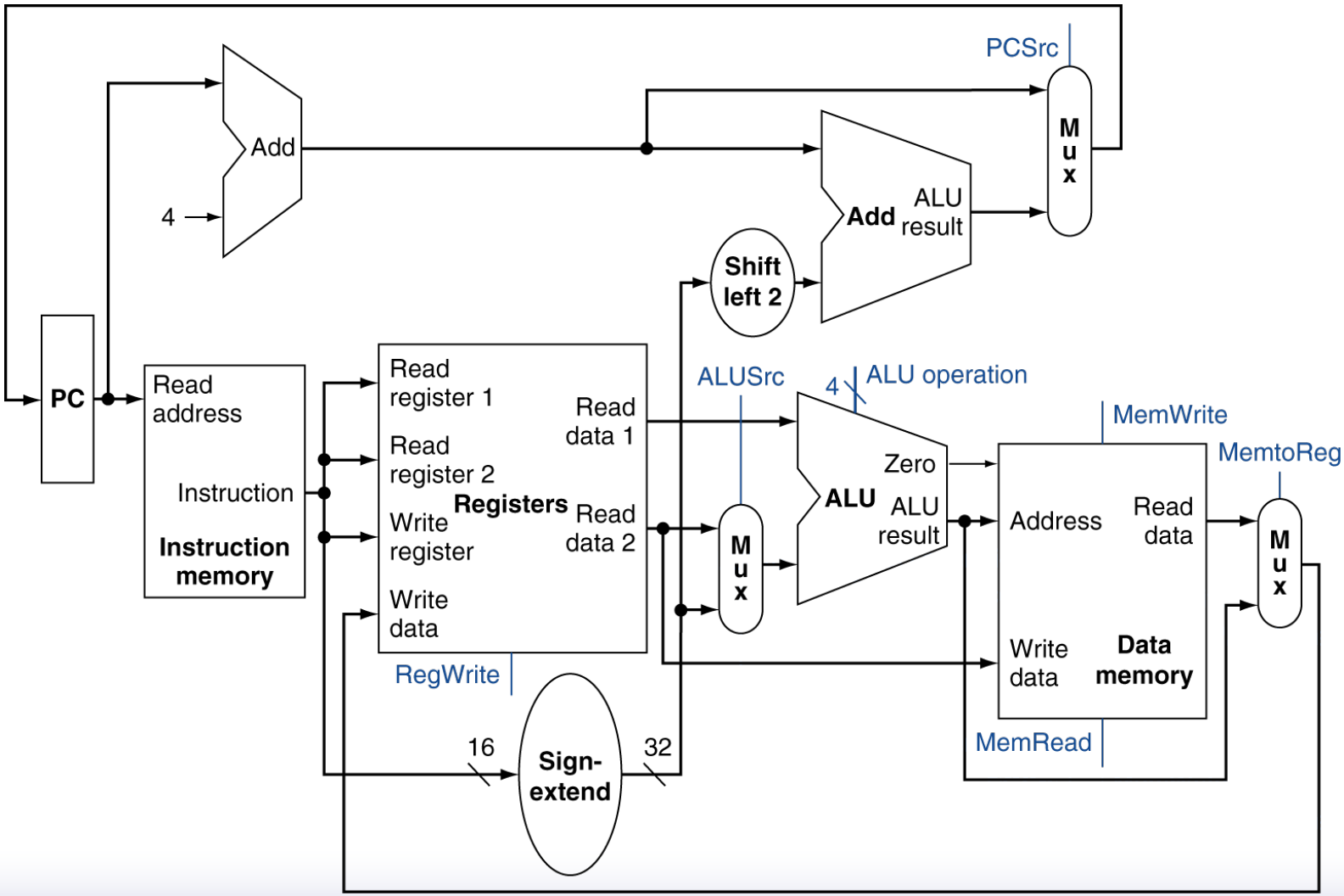


Area Dominated by Wiring

The Barrel Shifter

- Number of rows equals the word length of the data
- Number of columns equals to the maximum shift width
- The control wires are routed diagonally through the array

Full Datapath



Datapath With Control