# Self-timed Refreshing Approach for Dynamic Memories

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## Abstract

*Refreshing dynamic circuits must be carried out before stored voltages reach unacceptable levels. In this paper we present CMOS circuitry that can be used to sense the integrity of stored data, provide timely refreshing to these dynamic circuits and provide high performance. Differential amplifiers are used to provide the difference between a degrading stored voltage and a reference voltage. This difference gets converted to a single-ended output which serves as the refresh trigger. Memory arrays are used as test beds to verify the functionality and effectiveness of these circuits. The circuits considered in this paper are suitable for use in high speed, low power and high density memory arrays.*

## 1  Introduction

Low power dissipation, high density, and high performance are among the most important issues in VLSI circuits and systems. A number of techniques to maintain low power dissipation and give high performance have been developed; however, with transistor miniaturization there is a trade-off between high speed and low power dissipation depending on the threshold voltage and the power supply voltage [1]. In dynamic storage elements high performance can be compromised when the stored charge at these dynamic circuits gets degraded, due to leakage current [2],[3],[4]. Dynamic circuits, therefore, require refreshing of the stored charge. Care must be taken to refresh these circuits before unacceptable voltage levels occur. On the other hand, circuit refreshing before there is a need to do so leads to an increase in dynamic power dissipation.

A predetermined frequency at which to carry out the refreshing of dynamic circuits is often used [3],[4]. This frequency is determined by computing the time it takes for the voltage at a dynamic circuit to degrade to the lowest acceptable value. The definition of leakage current $I_D = I_{leakage} = I_S(e^{V_B/nV_T} - 1)$ is used as a basis to compute the refreshing frequency [3]. Where

$V_B$ is the maximum voltage at the dynamic node and $V_T$ is the thermal voltage. Knowledge of the leakage current and the node capacitance value allows for the computation of the change in voltage with respect to time, hence the ability to determine the frequency at which the dynamic node can be refreshed. However, this method requires a number of parameters to be determined and these parameters could vary for every silicon wafer. Use of circuitry to sense the voltage level at these storage nodes on the other hand does not require knowledge of any of the parameters associated with leakage current. We investigate the use of such circuitry in refreshing dynamic content addressable and random access memories.

In this paper we present the use of two differential amplifiers in sensing the voltage levels in dynamic memory arrays. To minimize static power dissipation within the differential amplifiers we use clocked CMOS logic [4],[5]. In Section 2 we present a system description, providing a block diagram that depicts how the refresh trigger signal is generated. In Section 3 circuitry to generate a reference signal and a test signal representative of stored data in memory and compare them is described, and in Section 4 we provide some concluding remarks.

## 2  Self-timed Refreshing Scheme

Refreshing a memory array requires use of a circuit that can provide a refreshing sequence. This circuit indicates the row that needs to be refreshed. In our approach once the refreshing process starts, it continues until the entire memory array is refreshed. This process however should be made transparent (or hidden) to other memory modes of operation [6],[7].

The refresh sequence circuit could take the form of a shift register where only one row is selected and this selection shifted to select the next row. Another approach could be to use an address decoder and a counter; where the counter could start counting from 0 and progress towards the maximum number of entries. The shift register approach needs clock, reset,

and refresh trigger (rtrigger) signals. The reset signal sets the circuit to point to the first row to be refreshed. The refresh trigger (rtrigger) signal initiates the refresh process. Thus, this signal is set when there is a need for refreshing. The goal is to set rtrigger as less frequent as possible in order to avoid unnecessary refresh cycles that consume power.

Figure 1 shows a block diagram of the circuitry that generates the rtrigger signal. A test memory cell which represents closely the memory array's cells is used to monitor a degrading stored signal. A reference signal is required to compare with the degrading stored signal; this signal is generated in the reference signal generator. A differential amplifier is required to compare these two signals and provide the difference, this is accomplished by the use of the NMOS differential amplifier. The difference between the reference signal $V_{ref}$ and the stored signal $V_s$ has to be converted into a single-ended output. The CMOS differential to digital converter shown as the last block in Figure 1 serves to convert the difference between $V_{ref}$ and $V_s$ into a single-ended output.
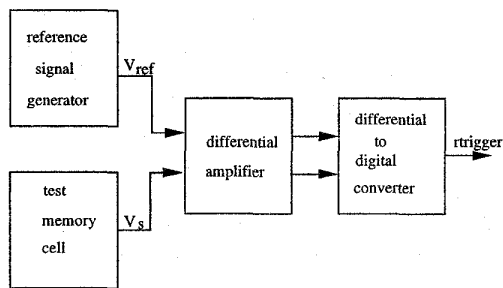


Figure 1: Block diagram of refresh trigger generator.

## 3 Refresh Trigger Signal

Dynamic circuits require periodic refreshing, in order to preserve the stored signal within acceptable limits. Dynamic random access and content addressable memories are some of the systems that require periodic refreshing [7]. There is a need to design circuitry to control the refreshing rate of the dynamic circuits. In this paper we present circuitry that provides a mechanism to trigger the refresh cycle when the voltage level is close to an unacceptable level. Several circuits have been designed to meet this goal and each has a specific function. Differential amplifiers have been used to sense the difference between the stored signal and a reference signal, and the results from this comparison are used to trigger a signal that initiates the refresh cycle. Two differential amplifiers have been used to

meet the design's requirements. Each differential amplifier requires two input signals. For the first amplifier these signals are the reference signal and a signal from a test memory cell, while the second amplifier uses the outputs from the first one as its inputs. The reference signal is kept constant at approximately 2 volts, (this being the minimum value to which we allow the stored "1" in the memory array to degrade to). The test cell stores a logic 1, that degrades with time and is monitored by way of the differential amplifiers.

### 3.1 Reference and Test Signals

The reference signal generator has been designed with the objective of keeping transistor count to a minimal, yet producing a very reliable circuit. The reference signal is shown in Figure 2(a), this circuit consists of four transistors and a write line. Transistor $T_w$ serves to pass a logic 1 to the storage element whenever the write line signal is at logic 1. The gate of transistor $T_c$ serves as the storage element for this dynamic circuit and allows a logic 1 to be passed to node $V_r$ once a "1" has been written to $V_{ref}$. We have included transistor $T_l$ to provide a temporary leakage path from the stored signal $V_{ref}$ to ground. This is necessary in order to reduce $V_{ref}$ from $V_{dd} - V_{tn}$ to the lowest acceptable value to which a stored "1" is allowed to degrade to. Transistor $T_{dr}$ is always conducting in order to drain node $V_r$ and eventually turns transistor $T_l$ off. Transistor ratios play an important role in the design of these circuits. Most of the transistors are configured to operate as resistors instead of switches, therefore, their gate lengths are made large, in order for the transistors to offer the required resistance. To maintain $V_{ref}$ at a constant voltage level, the write line signal is periodically raised to logic 1 in order to pass a "1" to the storage node. Figure 2(b) shows a plot of the generated reference signal. The simulation results on this figure shows the reference signal degrading to approximately 2.4V. If the simulation time is extended the target reference voltage of 2V is reached.

The test cell that stores the degrading signal, representative of a logic 1 stored in any of the cells in a memory array appears in Figure 3. This circuit has four transistors, bit, write and read lines. Transistors $T_{w1}$ and $T_{w2}$ are in series and serve to pass a logic value from the bit line to node $V_s$. The series combination of $T_{w1}$ and $T_{w2}$ passes a voltage slightly smaller than the voltage in a memory cell where only one transistor $T_{w1}$ is used. Thus, this voltage is going to degrade faster than a "1" stored in the memory array. This provides a safe margin in refreshing the stored data, allowing refreshing to take place before the stored voltage de-

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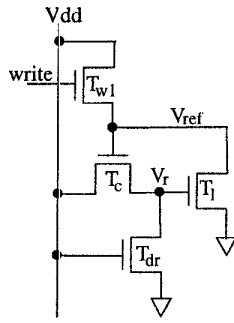
(a) $V_{ref}$ generator.
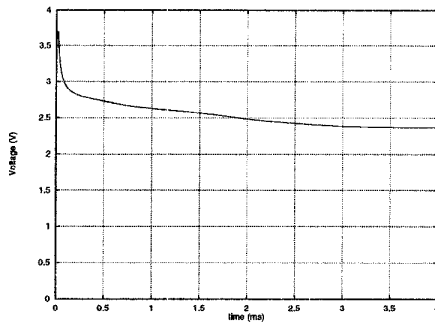


(b) Plot of reference voltage.

Figure 2: The reference signal generator.

grades to an unacceptable level. Transistor $T_{c1}$ allows the logic value on the bit line to be compared with the stored value at node $V_s$, while $T_{rx}$ is included to avoid having a direct path from the bit line to ground, with $V_s$ at logic 1. When conducting transistor $T_{rx}$ ensures that node $V_x$ is at logic 0. If the write signal is kept at logic 0, for a prolonged time after writing to node $V_s$, leakage current will cause the degradation of a stored "1" at this node. A stored "0" has been determined not to increase in value when stored. There, is therefore no test cell to monitor the behavior of a stored "0" in the design. Once a logic 1 has been written to $V_s$ the data presented on the bit line is made either a logic one or a logic 0 and is changed from time to time to represent the data presented on the bit lines of the memory arrays. The circuits of Figures 2(a) and 3, provide the input signals to the first amplifier.
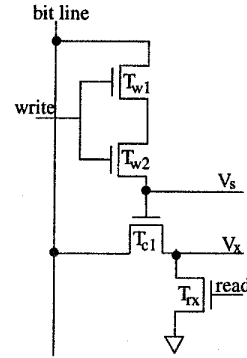


Figure 3: The test cell.

## 3.2 Comparing Reference and Test Signals

MOSFET differential amplifiers have been studied for a number of years [3],[5]. They carry different names based on different configurations. In this study we use an active load NMOS differential amplifier to compare two input signals and a CMOS current mirror (differential to digital converter) to provide a single-ended output. The NMOS differential amplifier has as its input signals: a reference signal generated by the circuit of Figure 2(a) and a degrading logic 1 stored in the test cell of Figure 3 which represents a stored "1" in a memory array.

The circuit of the NMOS differential amplifier appears in Figure 4(a). Transistors $T_{l1}$ and $T_{l2}$ constitute the resistive active load of this amplifier. The gates of these two transistors are connected to the power supply, causing them to conduct all the time. Large values for their gate lengths have been used to ensure that they present a large resistance. The gate width to gate length ratios for the load transistors are 10:8, and these values have been determined using simple KVL and KCL analysis. Transistors $T_{ref}$ and $T_s$ are driven by the reference signal from the reference signal generator and the stored signal from the test cell respectively. Transistor $T_{ref}$ is also resistive with a width to length ratio of 19:17 while that of $T_s$ is 10:8. $V_{ref}$ is a constant signal, keeping transistor $T_{ref}$ on constantly. This implies that there is always a path from the power supply to ground, since transistors $T_{l1}$, $T_{ref}$ and $T_{cs}$ are always conducting. The output voltage $V_{diffr}$ therefore has to attain a constant value. Transistor $T_s$ conducts better than $T_{ref}$, allowing $V_{diffs}$ to be discharged to logic 0 (1.5 V), as long as the stored signal from the test cell is a "good" 1. The voltage difference between $V_{diffr}$ and $V_{diffs}$ is at its maximum at startup. As $V_s$ decreases, $V_{diffs}$, approaches the value of node $V_{diffr}$. When $V_s$ finally

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has an equal value to that of $V_{ref}$ the difference between $V_{diffr}$ and $V_{diffs}$ becomes zero. This is the point of interest since the reference signal is the lowest acceptable value a stored logic 1 will be allowed to degrade to. Figure 4(b) shows a plot of $V_{diffr}$ and $V_{diffs}$. It can be seen from the figure that the difference between the two outputs does not get to zero, but does approach zero and is small enough to produce the signal required to trigger the refresh cycle.
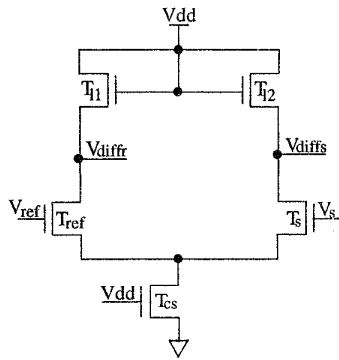

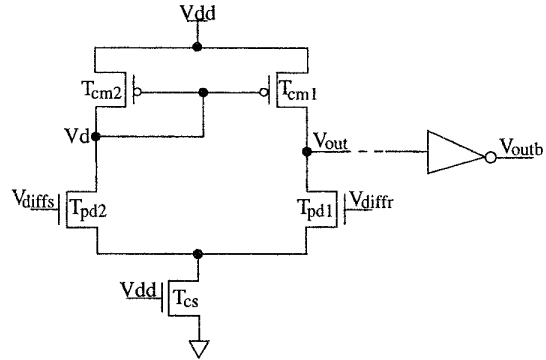
(a) Differential amplifier.
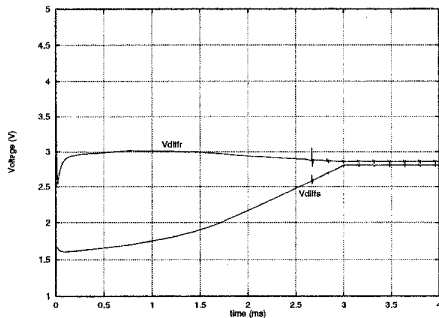
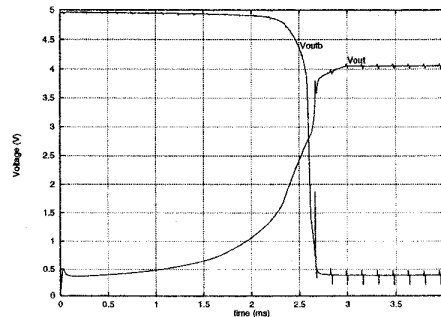

(b) Differential amplifier outputs.

Figure 4: The NMOS active load differential amplifier and a plot of the outputs.

The outputs of the differential NMOS amplifier ($V_{diffr}$ and $V_{diffs}$) serve as the input to the CMOS differential to digital converter which transforms these two inputs into a single-ended digital output. Figure 5(a) shows the differential to digital converter. The transistors that form the current mirror are $T_{cm1}$ and $T_{cm2}$, and their gates are connected to the drain of transistor $T_{cm2}$. If $V_{diffs}$ is at logic 0, transistors $T_{cm1}$ and $T_{cm2}$ will not conduct since node $V_d$ will not

be at logic 0. In Figure 4(b), it has been shown that $V_{diffs}$ is initially at logic 0, hence transistors $T_{cm1}$ and $T_{cm2}$ are off. As $V_{diffs}$ makes a gradual transition to logic 1, transistor $T_{pd2}$ starts conducting, discharging node $V_d$. This sets the gates of transistors $T_{cm1}$ and $T_{cm2}$ to logic 0, and causes node $V_{out}$ to charge up. Initially node $V_{out}$ is at logic 0 since transistor $T_{pd1}$ is always on, but poorly conducting. Transistor $T_{pd1}$ has been made to conduct poorly in order to avoid rapidly discharging node $V_{out}$ once $T_{cm1}$ starts conducting. When the current mirror pair start to conduct node $V_{out}$ makes a transition from logic 0 to logic 1. Figure 5(b) shows a plot of the single-ended output. $V_{out}$ makes a transition from logic 0 to logic 1 at the time the difference between $V_{diffr}$ and $V_{diffs}$ is approximately zero; when $V_{ref}$ is equal to $V_s$.



(a) Differential to digital converter.



(b) Single-ended output and its inverse.

Figure 5: The CMOS active load differential amplifier and a plot of the outputs.

The NMOS differential amplifier always has a direct path from the power supply to ground, and thus

dissipates power continuously. The CMOS current mirror has a similar situation once node $V_d$ is discharged. To prevent continuously dissipating power, clocked CMOS gates have been used. One p-type transistor has been added to each of the amplifier circuits of Figures 4(a) and 5(a). This scheme is shown in Figure 6. This p-type transistor has been included at the drains/sources of the load transistors and its gate is clocked by the inverse of the clock that drives the $T_{cs}$ transistors of the two amplifiers. Using clocked CMOS reduces power dissipation since the direct path between $V_{dd}$ and ground is not present all the time. The circuits described above are used in high density memory arrays. Only one instance of the circuitry described above gets included in the system.
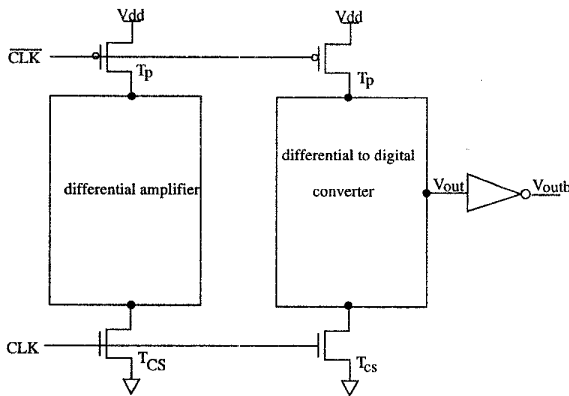


Figure 6: Clocked scheme to reduce power consumption.

## 4  Concluding Remarks

In this paper we have proposed circuitry that can be used to sense the levels of stored data and ensure refreshing of such data if it has reached a low acceptable level. Our circuitry takes into consideration power dissipation and high speed operations. Since both differential amplifiers may draw current constantly, clocked CMOS gates have been used in order to minimize power dissipation. A memory system has been used to determine the functionality and effectiveness of the design. We have presented circuits to trigger the refreshing process of dynamic circuits in content addressable and random access memories in order to maintain low power dissipation and operating at high clock rates. We have used a differential amplifier to compare a signal that represents degrading stored voltages and one that serves as the minimum value to which the stored signal is allowed to degrade to and still be considered a valid logic level. The difference between these sig-

nals gets converted into a single-ended digital output by means of a CMOS differential to digital converter circuit. The output of the differential to digital converter provides a refresh trigger; a signal which initiates the refresh cycle. A dynamic CAM based system that uses the proposed self-timed refresh approach has been fabricated using CMOS technology.

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