Through-Silicon-Via-aware Delay and Power Prediction Model for Buffered Interconnects in 3D ICs *

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ABSTRACT

In this paper, we present a delay and power prediction model for buffered interconnects used in 3D ICs. The key idea is to model the impact of RC parasitics of Through-Silicon Vias (TSVs) used in 3D interconnects on delay and power consumption. Due to its large size compared with other layout objects such as metal wires, TSVs contain significant RC parasitics, which directly affect the overall delay and power of the wires that contain them. On the other hand, buffer insertion on TSV-based 3D interconnects is also non-trivial mainly because buffers as well as TSVs have non-trivial area overhead. In addition, both TSVs and buffers occupy device and M1 layers, thereby becoming layout obstacles to each other. Our interconnect model accurately captures the impact of both TSVs and buffers on 3D interconnects.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids—*Simulation*; J.6 [**Computer-Aided Engineering**]: Computer-aided design (CAD)

General Terms

Algorithms, Experimentation, Theory

Keywords

TSV, Through-Silicon Via, 3D IC, Interconnect, Delay, Power, Buffer

1. INTRODUCTION

Recently three-dimensional integrated circuit (3D IC) has emerged as a possible candidate to resolve the performance and power limitation of 2D ICs. The total interconnect length of 3D IC is expected to be shorter than that of 2D IC [1] because transistors are placed in several dies so that the footprint area of 3D IC becomes smaller than that of 2D IC. Wirelength reduction in 3D ICs has been shown in several prediction studies [1–3], GDSII-level designs [4], and a real chip design [5].

One key observation regarding TSVs used in 3D IC layouts is that TSVs occupy significant amount of silicon area. For example, it is shown in [4] that TSV and its keep-out zone altogether has 4x larger area compared with a square-shaped standard cell. As a result, total wirelength reduction in 3D ICs is not as significant as one might expect [2, 3] although 3D wirelength [2] is in general shorter than 2D wirelength. However, the amount of increased silicon area due to TSV insertion depends highly on TSV size and the number of TSVs used in the layout.

Another important observation is that TSVs have non-negligible parasitic resistance and capacitance (RC) so that the delay of a 3D net[3] can be significantly affected by TSVs inserted in the net. For example, $20fF$ TSV capacitance is comparable to the capacitance of a $120\mu m$-long intermediate-layer wire (e.g. M4 to M6) in $45nm$ technology. In addition, TSV RC has a characteristic different from wire RC, which will be shown in Section 3. Therefore, if we use wire RC models for TSV parasitics, there will be non-negligible amount of errors in computation and prediction of TSV-related delay and power consumption in 3D ICs.

In this paper, we investigate the impact of TSV RC parasitics on delay and power consumption of buffered interconnects in 3D ICs. We extend the TSV-aware wirelength prediction model presented in [3] to model buffer insertion and show the delay of 3D nets under various TSV RC parasitics. We also present the power reduction/overhead mainly caused by TSV capacitance. Our experiments show that TSV capacitance has huge impact on delay and power of 3D ICs and that a proper buffer insertion scheme is crucial to correctly model the 3D interconnect in 3D ICs.

The rest of this paper is organized as follows. In Section 2, we review the related works such as 3D wirelength prediction models, and show the motivation of this work. Characteristics of TSV resistance and capacitance are explained in Section 3. In Section 4, we show our two simple buffer insertion schemes used in our model. In Section 5, we describe the TSV-aware delay computation for buffered 3D interconnects. Various experimental results are presented in Section 6. We discuss future works in Section 7, and conclude in Section 8.

2. PRELIMINARIES

2.1 TSV-aware 3D Wirelength Prediction

The authors of [1] presented a TSV-aware 3D wirelength prediction model. In the model, they include the TSV height in the wire-

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[1] '2D (or 3D) IC' means an IC designed in one die (or in multiple dies).

[2] '2D (or 3D) wirelength' means the wirelength of a 2D IC (or 3D IC).

[3] '2D (or 3D) net' means a net whose cells are placed in one die (or in multiple dies).

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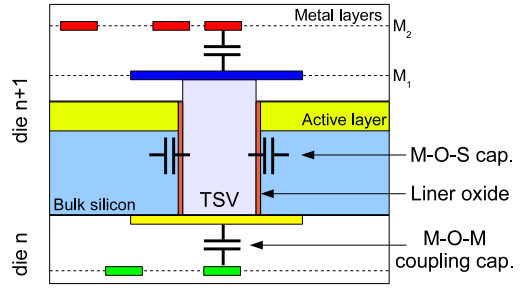

Figure 1: Via-first TSV and its capacitive components in face-to-back die bonding

length computation, thus the TSV height is treated as a wirelength. On the other hand, the authors of [6] presented a 3D wirelength prediction model. In the model, they include repeater (buffer) insertion considering electrical characteristics of TSVs. However, both works do not take TSV area and realistic TSV RC characteristics into account.

The authors of [3] observed that TSVs used in face-to-back die bonding (see Figure 1) occupy significant silicon area. This causes two important effects. First, 3D ICs may need more silicon area than 2D ICs depending on the number of TSVs used. The overall wirelength reduces upon more TSV usage up to a certain point. If more TSVs are used after that point, the wirelength goes back up primarily because the total area occupied by the TSVs cause the footprint area to increase. These TSVs also cause significant routing congestion, thereby increasing the overall wirelength again. Second, the real 3D wirelength will be longer than the predicted 3D wirelength if the silicon area is expanded significantly. Therefore, the authors of [2, 3] extended the 3D wirelength prediction model in [1] to consider the area expansion caused by TSV insertion. According to the results presented in [2], the additional silicon area required for TSVs has significant impact on the amount of wirelength reduction. For instance, wirelength reduction of a $40M$-gate 4-die 3D IC is 41% compared to 2D if we ignore TSV area. However, the wirelength reduction becomes 29% if we consider TSV area. Therefore, TSV area needs to be taken into account for 3D wirelength prediction.

2.2 Motivation of Our Work

The goal of our work in this paper is to model the impact of TSVs on the delay and power consumption of 3D interconnects. We also consider buffer insertion to model signal propagation on long global interconnects in 3D ICs. Buffers are essential in driving the large TSV capacitance. To the best of our knowledge, however, none of the existing 3D wirelength prediction works mentioned in previous sections address TSV RC parasitics. TSV height in [1] is a physical length, but the electrical characteristics of TSVs are different from those of wires. For example, the cross-sectional area of a TSV is much larger than that of a wire. Therefore, the resistance per unit length and the capacitance per unit length of a TSV are quite different from wire RC parasitics.

As shown in Figure 1, TSVs have very different kinds of coupling neighbors compared with wires. For example, the TSV landing pad in the top metal layer of the bottom die couples with other metal layers in that die. Likewise, the TSV landing pad in M1 of the top die also experiences similar coupling. Lastly, TSVs have capacitive coupling with neighboring TSVs if the bulk silicon is not DC-biased strongly, or have a MOS (metal oxide silicon) capacitor if the bulk silicon is DC-biased strongly.

Table 1: Variables affecting TSV capacitance and their effects

Variable	Effects	
	Capacitance	Chip
TSV width (or diameter) ↑	MOS cap. ↑ MOM coupling cap. ↑	Die area ↑ Wirelength ↑
TSV height ↑	MOS cap. ↑	
Liner oxide thickness ↑	MOS cap. ↓	Die area ↑ Wirelength ↑

Table 2: Variation of TSV capacitance

Dimension (μm)			Capacitance (fF)	
Width	Height	Liner oxide thickness	MOS cap.	Coupling cap.
2.0	40.0	0.1	133.7	0.6
4.0	40.0	0.1	261.2	2.4
2.0	10.0	0.1	33.4	0.6
2.0	20.0	0.1	66.9	0.6
2.0	10.0	0.1	33.4	0.6
2.0	10.0	1.0	4.7	5.3

On the other hand, buffer insertion on TSV-based 3D interconnects is also non-trivial. Buffers as well as TSVs have non-trivial area overhead. In addition, both TSVs and buffers occupy device and M1 layers, so they cannot overlap with each other. Therefore, buffer model has to address these issues when used to predict the impact on delay and power of 3D interconnects.

3. TSV PARASITIC RC

In this section, we present TSV RC models and values which will be used in this paper.

3.1 TSV Resistance

TSV resistance consists of a material resistance ($= \rho \cdot \frac{l}{S}$) of a TSV itself and the contact resistance between a TSV and a landing pad at both ends of the TSV. The material resistance of a TSV is small in general because the cross-sectional area of a TSV is much bigger than that of a wire. For instance, assuming 1) TSV is made of tungsten, 2) TSV width is $2\mu m$, and 3) TSV height is $20\mu m$, the material resistance is $280m\Omega$ which is much smaller than the resistance of a very short wire. On the other hand, the contact resistance is strongly dependent on TSV manufacturing and die bonding technologies. In our simulation, we use 100Ω as the baseline TSV resistance, which is the sum of the material resistance and the contact resistance.

3.2 TSV Capacitance

Assuming the bulk silicon around a TSV is DC-biased well as discussed in [7], TSV capacitance consists mainly of TSV(M)-Insulator(O)-Silicon(S) capacitance and TSV(M)-Insulator(O)-Wire(M) coupling capacitance as shown in Figure 1. The variables affecting these MOS and MOM TSV capacitances and their effects are shown in Table 1. As the table shows, TSV width and height are strongly related to TSV capacitance as well as the die area and the total wirelength in 3D ICs. For example, if the liner oxide thickness increases, TSV MOS cap decreases but the die area increases, and so does the total wirelength.

In Table 2, we show the capacitances of various combinations of TSV dimensions such as TSV width, height and the liner oxide thickness. We obtain these values by simulating the structures with Synopsys Raphael [8]. The assumptions that we use for this simulation are shown in Table 3). As Table 2 shows, TSV capacitance

Table 3: Parameters and assumptions used in this paper

Parameter or assumption	Value
TSV shape	Square
TSV type	Via-first
Die-bonding type	Face-to-back
TSV width + liner oxide thickness + keep-off distance	$2.47\mu m$
TSV resistance	100Ω
Die-to-gate-pitch ratio (r) [1]	40
Device technology	$45nm$
Wire resistance of intermediate metal layers	$3.31\Omega/\mu m$
Wire capacitance of intermediate metal layers	$0.171fF/\mu m$
Output resistance of a $20\times$ buffer	305Ω
Input capacitance of a $1\times$ buffer	$1.55fF$
Buffer delay	$70ps$
Buffer switching energy	$6.65fJ$
Buffer switching power @ $1GHz$	$6.65\mu W$
Buffer switching activity	0.3
L_{FIX} (see Figure 4)	$350\mu m$
Cell switching energy (avg.)	$7.28fJ$
Cell switching power (avg.) @ $1GHz$	$7.28\mu W$
Cell switching activity	0.5
Rent's parameter α	0.75
Rent's parameter k	4.0
Rent's parameter p	0.75
Gate pitch	$1.37\mu m$
Output resistance of a $1\times$ buffer	R_{drv}
Input capacitance of a $1\times$ buffer	C_{drv}
Wire resistance per unit length	r_{wire}
Wire capacitance per unit length	c_{wire}
Buffer size	S_{buf}
Buffer delay	D_{buf}

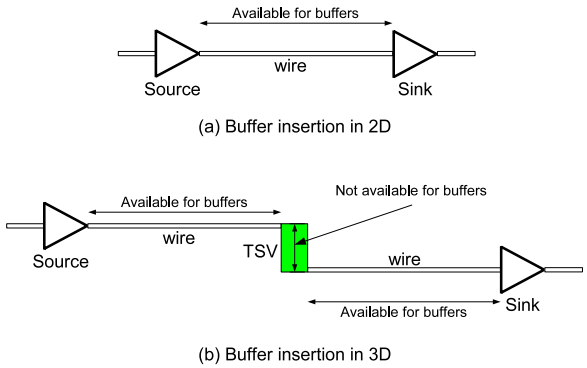

Figure 2: Buffer insertion in 2D and 3D ICs

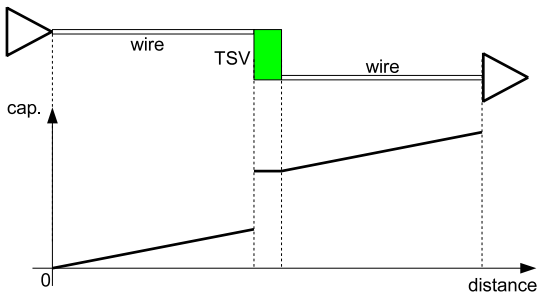

Figure 3: Distance-capacitance plot in a 3D wire

varies in a wide range depending on TSV width and height, and the liner oxide thickness. Therefore, we change the TSV capacitance from $5fF$ to $50fF$ in our simulation to cover the wide range of TSV capacitance.

4. BUFFER INSERTION SCHEMES

Theoretically a metal wire can be cut and split into two segments, and a buffer can be inserted into the cut point if there exists enough empty space to insert buffers along the wire. On the other hand, buffers cannot be inserted inside a TSV. Buffers actually can be inserted into one end or both ends of a TSV. In other words, buffers for metal wires that have no TSVs can be inserted anywhere along the wires, whereas buffer insertion for 3D interconnects that contain TSVs has to avoid TSV obstacles. This is illustrated in Figure 2 and Figure 3.

In our delay prediction model, we use two buffer insertion schemes for 2D and 3D ICs to illustrate the impact of TSV RC on delay and power. Our buffering scheme is based on the consideration that buffer insertion cannot be too much detailed during wirelength prediction. The first scheme, **BIS1** (Buffer Insertion Scheme 1), is to insert a buffer at every fixed distance as shown in Figure 4 (a). This applies to both 2D ICs and 3D ICs. In 3D ICs, we also insert a buffer in front of a TSV to increase the driving strength for the TSV. The second scheme, **BIS2** (Buffer Insertion Scheme 2), is same as BIS1 but we insert an additional buffer at the end of a TSV as shown in Figure 4 (b) so that we minimize the TSV RC effect on delay. The distance-capacitance plots for BIS1 and BIS2 are shown in Figure 4.

Another assumption used in our simulation for buffer insertion is that a buffer is in fact a buffer chain. The first buffer in the buffer chain is a $1\times$ buffer, thus the input capacitance is minimized. The last buffer in the chain is a $20\times$ buffer, thus the output resistance becomes sufficiently small. The buffers between them are properly scaled based on the process technology. The internal delay of the buffer chain is $70ps$.

5. DELAY COMPUTATION

In this section, we briefly explain how we calculate the delay of 3D wires.

5.1 3D Wire Delay without TSV RC and without Buffer Insertion

When we ignore TSV RC, we add TSV height into wirelength to include the impact of TSVs on delay. Therefore, TSVs are considered as plain wires in this case. Then the delay of a wire whose length is $L(\mu m)$ is computed using Elmore delay as follows:

$$D_1(L) = \frac{R_{drv}}{S_{buf}} \cdot c_{wire} \cdot L + \frac{1}{2} \cdot r_{wire} \cdot c_{wire} \cdot L^2 + (\frac{R_{drv}}{S_{buf}} + r_{wire} \cdot L) \cdot C_{drv} \quad (1)$$

where the definitions of the variables are shown in Table 3.

5.2 3D Wire Delay without TSV RC and with Buffer Insertion

If we consider buffer insertion, we first split a 3D wire of length $L(\mu m)$ into segments of length L_{FIX} (Figure 4). The delay of a wire segment of length L_{FIX} is computed by $D_1(L_{FIX})$ in Equation (1). If the length of a 3D wire is not a multiple of L_{FIX}, we also add the delay of the remaining length. The delay of a 3D wire is then computed as follows:

$$D_2(L) = n_{buf} \cdot (D_1(L_{FIX}) + D_{buf}) + D_r \quad (2)$$

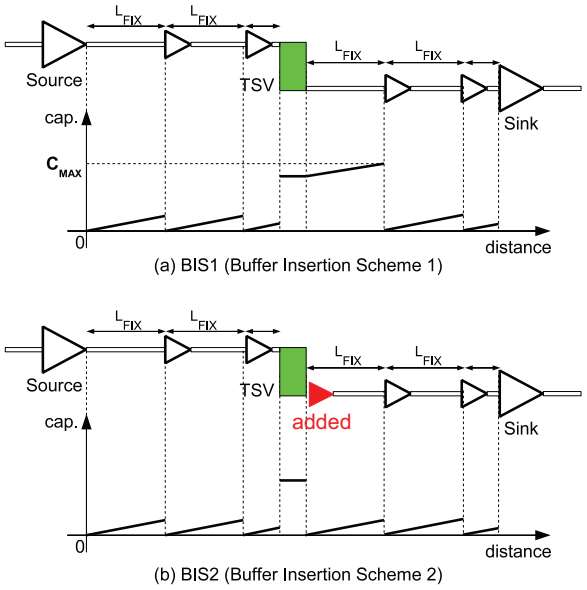

Figure 4: Two buffer insertion schemes used in this paper and their distance-capacitance plot

where n_{buf} is the number of buffers in the wire and D_r is the wire delay of the remaining length.

5.3 3D Wire Delay with TSV RC and with Buffer Insertion

If a wire is a *PV* wire whose horizontal length is negligible [2], the delay of the wire is computed as follows:

$$D_{PV} = N_{TSV} \cdot \frac{R_{drv}}{S_{buf}} \cdot C_{TSV} + \frac{1}{2} \cdot {N_{TSV}}^2 \cdot R_{TSV} \cdot C_{TSV} + (\frac{R_{drv}}{S_{buf}} + N_{TSV} \cdot R_{TSV}) \cdot C_{drv} \quad (3)$$

where N_{TSV} is the number of TSVs in the wire, R_{TSV} is the TSV resistance, and C_{TSV} is the TSV capacitance. We use Π-model to convert TSV RC into an equivalent RC model. In the above equation, we did not consider buffers. If we take buffer insertion into account, the delay becomes as follows:

$$D'_{PV} = \frac{1}{2} \cdot \frac{R_{drv}}{S_{buf}} \cdot C_{TSV} \cdot N_{TSV} + (\frac{R_{drv}}{S_{buf}} + R_{TSV}) \cdot (\frac{1}{2} \cdot C_{TSV} + C_{drv}) \cdot N_{TSV} + (N_{TSV} - 1) \cdot D_{buf} \quad (4)$$

Delay computation for *NPV* wires whose horizontal length is not negligible [2] is computed by combining Equation (1), (2), and Π-model of TSV RC with wire RC model.

6. EXPERIMENTAL RESULTS

In this section, we first compare the maximum delay and buffer counts in 2D and 3D ICs. Impact of TSV resistance and capacitance on the delay of short and medium wires is shown in the next subsection. We also present the impact of TSV RC on delay and power consumption in different circuit sizes. Since buffers need additional silicon area, we show the amount of silicon area required by buffer insertion. Table 3 shows the parameters and assumptions used in our simulation.

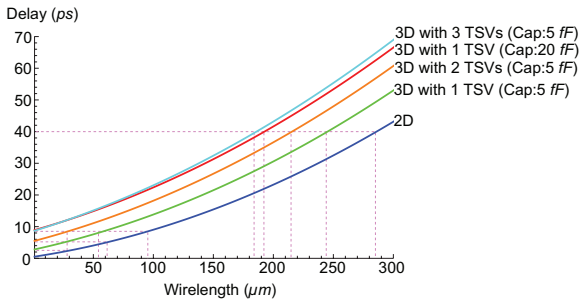

Figure 6: Comparison of delay in various cases. Wirelength in the x-axis does not include TSV height, and we assume that TSVs are evenly distributed along a 3D net. The driver size is $20\times$, and buffer insertion was not used.

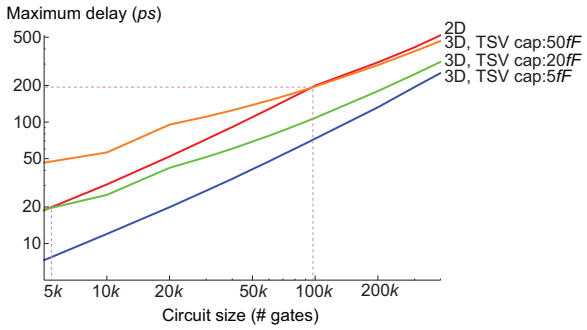

Figure 8: Circuit size vs maximum delay. # dies = 4.

6.1 Maximum Delay and Buffer Count

In Table 4, we compare the maximum delay and buffer counts of 2D and 3D ICs. In case of 2D ICs, we use the 2D wirelength prediction model in [9]. The 3D IC prediction is done using the TSV-aware 3D wirelength prediction model in [3], where TSV RC parasitics are not considered.

First, columns (2), (5), and (8) in Table 4 compare the maximum delay without buffer insertion. The longest wire in 2D is about $14.6mm$ so that the delay in 2D is very high ($61.3ns$) without buffer insertion. On the other hand, the longest wire in 3D is about $9.0mm$ so that the delay without TSV RC in 3D is much smaller ($23.5ns$) than the 2D delay ($61.3ns$). Impact of TSV RC is shown in column (8) in Table 4. The maximum delay increases as TSV capacitance goes up. TSV resistance shows a similar trend, but we did not show the results in the table for brevity. However, the effect of TSV RC on the longest net is not significant because wire RC is much larger than that of TSVs in long nets. The impact of TSV RC on short/medium wires will be shown in the next section.

Next, columns (3), (6), (9), and (11) in Table 4 compare the maximum delay with buffer insertion. The columns (4), (7), (10), and (12) compare the buffer usage for these cases. The maximum delay in 2D becomes $5.29ns$ after buffer insertion. On the other hand, the maximum delay in 3D becomes $3.24ns$ without TSV RC after buffer insertion. The difference ($2.05ns$) is quite significant because the longest wire ($9.0mm$) in 3D is much shorter than that ($14.6mm$) in 2D. The buffer count ($4.94M$) in 3D is also much smaller than the buffer count in 2D ($9.8M$).

If we consider TSV RC during delay computation, the maximum delay ($\sim 9.2ns$) becomes much bigger than the case without TSV RC ($3.24ns$). Moreover, the maximum delay is even bigger than the 2D case ($5.29ns$), and the buffer count ($11.8M$) increases sig-

Table 4: Comparison of the maximum delay. 'B.I.' means 'Buffer Insertion'. BIS1 is the Buffer Insertion Scheme 1, and BIS2 is the Buffer Insertion Scheme 2 shown in Figure 4. '# B' is the number of buffers. (Design : # gates = $40M$, # dies = 4, and # signal TSVs = $8.3M$).

TSV cap. (fF)	Delay of a 2D design [9] (longest WL = $14.6mm$)			Delay of a 3D design (longest WL = $9.0mm$)							
				Without TSV RC [3]			With TSV RC				
	w/o B.I.	BIS1	# B	w/o B.I.	BIS1	# B	w/o B.I.	BIS1	# B	BIS2	# B
5	$61.3\ ns$	$5.29\ ns$	$9.8M$	$23.5\ ns$	$3.24\ ns$	$4.94M$	$23.5\ ns$	$9.22\ ns$	$11.8M$	$3.56\ ns$	$20.1M$
20							$24.0\ ns$	$9.23\ ns$		$3.57\ ns$	
50							$25.4\ ns$	$9.24\ ns$		$3.61\ ns$	
(column #)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)
Ratio of delay w/o B.I.	1.00			0.38			0.38 0.39 0.41				
Ratio of delay with B.I.		1.00			0.61			1.74 1.74 1.75		0.67 0.67 0.68	
Ratio of buffer count			1.00			0.50			1.20		2.05

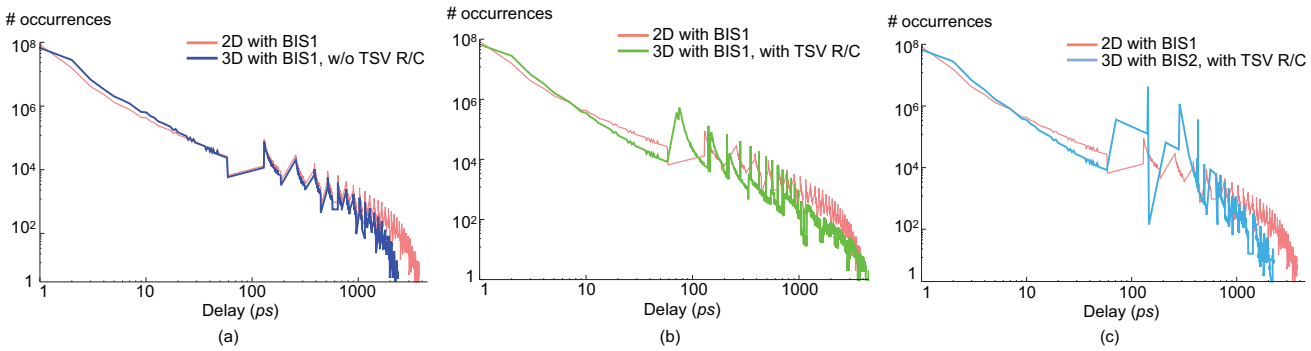

Figure 5: Delay distribution of 3D ICs ($40M$ gates). (a) 3D with BIS1, w/o TSV RC, (b) 3D with BIS1, with TSV RC, and (c) 3D with BIS2, with TSV RC. TSV capacitance is $5fF$.

Table 7: Additional silicon area (in mm^2) required for buffer insertion)

Chip area (mm^2)	# gates	2D	3D w/o TSV RC	3D with TSV RC	
		BIS1	BIS1	BIS1	BIS2
250.3	$100M$	64.0	33.0	66.1	106.8
125.1	$50M$	25.0	12.7	28.9	48.6
25.0	$10M$	2.63	1.24	4.28	7.83
12.5	$5M$	1.4	0.43	1.90	3.57
2.50	$1M$	0.07	0.03	0.29	0.56
1.25	$500K$	0.02	0.01	0.13	0.25
0.25	$100K$	0.0004	0.0001	0.02	0.04

nificantly in BIS1 because we insert a buffer right in front of a TSV. The increased maximum delay ($\sim 9.2ns$) is mainly due to C_{MAX} shown in Figure 4. Moreover, if we do not insert a buffer in front of a TSV, the maximum delay becomes much bigger than $9.2ns$.

In order to decrease the impact of TSV capacitance on the delay, we insert a buffer as an intermediate sink at another end of a TSV in BIS2 as shown in Figure 4, and the maximum delay ($\sim 3.6ns$) finally becomes lower than the 2D case ($5.29ns$). However, the buffer count increases significantly ($20.1M$).

Figure 5 shows the delay distribution of the four cases (column 3, 6, 9, 11) in Table 4. As expected, there are more wires having small delay in 3D than 2D. In addition, the green graph in Figure 5(b), which shows '3D with BIS1, with TSV RC', has the biggest delay because C_{MAX} in the case is the biggest capacitance which a buffer should drive. The discontinuities in Figure 5 are caused by buffer insertion.

6.2 Impact of TSV RC on Short and Medium Wires

Figure 6 shows delays in various cases for short/medium wires in 2D and 3D. First of all, there exists an intrinsic delay in a 3D net. This intrinsic delay cannot be decreased further because there exist TSVs in the net. Moreover, the intrinsic delay is strongly related to the number of TSVs used in a 3D net as well as TSV RC. For example, the intrinsic delay of '3D with 1 TSV' is $3ps$ when the TSV capacitance is $5fF$, and $9ps$ when the TSV capacitance is $20fF$ as shown in Figure 6. Similarly, the intrinsic delay of '3D with 3 TSVs' is $9ps$ when the TSV capacitance is $5fF$.[4]

In addition, the minimum delay of '3D with 1 TSV (Cap:$5fF$)' is $3ps$, but this delay corresponds to a $30\mu m$-long wire in 2D. Similarly, the delay of a short 3D wire having three TSVs (Cap:$5fF$) is $9ps$, but this delay corresponds to a $90\mu m$-long wire in 2D. Therefore the following two cases have the same delay:

- Two gates are placed in 2D and their distance is $90\mu m$.
- One gate is placed in $die0$, another gate is placed in $die3$ in 3D (so that there exist three TSVs), their horizontal distance is almost zero, and the TSV capacitance is $5fF$.

In order to benefit from 3D design for this net, the two gates need to be connected through less than three TSVs.

[4]The intrinsic delay in Figure 6 is small because the driver size is $20\times$.

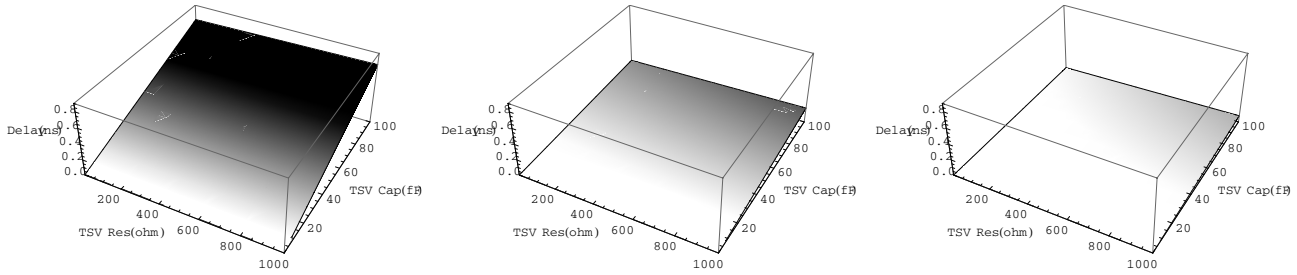

Figure 7: TSV RC vs Delay for each buffer size. (a) $1\times$ buffer, (b) $5\times$ buffer, (c) $20\times$ buffer

Table 5: Comparison of the maximum delay and buffer counts in different circuit sizes. TSV resistance is 100Ω and TSV capacitance is $20fF$. # dies = 4.

circuit		longest wire		2D			3D w/o TSV RC			3D with TSV RC				
area	# gates	2D	3D	w/o B.I.	BIS1	# B	w/o B.I.	BIS1	# B	w/o B.I.	BIS1	# B	BIS2	# B
$400\ mm^2$	$160M$	$29\ mm$	$18\ mm$	$243\ ns$	$10.7\ ns$	$64.2M$	$94.9\ ns$	$6.60\ ns$	$33M$	$95.6\ ns$	$30.6\ ns$	$62M$	$6.86\ ns$	$97M$
$225\ mm^2$	$90M$	$22\ mm$	$14\ mm$	$137\ ns$	$7.98\ ns$	$29.6M$	$53.1\ ns$	$4.92\ ns$	$15.3M$	$53.9\ ns$	$18.5\ ns$	$31M$	$5.18\ ns$	$50M$
$100\ mm^2$	$40M$	$15\ mm$	$9\ mm$	$61\ ns$	$5.29\ ns$	$9.78M$	$23.5\ ns$	$3.24\ ns$	$4.94M$	$24.0\ ns$	$9.23\ ns$	$12M$	$3.57\ ns$	$20M$
$25\ mm^2$	$10M$	$7.3\ mm$	$4.4\ mm$	$15.6\ ns$	$2.61\ ns$	$1.38M$	$5.84\ ns$	$1.57\ ns$	$0.66M$	$6.11\ ns$	$3.12\ ns$	$2.28M$	$2.00\ ns$	$4.17M$
$1\ mm^2$	$0.4M$	$1.5\ mm$	$0.8\ mm$	$0.70\ ns$	$0.52\ ns$	$7.09K$	$0.25\ ns$	$0.27\ ns$	$1.90K$	$0.31\ ns$	$0.45\ ns$	$51.7K$	$0.45\ ns$	$103K$
(column #)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)
Ratio of delay w/o B.I.	$160M$			1.00			0.39			0.39				
	$90M$			1.00			0.39			0.39				
	$40M$			1.00			0.39			0.39				
	$10M$			1.00			0.37			0.39				
	$0.4M$			1.00			0.36			0.44				
Ratio of delay with B.I.	$160M$				1.00			0.62			2.86		0.64	
	$90M$				1.00			0.62			2.32		0.65	
	$40M$				1.00			0.61			1.74		0.67	
	$10M$				1.00			0.60			1.20		0.77	
	$0.4M$				1.00			0.52			0.87		0.87	
Ratio of buffer count	$160M$					1.00			0.51			0.97		1.51
	$90M$					1.00			0.52			1.05		1.69
	$40M$					1.00			0.51			1.23		2.04
	$10M$					1.00			0.48			1.65		3.02
	$0.4M$					1.00			0.27			7.29		14.5

Figure 6 also shows that TSV RC needs to be considered in delay computation. According to the figure, using one TSV having bigger capacitance ($20fF$ for example) could be better than using three TSVs having smaller capacitance ($5fF$ for example) if TSVs are distributed evenly.

We also present the impact of TSV RC on the delay for each buffer size in Figure 7. When the buffer size is small ($\sim 1\times$), the delay changes in a wide range ($10ps$ to $700ps$) as TSV capacitance varies from $1fF$ to $100fF$. On the other hand, TSV resistance does not have big impact on delay. For a medium-size buffer ($\sim 5\times$), TSV capacitance again has significant impact on delay, but the delay range ($2ps$ to $200ps$) is smaller than that of the $1\times$ buffer case. The impact of TSV resistance in this case becomes bigger if TSV capacitance is high. If the buffer size is big ($\sim 20\times$), the impact of TSV RC becomes small as shown in Figure 7(c).

6.3 Impact of TSV RC on Delay in Different Circuit Sizes

In Table 5, we compare the maximum delay and buffer counts for various circuit sizes. Columns (5), (8), and (11) in Table 5 compare the maximum delay without buffer insertion. In all the cases, the maximum delay of 3D ICs is much smaller than the maximum delay of 2D ICs even when we consider TSV RC. This is again mainly due to the fact that wire RC is dominant in the longest wire. However, the difference between '2D w/o B.I.' and '3D w/o B.I. with TSV RC' becomes smaller as the circuit size goes down. 2D delay could eventually be smaller than 3D delay if the circuit size is very small. This means that 1) 2D ICs are superior to 3D ICs for small circuits, and 2) there exists a reversion point where 2D designs become better than 3D designs or vice versa. Since TSVs are used only in 3D ICs, the reversion point where 2D delay and 3D delay meet will increase as the TSV capacitance increases as shown in Figure 8. For example, if the TSV capacitance is $50fF$, the circuit should contain more than about $100k$ gates to benefit from 3D design.[5]

Columns (6), (9), (12), and (14) in Table 5 compare the maximum delay with buffer insertion, and columns (7), (10), (13), and (15) compare buffer counts. Similarly as shown in Table 4, buffer insertion schemes need to be considered carefully when TSV RC comes into the delay computation. Moreover, the buffer delay also needs to be taken into account. The delay of BIS1 and BIS2 (column 12,14) is worse than 'w/o B.I.' (column 11) for small circuits in our simulation because our buffer insertion scheme is not flexible.

6.4 Impact of TSV RC on Power

Table 6 shows total chip power which consists of cell internal

[5]The reversion point is dependent on TSV size, TSV RC, the number of dies, process technology, buffer insertion schemes, etc.

Table 6: Total power (cell power + interconnect power + buffer internal power). unit:W. The ratios of 3D to 2D are shown in the parentheses.

Chip area		2D	3D w/o TSV RC	3D with TSV RC					
				TSV cap. = $5fF$		TSV cap. = $20fF$		TSV cap. = $50fF$	
(mm^2)	# gates	BIS1	BIS1	BIS1	BIS2	BIS1	BIS2	BIS1	BIS2
25.0	$10M$	73.5	63.7(−13.3%)	68.7(−6.53%)	72.4(−1.50%)	78.1(+6.26%)	81.8(+11.3%)	92.3(+25.6%)	96.0(+30.6%)
12.5	$5M$	33.7	30.4(−9.79%)	32.7(−2.97%)	34.5(+2.37%)	37.2(+10.4%)	39.0(+15.7%)	43.9(+30.3%)	45.7(+35.6%)
2.50	$1M$	6.16	4.43(−28.1%)	5.98(−2.92%)	6.27(+1.79%)	6.72(+9.09%)	7.01(+13.8%)	7.82(+26.9%)	8.11(+31.7%)
1.25	$500K$	2.71	2.69(−0.74%)	2.88(+6.27%)	3.02(+11.4%)	3.21(+18.5%)	3.35(+23.6%)	3.71(+36.9%)	3.85(+42.1%)
0.25	$100K$	0.49	0.50(+2.04%)	0.53(+8.16%)	0.55(+12.2%)	0.58(+18.4%)	0.60(+22.4%)	0.65(+32.7%)	0.67(+36.7%)

power, interconnect power, and buffer internal power. We use the power model presented in [10] to estimate interconnect power. Although the total wirelength becomes shorter in 3D ICs, the total power of 3D ICs could be greater than that of 2D ICs due to the non-negligible TSV capacitance and the number of buffers required to drive TSVs.

If we ignore TSV RC, power saving in 3D ICs is huge for medium-size or large circuits (-9% to -28%) because the total wirelength of 3D ICs is much smaller than the total wirelength of 2D ICs. However, if TSV RC is considered, power consumption of 3D ICs becomes bigger than 2D ICs unless TSV capacitance is small as shown in Table 6. Therefore, power consumption of 3D ICs is expected to be greater than 2D ICs in general unless few TSVs are used in 3D ICs or TSV capacitance is small (e.g. less than $2fF$).

6.5 Impact of Buffer Insertion on Silicon Area

Table 7 shows the additional silicon area required for buffer insertion. The additional area for buffer insertion in 2D ICs ranges from 2% for small circuits to 26% for big circuits compared to the original chip area. On the other hand, the additional area for 3D ICs ranges from 20% for small circuits to 40% for big circuits if BIS2 is used. This means that 3D IC is not suitable for too big circuits in terms of additional silicon area required for buffer insertion. Therefore, 3D ICs are suitable for medium or big circuits with respect to silicon area (Table 7), power consumption (Table 6), and the maximum delay (Figure 8) in the current assumptions and parameter settings.

7. FUTURE WORK

In this paper, we assume that the bulk silicon around a TSV is DC-biased well as mentioned in Section 3.2. Therefore we ingore TSV-to-TSV coupling capacitances. However, if the bulk silicon around TSVs is not DC-biased well so that there exists capacitive coupling between two adjacent TSVs, we have to consider TSV-to-TSV coupling capacitances as well as TSV-to-bulk silicon MOS capacitance. We will thoroughly investigate the capacitive coupling phenomena in 3D ICs and bring more accurate TSV capacitance models into our work.

In this work, we use a simple buffer insertion scheme. However, there is a need to use more sophisticated buffer insertion algorithms such as van Ginneken's algorithm for more accurate prediction of delay and power consumption. We will use those algorithms to predict the delay of 3D IC more accurately in the future. Moreover, we will also design physical layouts using 3D placement, 3D routing, and 3D timing optimization so that we can validate the delay and power consumption models presented in this work.

8. CONCLUSIONS

In this paper, we investigated the impact of TSV parasitic RC on delay and power in 3D ICs. For realistic simulation, we use TSV-aware 3D wirelength prediction models, technology-specific parameters, and TSV capacitance based on Raphael simulation. The experimental result shows that TSV capacitance is not negligible, and it affects delay and power of 3D ICs significantly. This effect is not clearly revealed unless we consider buffer insertion. Since the impact of TSV RC on delay and power is not negligible, a 3D design could be worse than a 2D design unless buffers are inserted properly and the TSV count is controlled well. Therefore, proper buffer insertion algorithms for 3D ICs need to be developed considering the non-negligible TSV RC. In addition, TSV-count-aware physical design algorithms for 3D ICs also need to be developed in order to minimize the side-effects of TSV RC.

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