Backend Dielectric Reliability Full Chip Simulator

Muhammad Muqarrab Bashir, Chang-Chih Chen, Linda Milor, Dae Hyun Kim, and Sung Kyu Lim, *Senior Member, IEEE*

***Abstract*— Backend dielectric breakdown degrades the reliability of circuits. A methodology to estimate chip lifetime because of backend dielectric breakdown is presented. It incorporates failures because of parallel tracks, the width effect, and field enhancement due to line ends. It also includes the operating temperature and activity.**

***Index Terms*— Design for manufacture, dielectric breakdown, integrated circuit reliability.**

I. Introduction

EACH technology generation reduces the interconnect dimensions without always reducing the supply voltage in proportion. This results in higher electric fields within the backend dielectric. Simultaneously, as the dielectric constant (k) decreases to reduce parasitics, as prescribed by the International Technology Roadmap for Semiconductors, the porosity of materials must increase, at the possible cost of increasing the vulnerability of materials to breakdown. These factors combine to increase the risk of failure of chips because of backend dielectric breakdown in the newer technology nodes.

To better understand the impact of the backend dielectric on design, this paper builds an interface between data collected by reliability physicists and designers by linking test structure data to chip-level lifetime estimates. In other words, in this paper, the physical and electrical features of a chip are analyzed and combined with known physical wearout models to determine an overall failure rate distribution for a chip. Such an analysis should be performed before tapeout of a chip to minimize the risk of unexpected reliability problems.

It is a common assumption that the vulnerable area for backend dielectric breakdown for a full chip is the area between minimum spaced lines [1]. This paper shows that it is necessary to consider all the areas with different line spaces.

In addition, lifetime is modulated by linewidth, even when the line space is constant, because of aspect ratio-dependent etch. Lifetime is also impacted by irregular geometries due to aspects of advanced lithography. Others have demonstrated dependencies on the presence of vias [2] and line-edge roughness [3].

In this paper, initially, our methodology to estimate lifetime, based on the data collected from test structures, is summarized in the following section. Section III discusses our test structures and vulnerable length, together with all geometric features that are extracted from a chip layout, and the circuit feature extraction algorithm is presented. Test data are presented to assess the impact of layout geometries on lifetime. Section IV summarizes the modeling of operating conditions and temperature. Section V contains case study results, and finally Section VI summarizes the conclusions.

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The authors are with the School of Electrical and Computer Engineering, Georgia Tech, Atlanta, GA 30332 USA (e-mail: muqarrab@gmail.com; changchih@gatech.edu; linda.milor@ece.gatech.edu; daehyun@gatech.edu; limsk@ece.gatech.edu).

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II. Backend Dielectric Breakdown Models and Simulation

The most important reliability concerns for interconnects are electromigration, stress-induced voiding, and time-dependent dielectric breakdown (TDDB) of the backend dielectric. Our purpose is to consider time-dependent backend dielectric breakdown. This paper focuses on intralayer backend dielectric breakdown, because the intralayer distances are smaller than the interlayer distances. Interlayer breakdown, however, can also be an issue, although a lesser one.

A. TDDB Models

Models of backend TDDB are of the form [4]–[7]

$$\ln \mathrm{TF} = A - \gamma E^m \quad (1)$$

where A is a constant that depends on the material properties of the dielectric, γ is the field acceleration factor, m is one for the E model and 1/2 for the $E^{1/2}$ model, and TF is the time-to-failure. The field acceleration factor, γ, is a function of temperature [8]. Equation (1) provides a correction between the electric field during the use conditions and accelerated stress tests.

Test structures are stressed with dc stress, whereas chip dielectrics undergo ac stress. If two signals are switching with a 50% duty cycle, the dielectric between the signals is stressed 50% of the time. Fig. 1 shows scaling to use conditions for 45-nm technology, with a supply voltage of 0.8 V for a dielectric that is stressed 50% of the time. In addition to the fact that geometries with different line spacings scale differently to use conditions, it should be noted that the field acceleration factor strongly impacts the estimate of lifetime at use conditions. Specifically, circuits are required to achieve a fixed lifetime, 10 years, under use conditions. Because it is not possible to evaluate a circuit's lifetime under use conditions, as this would take 10 years, circuits and test structures are stressed at high voltages. The field acceleration parameter determines the relationship between a lifetime obtained when a high voltage test is conducted versus the lifetime when operating with the nominal supply voltage.

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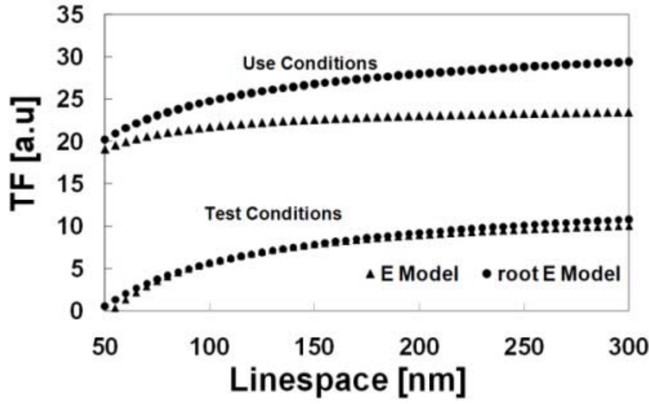

Fig. 1. Scaling of test results to use conditions.

Time-to-failure is also a function of temperature, modeled with an Arrhenius relationship [6]

$$ln\mathrm{TF} = B - E_a/T \tag{2}$$

where B is a constant and is an activation energy that depends on electric field. Equation (2) provides a correction between chip operating conditions and accelerated temperature stress conditions. There is a concern that stressing at high temperatures can activate failure modes that are not present during use conditions. Hence, stressing at high electric fields is preferred in comparison with testing at high temperatures. Our tests were conducted at 150 °C.

B. Chip Lifetime Models

It should be noted that circuits wearout for a variety of reasons, both related to devices and interconnect. All of these wearout mechanisms happen simultaneously. It is common to describe reliability mechanisms with a Weibull distribution

$$P(\mathrm{TF}) = 1 - \exp\left(-\left(\mathrm{TF}/\eta\right)^{\beta}\right) \tag{3}$$

having two parameters: 1) the characteristic lifetime, η, and 2) the shape parameter, β. The characteristic lifetime is the time-to-failure at the 63% probability point, when 63% of the population have failed, and the shape parameter describes the dispersion of the failure rate population. Typically, the shape parameter is close to one.

To test the lifetime of a specific wearout mechanism and circuit geometry, several samples of a test structure containing that feature are tested and the time-to-failure for each sample is recorded. The resulting data are fit with a Weibull distribution. To fit the data with a Weibull distribution, it is necessary to estimate η and β. To do this, we order that time-to-failure data from smallest to largest, i.e., $\mathrm{TF}_1, \ldots \mathrm{TF}_n$, for n data points. Probabilities, $P_i \epsilon [0, 1]$, are assigned to each data point, by partitioning the probability scale equally, i.e., $P_i = (2i - 1/2n)$, $i = 1, \ldots, n$. The pairs $[\ln(\mathrm{TF_i}), \ln(-\ln(1 - \mathrm{P_i}))]$ are plotted. η_t is the x-intercept and β_t is the slope.

Given a collection of n independent wearout mechanisms modeled with Weibull distributions, having parameters, $\eta_i, i = 1, \ldots, n$, and $\beta_i = i = 1, \ldots, n$, then the characteristic lifetime of the system, η_{chip}, i.e., the time when 63% of the population have failed from any mechanism, is the solution of [9]–[11]

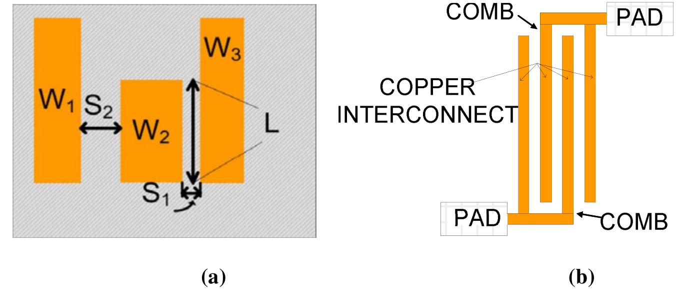

Fig. 2. (a) Vulnerable length, L, associated with a line space. The rectangles are Cu wires, surrounded by the backend dielectric. (b) Top view of a comb test structure.

$$1 = \sum_{i=1}^{n} \left(\eta_{\mathrm{chip}}/\eta_i\right)^{\beta_i}. \tag{4}$$

Similarly [10]

$$\beta_{\mathrm{chip}} = \sum_{i=1}^{n} \beta_i \left(\eta_{\mathrm{chip}}/\eta_i\right)^{\beta_i}. \tag{5}$$

The components in (4) and (5) could be different wearout mechanisms, different layers of a chip, different geometries within a layer, or different geometries within a layer at different temperatures. Hence, a reliability simulator has to: 1) determine the characteristic lifetimes and shape parameters for all of the underlying wearout mechanisms and geometries, after all the components are scaled for temperature and to use conditions with (1) and (2) and 2) apply (4) and (5) to solve for η_{chip} and β_{chip}.

Note that if the dielectric segments fail based on a Weibull distribution, the system may not fail according to a Weibull distribution if the parameters of the underlying components vary widely. Equation (4) provides the lifetime of the system when 63% have failed, the Weibull characteristic lifetime. If all the dielectric segments fail according to a Weibull distribution, then for an arbitrary probability of failure, P, the time-to-failure, $\mathrm{TF}_{\mathrm{chip}}$, is the solution of the following:

$$-ln(1 - P) = \sum_{i=1}^{n} \left(\mathrm{TF}_{\mathrm{chip}}/\eta_i\right)^{\beta_i}. \tag{6}$$

Similarly, (5) provides the slope of the Weibull curve at the x-intercept (63% failures). The slope at other probabilities of failure may be different.

III. Determining the Impact of Backend Geometries

A. Vulnerable Length and the Test Structures

The simulator operates by determining the vulnerable length of the chip layout and the corresponding test structure. The vulnerable length is the length, L_i, of lines associated with a line space S_i, shown in Fig. 2(a). Dielectric lifetime for line space, S_i, is also a function of the widths of the two adjacent lines, W_{iL} and W_{iR}. A given layout is analyzed by

determining the pairs $[S_i(W_L W_R), L_i]$ for each layer for all line spaces surrounded by the linewidths W_L and W_R.

Test structures that vary area, line space, and linewidth have been implemented [9]–[13]. Fig. 2(b) shows a top view of a comb test structure used in this paper. The test structure in Fig. 2(b) is used to determine the lifetime of the dielectric between parallel tracks with a specific line space, S. This test structure has a fixed line space, S, and vulnerable length, L. To test the lifetime of such a feature, a voltage difference is applied between the two combs. The current between the combs is monitored to determine the time-to-failure. The data set from several samples is fit with a Weibull distribution to estimate η_t and β_t.

Because the features on a chip differ from a test structure layout, area scaling must be performed to adjust the lifetime to consider the difference in vulnerable area between the chip and the test structure. To do this, let L_t and L_i be vulnerable lengths of the test structure and chip, i.e., the length of the lines that run in parallel in the test structure and chip, respectively, with the same line space, S. η_t is determined by stressing a test structure with line space S and vulnerable length L_t. Then, the corresponding characteristic lifetime for that feature in the chip is

$$\eta_i = \eta_t \left(L_t / L_i\right)^{1/\beta}. \tag{7}$$

Test structures with four areas, 1X, 3X, 4.5X, and 9X, have been implemented. Test structures with different widths and a fixed line space have also been implemented. Fig. 3(a) versus (b) shows top views of test structures with different linewidths. The width ratios are 1X, 3X, and 5X. To distinguish between the density and linewidth effect, a test structure, where the width of the lines for one comb is 1X and the other is 5X is included. The density of this test structure matches that of the 3X width test structure. The top view of this test structure is shown in Fig. 3(c).

Our study has included test structures that have several irregular features to determine any impact of field enhancement. Fragments of these test structures are shown in Fig. 4. Top views of these test structures are shown in Figs. 3(d)–(h). PTT emphasizes the electric field between parallel routing tracks that end at the same point. TLa and TLb emphasize the electric field between line ends and perpendicular lines. TLb includes additional fringing fields, because the line ends are more widely spaced. TTa and TTb emphasize electric fields between line ends. In TTa, the line ends abut, and in TTb, the line ends are in parallel tracks. TLa, TLb, TTa, and TTb have 528 line ends each. The separation between line ends is the same for all test structures.

To account for irregular features, the counts of the irregular features are extracted from the circuit layout. Each adds additional parameters, η_{PTT}, β_{PTT}, $\eta_{\mathrm{TLa/b}}$, $\beta_{\mathrm{Tla/b}}$, η_{Tta}, β_{Tta}, η_{TTb}, and β_{TTb} to (4) and (5). These parameters depend on the number of minimally spaced line ends in each category of the layout. Let us consider the computation of $\eta_{\mathrm{Tla/b}}$ for the sake of illustration. Let us suppose the test structure has N_{test} minimally spaced line ends, from which η_{test} and $\beta_{\mathrm{Tla/b}}$ are computed from the data collected from a set of tests. Then,

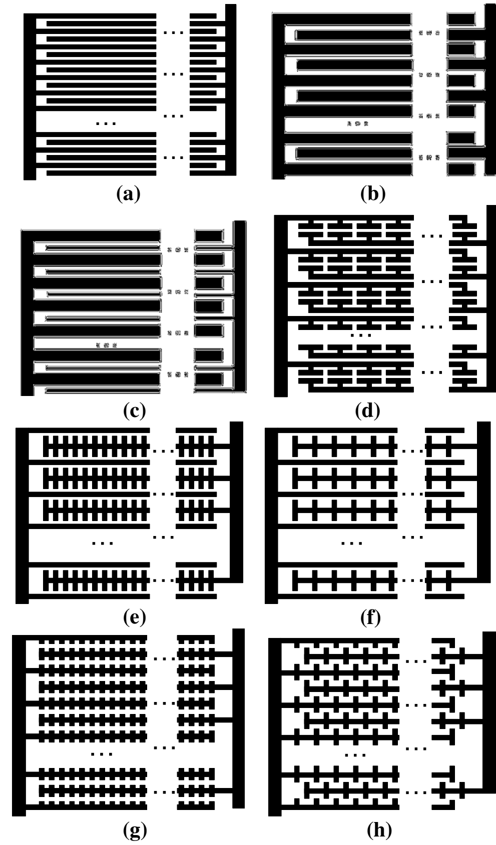

Fig. 3. Top views of comb test structures to characterize the impact of geometry on TDDB. (a) Standard comb structure. (b) Comb structure with wide lines. (c) Comb structure with both wide and narrow lines. (d) PTT. (e) TLa. (f) TLb. (g) TTa. (h) TTb.

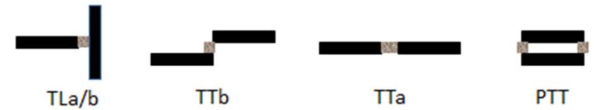

Fig. 4. Vulnerable line ends that need to be extracted from a layout.

for a layout with N_{chip} similar line ends, by area scaling

$$\eta_{\mathrm{Tla/b}} = \eta_{\mathrm{test}} (N_{\mathrm{test}} / N_{\mathrm{chip}})^{1/\beta_{\mathrm{TLa/b}}}. \tag{8}$$

B. Vulnerable Length and Feature Extraction

The layout extraction tool was developed using a standard object-oriented programming language.

Vulnerable area and features are extracted by comparing pairs of lines in a layout. Because tens of millions of lines exist in each metal layer in a layout, it is necessary to find the adjacent lines that border a vulnerable area or form a critical feature quickly. Therefore, vulnerable area and features are extracted as shown in Algorithm 1.

Initially, lines are read from a layout, sorted by the bucket sort algorithm, and stored in two separate data variables, LineDataX and LineDataY. The lines in LineDataX (and LineDataY) are sorted in ascending order of the x-coordinate (y-coordinate) of the bottom left corner of the line. If two lines have the same x-coordinate (or y-coordinate), they are sorted in the ascending order of the y-coordinate (or x-coordinate)

Algorithm 1 Layout Extraction Flow

Input: The maximum line spacing S_{max} and a layout L
Output: Tables of vulnerable lengths (VulnerableLengthTable) and new features (TLab, TTa, TTb, PTT)

```
for each metal layer m do
  LineDataX (m) ← ReadLines (L); // BucketSort
  LineDataY (m) ← ReadLines (L); // BucketSort
  TTa (m) ← 0; TTb (m) ← 0; PTT (m) ← 0; TLab (m) ← 0;
  c ← 1;
  n ← 2;
  while c<N_line do // N_line: # lines in LineDataY
    L1 ← LineDataY (m,c); // c-th line
    L2 ← LineDataY (m,n); // n-th line
    if Spacing (L1, L2)<=S_max then
      TLab (m) += CheckTLab (L1, L2); // check TLab between L1 and L2
      TTa (m) += CheckTTa (L1, L2); // check TTa between L1 and L2
    end
    n ← Adjust (c, n);
    L2 ← LineDataX (m,n);
    if Spacing (L1, L2)<=S_max then
      TLab (m) += CheckTLab (L1, L2); // check TLab between L1 and L2
    end
    n ← Adjust (c, n);
    L2 ← LineDataY (m,n);
    if Spacing (L1, L2)<=S_max then
      PTT (m) += CheckPTT (L1, L2); // check PTT between L1 and L2
      TTb (m) += CheckTTb (L1, L2); // check TTb between L1 and L2
      VulnerableLengthTable (m) ← VulnerableLength (L1, L2);
      LineDataY (m) ←Split (L1, L2);
      n ← Adjust (c, n);
    end
    n ← Adjust (c, n);
  end
end
```

of the bottom left corner of the line. The lines with the same x-coordinate (or y-coordinate) are placed in the same bucket.

Then, the extraction process starts by comparing the first (L_1) and the second (L_2) lines in the first bucket of LineDataY. Because each metal layer has a preferred routing direction (horizontal or vertical), the preferred routing direction is assumed to be horizontal in this description. If the y-coordinates of the two lines in the same bucket are the same, they can form TTa or TLa/b, depending on the distance between them and the direction (horizontal or vertical) of L_2. To form TTa or TLa/b, the spacing between L_1 and L_2 must be the minimum distance. If both L_1 and L_2 are horizontal, they can form a TTa feature. If L_1 and L_2 are perpendicular, they can form TLa/b. To find TLa/b, LineDataX is searched based on the x-coordinate of the bottom right corner of L_1 to find any L_2 that can form TLa/b with L_1. If an L_2 has been determined with a critical feature, in addition to L_2, L_1 cannot form any critical features with other lines in the same bucket, because L_2 lies between L_1 and the other lines in the bucket.

TTb and PTT are extracted by comparing two lines in adjacent buckets in LineDataY (lines in different buckets have different y-coordinates). TTb and PTT are checked by comparing L_1 and any L_2 in the next bucket. If a TTb or PTT is found, a flag for the corresponding edge of L_1 is set. By setting the flag, counting an extra TTb or PTT formed by L_1 and any other line L_3, is avoided, because there may be other lines, L_3, that have the same x-coordinate as L_2 and that are within the minimum distance. TLa/b can also be found by comparing lines in adjacent buckets, if L_2 is perpendicular to L_1.

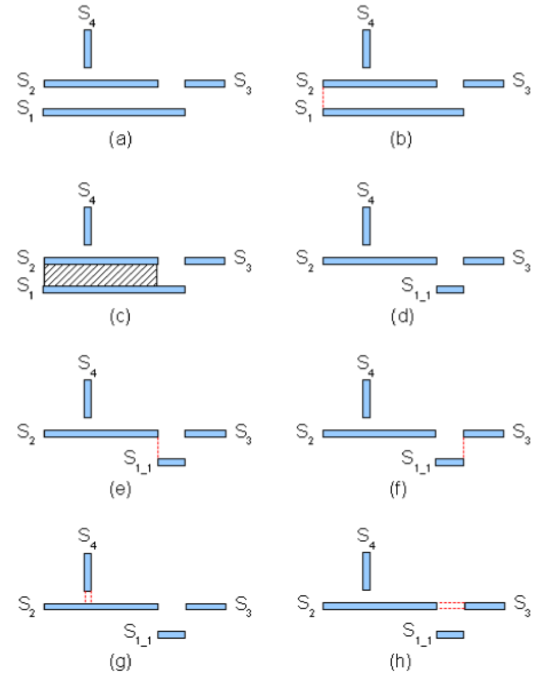

Fig. 5. (a) Initial line structure. (b) PTT between S1 and S2. (c) Vulnerable length between S1 and S2. (d) Postprocessing after vulnerable area extraction. (e) TTb does not exist between S1_1 and S2. (f) TTb between S1_1 and S3. (g) TLa/b between S2 and S4. (h) TTa between S2 and S3.

After extracting irregular features formed by L_1 and its adjacent lines, the algorithm searches for a vulnerable length associated with L_1. To form a vulnerable length, L_2 must be in a different bucket. L_2 is the first line in the sorted list where the area between the x-coordinates overlaps. If the vertical spacing is less than or equal to the maximum line spacing, a vulnerable area surrounded by these two lines exists. The line space is computed, and the vulnerable length is added to the vulnerable length table for the corresponding line space. Then, L_1 is split into one or two new lines; they are inserted into LineDataY; and L_1 is removed from LineDataY.

Fig. 5 shows an example with four line segments, S_1, S_2, S_3, and S_4. They are ordered according to their bottom left coordinate. The algorithm starts with the first line segment, S_1. Initially, the irregular features are checked. In checks for irregular features, the algorithm looks for specific geometries that are within a minimum distance from S_1. Hence, for S_1 PTT, TTa, TTb, and TLa/b are checked. The TTa geometry only appears if the segments are on the same track. TLa/b is a check for a perpendicular geometry. PTT and TTb appear if the line ends line up. The PTT geometry is found between S_1 and S_2, as shown in Fig. 5(b). Next, the vulnerable length between S_1 and S_2 is extracted in Fig. 5(c). Because there exists a vulnerable length, it is stored in the vulnerable length table. Then, the split process is applied. S_1 is split into two segments, and the part of the S_1 segment included in the extracted vulnerable area is removed. In this example, only one new line (S_{1-1}) is created because the left boundaries of S_1 and S_2 are aligned, as shown in Fig. 5(d).

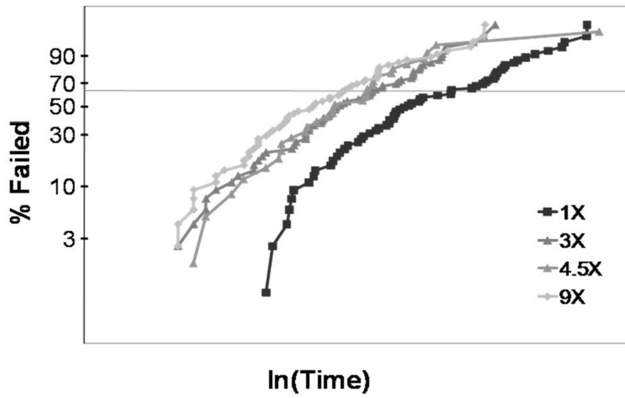

Fig. 6. Weibull plot of time-to-failure for comb test structures with four areas: 1X, 3X, 4.5X, and 9X.

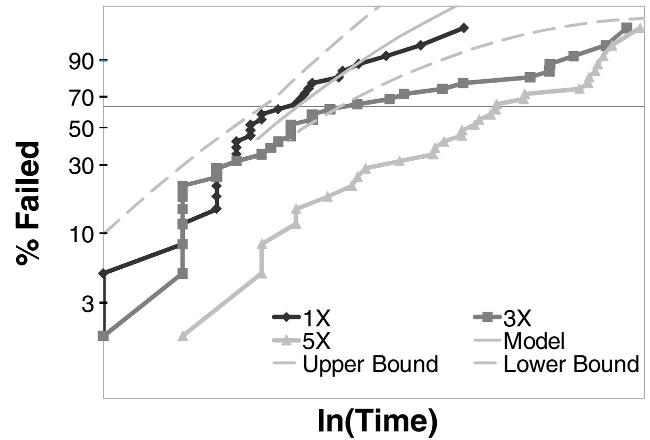

Fig. 7. Weibull plot of the time-to-failure distributions for test structures with 1X, 3X, and 5X linewidths. 90% confidence bounds are included for the 1X test structure.

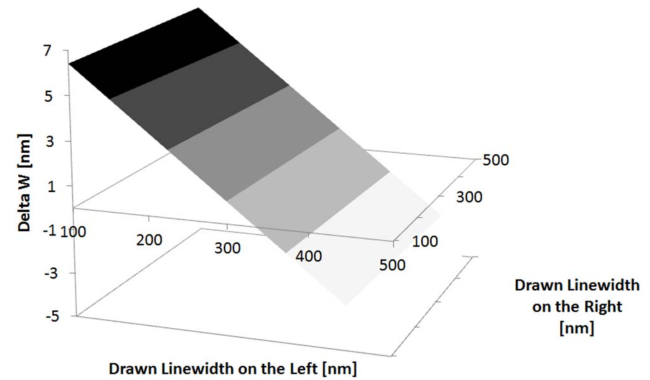

Fig. 8. Variation in line space as a function of the widths of the lines on either side of the vulnerable dielectric. The data were collected using SEM and were fit with regression.

After inserting S_{1-1} into LineDataY, L_1 is set to S_{1-1} and the extraction process is repeated. The algorithm checks for PTT, TTa, TTb, and TLa/b between S_{1_1} and other lines. Although there exists a TTb relation between S_{1_1} and S_2, as shown in Fig. 5(e), it is not included in the TTb count, because the left side of S_{1_1} was generated during the split operation. On the other hand, the right side of S_{1_1} is the right side of the original line S_1, and there exists a TTb relation between S_{1_1} and S_3, as shown in Fig. 5(f). Hence, the TTb count is incremented. S_{1_1} does not have a minimum distance with any other line segment. It does not have a vulnerable area either. Therefore, the algorithm proceeds to the next line S_2. L_1 is set to S_2 by the index adjustment function. The algorithm checks for irregular geometries that are separated from S_2 by the minimum distance. It finds a TLa/b relation between S_2 and S_4, as shown in Fig. 5(g). It also finds a TTa relation between S_2 and S_3 in Fig. 5(h). The TLa/b and TTa counts are incremented.

The runtime for the simulator is the sum of the time taken to extract features from the layout and a constant time to evaluate equations (4) and (5). Complexity of feature extraction is $O(n)$, where n is the number of features, because bucket sort is used. Complexity of extracting statistics from features is also $O(n)$, because the bucket is scanned from the bottom most element, and the maximum number of features within a fixed distance from an element is constant. Lifetime is estimated in a constant time.

C. Test Results

Test results show a strong impact of area, as illustrated in Fig. 6. Die-to-die linewidth variation creates curvature in failure rate distributions [13]. This curvature does not impact η. Hence, initially, η is extracted and then used to determine β by area scaling [14]. Specifically, β is determined by finding the best fit of slope of ordered pairs, $[ln\eta_{NX} - ln\eta_{1X}, ln(1/N)]$ where N is the area ratio, i.e., two if the area is 2X larger than the reference 1X. Once η_{1X} and β are known, the failure rate distribution is known for all areas. For instance, $\eta_{NX} = \eta_{1X} + \ln(1/\mathrm{N})/\beta$.

Line edge roughness impacts both the circuit and the test structures, and therefore it is considered.

Lifetime is also impacted by the linewidth on each side of the dielectric segment. Fig. 7 shows the failure rate distributions for the test structures with 1X, 3X, and 5X linewidths, with fixed line space.

These test results show a strong impact of linewidth, when the line space remains constant. Note that the test structures in Fig. 7 simultaneously vary density and linewidth. Compare, for example, Fig. 3(a) and (b). To isolate the cause of variation, our test structure set also includes a test structure that varies linewidth independently of density, as shown in Fig. 3(c) [10], [12]. It was found that linewidth, rather than density, determines the lifetime. ARDE [15], [16], where narrow trenches suffer from greater lateral etch near the critical CMP interface and a less vertical sidewall profile, can explain such a trend.

Scanning electron microscopy (SEM) data were used to determine the difference between the actual linewidth, W_a, and the drawn linewidth, W_d, i.e., $\Delta W = W_a - W_d$. This translates into a shift in line space, i.e., $S_a = S_d - \Delta W$, where S_a is the actual line space and S_d is the drawn line space. Line spaces with larger positive values of ΔW breakdown faster, because $E = V/S_a$. A model based on SEM data was used to determine ΔW, by fitting measured data through regression, as shown in Fig. 8.

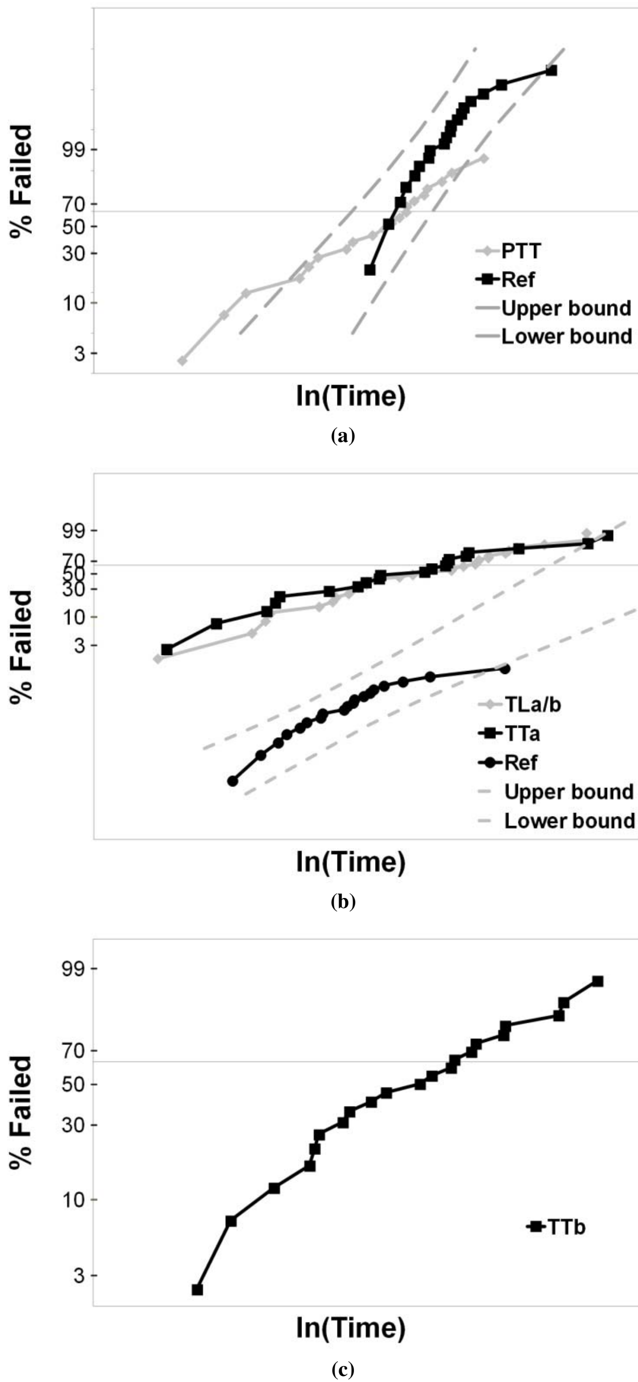

Fig. 9. Data collected from (a) PTT versus the reference structure, (b) TLa, TLb, and TTa versus the reference structure, and (c) TTb confidence bounds are included for the area scaled reference test structure.

The line end features in Fig. 4 were also found to have a significant impact on lifetime. The data collected from the test structures are presented in Fig. 9. An area-scaled version of a standard comb test structure is included for comparison. It can be observed that all the test structures (PTT, TLa, TLb, TTa, and TTb) result in a significantly reduced lifetime in comparison with the reference test structure. The data also show that TLa and TLb fail at the same rate, showing that fringing fields are not significant. The data from these two test structures can be merged to determine a single model. TTa has an improved lifetime, in comparison with TLa/b. No reference curve is included for comparison for TTb because TTb has no vulnerable length.

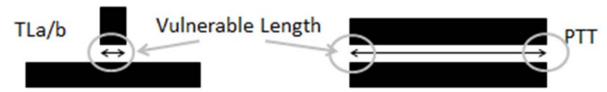

Fig. 10. Vulnerable length and line ends extracted from test structure TLa/b and PTT. The vulnerable length is represented with arrows and the line ends are represented with circles.

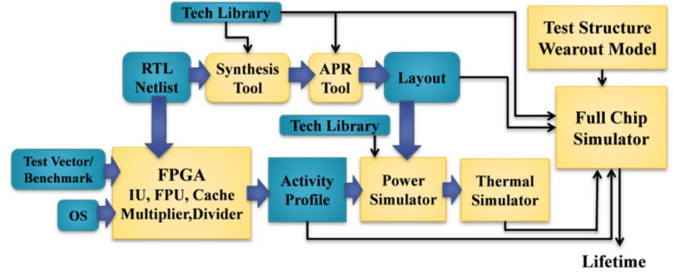

Fig. 11. Flow for extracting electrical and thermal profiles.

A model was extracted for PTT, TLa/b, TTa, and TTb. The model for TTa and TTb was found with the standard method, involving fitting a linear function to the data to find η_{TTa}, β_{TTa}, η_{TTb}, and β_{TTb}.

Extraction of the model for TLa/b and PTT is more complex, because these structures combine both line ends and vulnerable length. Fig. 10 shows one TTa/b line end and two PTT line ends, together with the vulnerable length extracted. If we find $\eta_{\mathrm{TLa/b}}, \beta_{\mathrm{TLa/b}}, \eta_{\mathrm{PTT}}$, and β_{PTT}, by fitting a linear function, then the model would include both the impact of the line ends and the vulnerable length. For circuit analysis purposes, it is necessary to eliminate the effect of vulnerable length to create a model for line ends only. To find the model for line ends, it is necessary to subtract the effect of vulnerable length. Details of the methodology are presented in [17].

IV. Determining the Impact of Operating Conditions

Because backend dielectric breakdown is activity and temperature dependent, our methodology includes determining the temperature and stress for each dielectric segment while running benchmarks. A framework for acquisition of spatial and temporal thermal/electrical stress of the system was constructed. Fig. 11 shows the electrical and thermal profile acquisition flow.

For activity tracking, the hardware RTL/netlist was synthesized for emulation on an FPGA, and counters were placed at the I/O ports, which track both the state probabilities and the toggle rates of the ports during application runtime, as shown in Fig. 12. A standard set of benchmarks was used as the applications for analysis [18].

The I/O activities and the gate-level netlist were then used for activity propagation to each net in the design, for a complete stress/transition probability profile of the internal

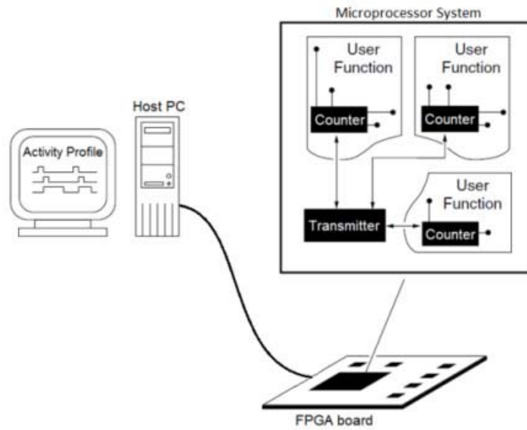

Fig. 12. System to collect the activity profile of a microprocessor.

nodes of a circuit under study. This provides the probability of a transition occurring at any node and the probability at each state, i.e., the probability at logic 1. It is this probability at logic 1 and 0 that is needed to compute the probability that each dielectric segment is under stress. The probability of dielectric stress of each dielectric segment is determined by

$$\alpha = \alpha_1(1 - \alpha_2) + \alpha_2(1 - \alpha_1) \tag{9}$$

where α_1 and α_2 are the probabilities that each net in the pair of nets that border the dielectric segment is at logic 1. If η_{dc} is the characteristic lifetime under dc stress, then the characteristic lifetime under ac stress, η_{ac}, is

$$\eta_{ac} = \frac{\eta_{dc}}{\alpha}. \tag{10}$$

The netlist is also used for layout generation. The RC information from the layout, together with the net activity, is used for extraction of the power profile and the consequent thermal profile, through the power simulator [19] and the thermal simulator [20].

Note that computational complexity in accounting for operating conditions is dominated by the complexity to propagate activities within a circuit block, which is $O(n)$, where n is the number of gates in the system. Hence, the overall complexity of the simulator is $O(n)$.

To illustrate the fact that the electrical and thermal stress are not constant, the well-known open-source LEON3 IP core processor with super scalar abilities [21] was considered. Fig. 13 shows the average temperature distribution while running one of the standard benchmarks [18]: bitcnts. Fig. 14 shows the electrical stress distribution. The distribution of electrical stress is shown in Fig. 15.

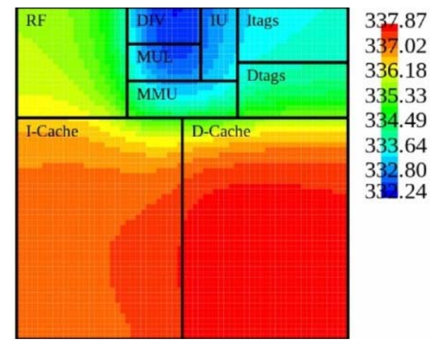

Fig. 13. Average temperature distribution for the microprocessor while running the bitcnts benchmark.

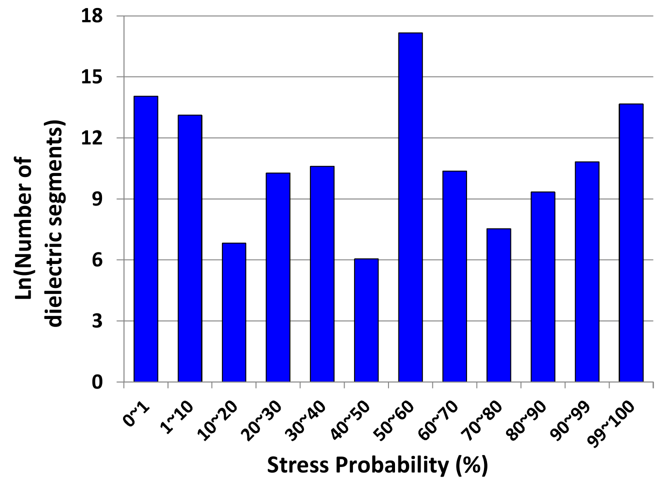

Fig. 14. Stress profile of the dielectric segments in the microprocessor while running the bitcnts benchmark.

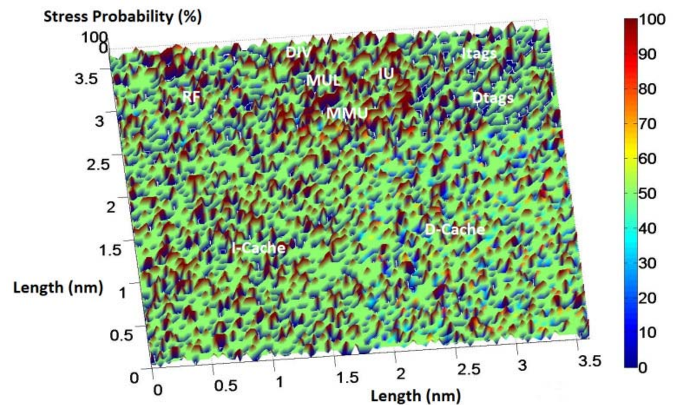

Fig. 15. Distribution of the stress probability for the microprocessor while running a standard benchmark.

V. Case Studies

In this paper, we have considered two case studies: a set of fast Fourier transform (FFT) circuits [22] with different layouts and the LEON3 IP core processor. The FFT circuits were used to study the impact of circuit geometries on dielectric lifetime, whereas the microprocessor was used to study the impact of blocks. The study of the smaller FFT circuit allows us to vary the layout and determine the impact of different geometries and design parameters during circuit synthesis, whereas the larger LEON3 circuit allows us to incorporate the impact of activity and temperature and allows us to check some of our conclusions with a larger circuit.

A. FFT Circuits

Several versions of a radix-2, 256-point and 512-point FFT circuit were synthesized and implemented with the NCSU

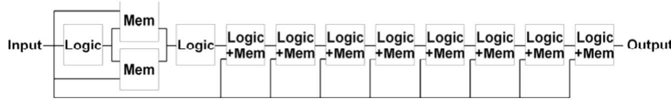

Fig. 16. Block diagram of the FFT circuit.

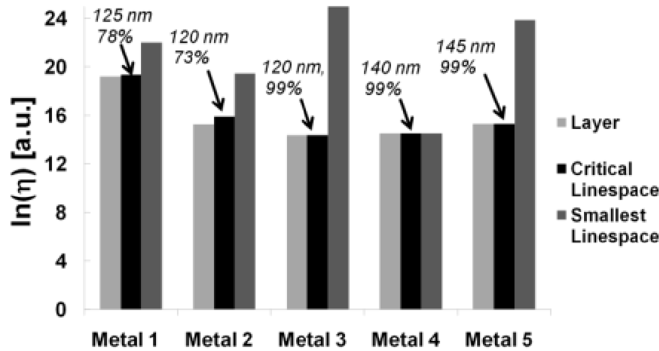

Fig. 17. Characteristic lifetime for each layer, considering all line spaces, the critical (most frequent) line space only, and the smallest line space (in the given layer). The percentage of features with the critical line space is also noted.

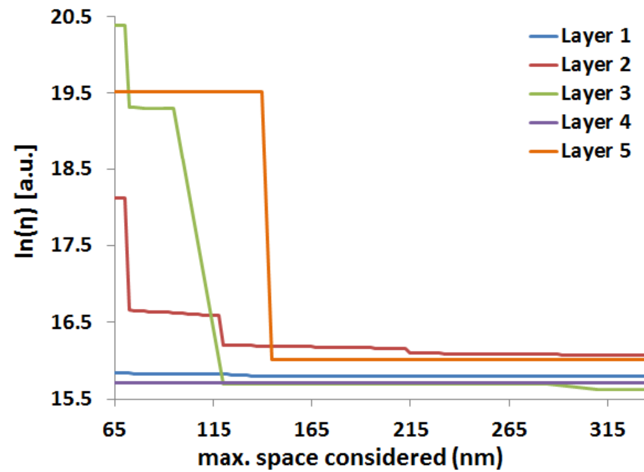

Fig. 18. Characteristic lifetime for each layer as a function of the maximum line space considered in the calculation of characteristic lifetime.

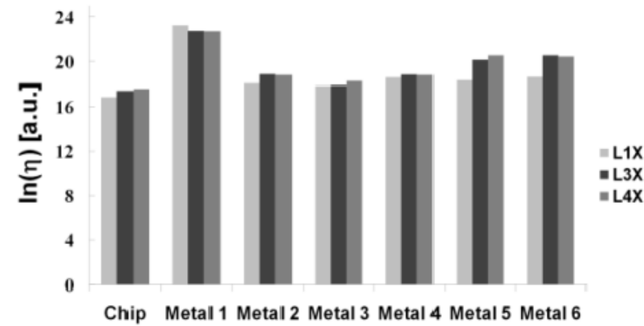

Fig. 19. Characteristic lifetime for different instantiations of the FFT8 chip. The Metal 3 linewidth of L3X and L4X is three and four times the linewidth of L1X, respectively.

45-nm technology library [23]. The block diagram is shown in Fig. 16. The 256-point circuit has 324-k gates and 329-k nets, and the 512-point circuit has 708-k gates and 712-k nets. The number of layers used in routing varied from five to eight. Using more routing layers results in shorter wirelength and better timing performance. Timing was optimized using buffer insertion and gate sizing.

Synopsys design compiler was used for synthesis. Cadence SoC encounter was used for placement, clock-tree synthesis, routing, optimization, *RC* extraction, and static power analysis. Synopsys PrimeTime was used for timing analysis.

1) Critical Physical Features: The characteristic lifetime for chips is more pessimistic than the characteristic lifetime for individual layers, because the characteristic lifetime for the chip combines the vulnerable areas for all the layers.

Fig. 17 shows the characteristic lifetime for each layer. It contains three estimates of lifetime: 1) an estimate that takes all line spaces into account; 2) an estimate that takes only the smallest line space into account; and 3) an estimate that takes only the critical line space into account. The critical line space for each layer is defined as the most frequent line space in the layout. It is not necessarily the smallest line space. As shown in Fig. 17, the characteristic lifetime for a layer is dominated by the contribution of dielectric in the critical line space group. Fig. 17 also shows the percentage of dielectric area formed by the critical line space group.

Fig. 17 also shows the characteristic lifetime computed based on only the minimum line space for each layer. The chart shows that when a layout is dominated by a line space other than the minimum line space, lifetime estimates can be optimistic by the orders of magnitude. Metal 2 contains 40 different line spaces, ranging from 70 to 252.5 nm. The smallest line space in Metal 2 is 70 nm, but the line space dominating the characteristic lifetime for this layer is 120 nm; 73% of the dielectric segments in this layer have a line space of 120 nm, whereas only 0.11% have a line space of 70 nm. Fig. 18. shows the lifetime per layer as a function of the maximum line space considered.

The layers with the highest wire density dominate the lifetime. Higher wire coverage is achieved by closely packing the metal lines together, increasing electric field, and consequently degrading reliability.

2) Linewidth: Linewidth impacts lifetime. Test structure results show that lifetime improves as linewidth increases, because of the interaction between physical design and etching. Several layouts were generated, labeled L1X, L3X, and L4X. L3X and L4X have Metal 3 that is three and four times wider than the linewidth of Metal 3 in L1X. Fig. 19 shows that increasing the line width design rule does not improve lifetime significantly, because the overall dielectric area increases after rerouting. The increase in lifetime for all layers can be attributed to a change in the routing for all layers because of the smaller number of routing tracks in Metal 3.

3) Irregular Geometries: Fig. 20 shows the characteristic lifetime results with and without the inclusion of degradation in lifetime because of irregular features, i.e., PTT, TLa/b, TTa, and TTb. The impact of irregular features is strongest for Metal 1. This is because the number of irregular geometries decreases from Metal 1 to 5, because of routing restrictions associated with higher layers of metal.

Fig. 20. Lifetime for individual layers of an FFT circuit considering only the dielectric between parallel lines (gray) and also considering the irregular features (black).

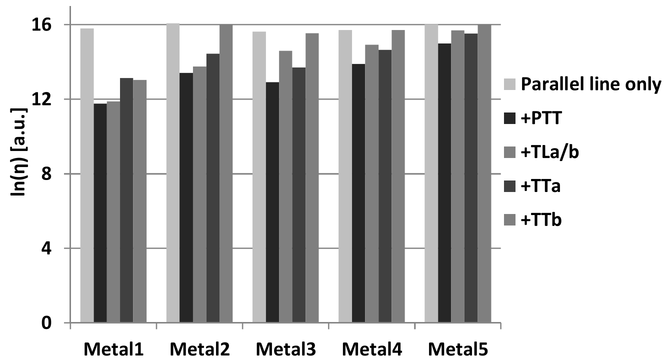

Fig. 21. Characteristic lifetime for individual layers of an FFT circuit considering only the dielectric between parallel lines and considering the impact of each irregular geometry separately.

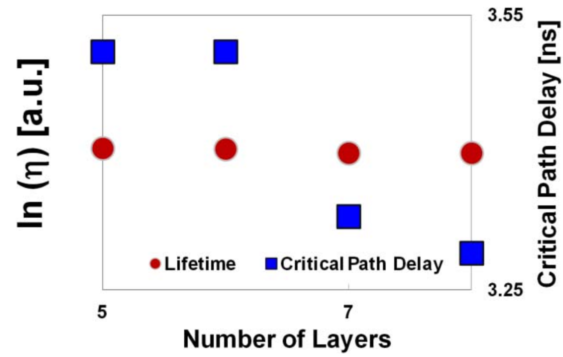

Fig. 22. Lifetime and critical path delay as a function of the number of layers.

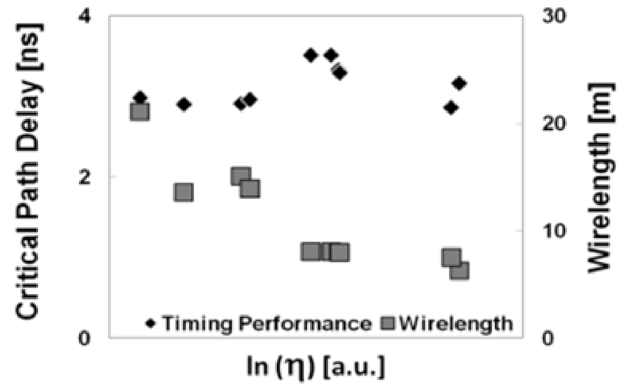

Fig. 23. Comparison of lifetime, timing performance, and wirelength.

Fig. 21 shows the impact of each of the irregular features. The irregular geometry that most strongly impacts lifetime is PTT. This is because there are numerous PTT geometries on Metal 1 and above. On the other hand, TTb geometries rarely (or never) occur above Metal 1, and there is a negligible impact of these geometries. TLa/b geometries essentially consist of two perpendicular wires. In general, each metal layer has a preferred routing direction, either horizontal or vertical. Perpendicular wires are usually not allowed for global routing. Therefore, TLa/b geometries above Metal 1 are rare. TLa/b geometries were, however, frequently found on Metal 1, because Metal 1 is used in cell libraries for internal wiring.

4) Timing and Wirelength: Using more metal layers generally results in a decrease in routing congestion, eliminating the need for long detours to avoid routing congestion. This leads to less coupling capacitance between wires and reduces the critical path delay. Because a router can spread out wires in several metal layers, this is expected to improve lifetime.

As expected, the critical path delay decreases as the number of metal layers increases, as shown in Fig. 22. Fig. 22, also shows, however, that lifetime increases only marginally as the number of layers increases. This lack of improvement in lifetime as a function of the number of layers can be explained because, even though the number of layers increases from five to eight, the percentage of total wirelength in the additional layers is $< 6\%$. A large percentage of total wirelength remains in a single layer, Metal 3. Metal 3 has mid-distance interconnects performing vital operations.

By varying layout parameters, we can study the relationship between lifetime and wirelength and critical path delay. There is a strong correlation between total wirelength and lifetime. This is shown in Fig. 23.

Timing optimization is achieved through buffer insertion, changing gate locations, and gate sizing. Buffer insertion results in an increase in total wirelength, resulting in a decrease in lifetime. Hence, buffer insertion can degrade lifetime. If gate sizing is used for timing optimization, then the goals of timing align with those of reliability. Increasing the gate size increases the degrees of freedom for wire-to-pin connections, and this can enable improved reliability. Ripup and rerouting are aimed at reducing wiring congestion and coupling capacitance. Areas with high coupling capacitance are also likely to be associated with lower lifetimes. Hence, ripup and rerouting for coupling capacitance can improve lifetime. Overall, despite all of these factors, we did not observe any relationship between timing and lifetime, as a result of varying the layout and synthesis parameters, as shown in Fig. 23.

B. Microprocessor Circuit

The well-known open-source LEON3 IP core processor with superscalar abilities was studied. The microprocessor logic units consist of a 32-bit general purpose integer unit,

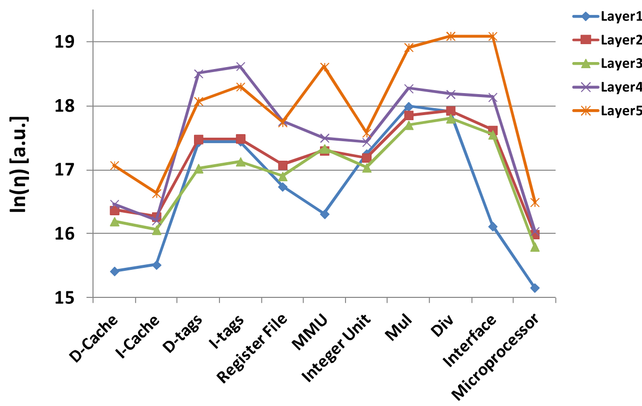

Fig. 24. Characteristic lifetimes for each layer and for each unit of the microprocessor system while running the bitcnts benchmark.

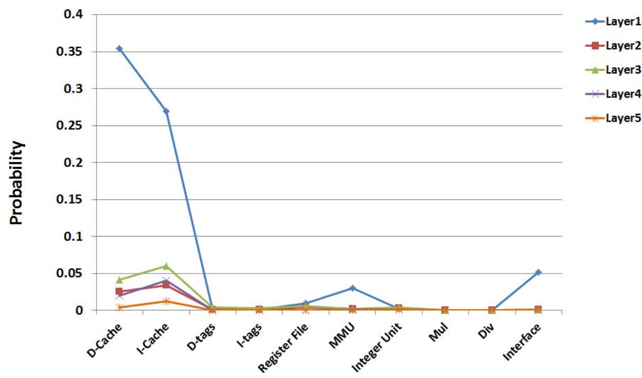

Fig. 25. Probability of first failure for each layer and each unit of the microprocessor system while running the bitcnts benchmark.

a 32-bit multiplier (MUL), a 32-bit divider (DIV) and a memory management unit (MMU). Storage blocks include a window-based register file unit, separate data (D-cache) and instruction (I-cache) caches and cache tag storage units (Dtags and Itags). The microprocessor includes around 20–25-k gates.

The electrical and thermal profiles from Section IV, together with the lifetime models from Section II, were used to estimate the lifetime of each functional unit in the system, as shown in Fig. 24 for the bitcnts benchmark.

The lifetime of the system under study is clearly limited by the Metal 1 layer. Higher metal layers are associated with increased metal spacing, resulting in an increase in time-to-failure. The data- and the I-cache are the lifetime limiting units in the microprocessor. Online reconfiguration, through redundancy allocation, was not considered here, but could improve the lifetime of these units. Among the combinational blocks, lifetime is limited by the MMU, whereas the MUL and the DIV blocs had relatively better lifetimes. Figs. 13 and 24 clearly suggest a strong temperature dependence of the system lifetime.

If we aim to prioritize efforts to improve lifetime, it is helpful to find the probability that each block will fail first. This is shown in Fig. 25. The graph shows that most failures will happen in Metal 1 in the D-cache or I-cache. The equations used for Fig. 25 are in Appendix A.

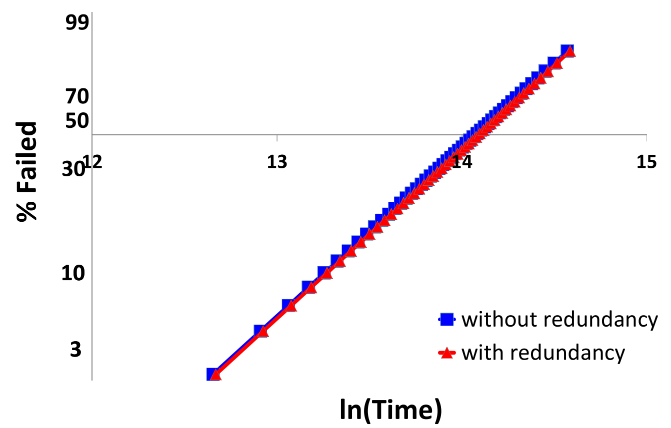

Fig. 26. Microprocessor wearout distribution with and without redundancy using the Weibull scale.

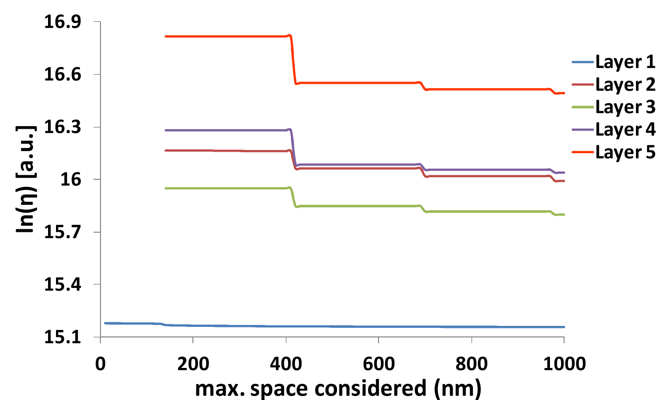

Fig. 27. Microprocessor characteristic lifetimes for each layer as a function of the maximum line space considered.

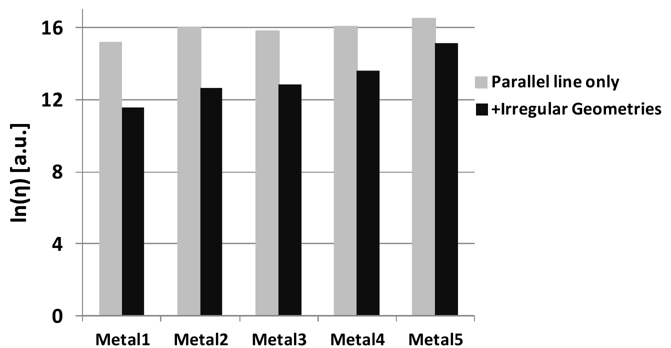

Fig. 28. Microprocessor characteristic lifetimes for each layer considering only the dielectric between parallel lines (gray) and considering also the dielectric involved in irregular geometries.

We also considered online reconfiguration through redundancy allocation. Two additional columns were considered for each of the memory units. The distribution of the microprocessor lifetime with and without redundancy is shown in Fig. 26. The formulas needed to consider redundancy are given in Appendix B.

Fig. 27 shows the characteristic lifetime as a function of the maximum line space considered. The graph shows that large line spaces have an impact on the lifetime, especially for the higher layers of metal.

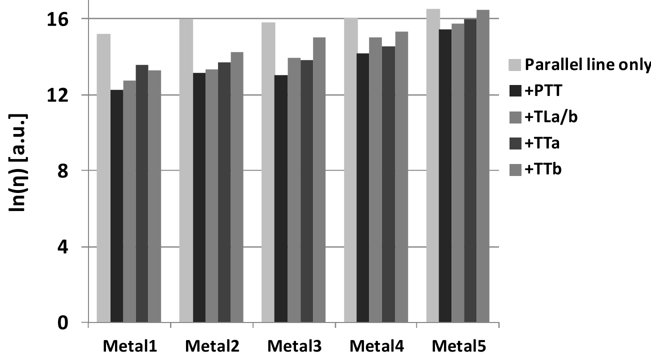

Fig. 29. Microprocessor characteristic lifetimes for each layer considering only the dielectric between parallel lines and considering the impact of each irregular feature geometry.

Fig. 28 shows the impact of irregular features. It can be observed that, as with the FFT circuit, the number of irregular geometries decreases for higher layers of metal. Fig. 29 shows the impact of each of the irregular geometries. The results are also consistent with the FFT circuit, with PTT having the strongest impact and TTb having the least impact.

VI. Conclusion

A methodology has been proposed to assess backend dielectric reliability of full chips. It considers all vulnerable dielectric areas with all line spaces in a layout. It also considers linewidth and many critical geometries, as well as the temperature and activity profiles during chip operation.

Several layouts were analyzed. No correlation between timing performance and dielectric lifetime was observed. Greater wire coverage, however, results in reduced lifetimes, as expected. It was also demonstrated that the area in a layout with the smallest line space may not significantly impact chip lifetime. Instead, all line spaces must be considered when estimating lifetime.

Appendix A

Estimation of the Probability of First Failure

Let us suppose that we are given a collection of n independent wearout mechanisms, modeled with Weibull distributions, having parameters, $\eta_i, i = 1, n$ and $\beta_i, i = 1, \ldots, n$. We want to find the probability that the first wearout mechanism fails before the other wearout mechanisms. Let $f_i(t_i)$ be the probability density function of the ith wearout mechanism. Then, the probability that the ith wearout mechanism fails first is

$$P = \int_0^\infty \int_{x_1}^\infty \int_{x_1}^\infty \cdots \int_{x_1}^\infty f_1(t_1) \cdots f_n(t_n) dt_n \cdots dt_3\, dt_2\, dt_1 \tag{A.1}$$

where

$$f_i(x_i) = \frac{\beta_i}{\eta_i}\left(\frac{t_i}{\eta_i}\right)^{\beta_i - 1} \exp\left(-\left(\frac{t_i}{\eta_i}\right)^{\beta_i}\right). \tag{A.2}$$

After substituting (A.1) into (A.2), we obtain

$$P = \frac{\beta_1}{\eta_1}\int_0^\infty \left(\frac{t_1}{\eta_1}\right)^{\beta_1 - 1} \exp\left(-\left(\frac{t_1}{\eta_1}\right)^{\beta_1}\right) - \cdots - \left(\frac{t_1}{\eta_n}\right)^{\beta_n}\Bigg) dt_1. \tag{A.3}$$

If β is a constant, then (A.3) reduces to

$$P = \left(\frac{\eta_{\text{chip}}}{\eta_1}\right)^{\beta}. \tag{A.4}$$

If β is not a constant, then numerical integration is required

$$P = \int_0^\infty e^{\alpha} du \tag{A.5}$$

where

$$\alpha = -u - \left(\frac{\eta_1}{\eta_2}\right)^{\beta_2} u^{\beta_2/\beta_1} - \cdots \left(\frac{\eta_1}{\eta_n}\right)^{\beta_n} u^{\beta_n/\beta_1}. \tag{A.6}$$

Appendix B

Dielectric Lifetime With Reconfiguration Through Redundancy Allocation

Online reconfiguration through redundancy allocation involves detecting failing memory cells and reconfiguration of memory blocks using redundant spare rows and columns. In this way, memory blocks can tolerate a small number of faults.

To determine the impact of redundancy, note that defect density associated with each component, i, is $(\text{TF}/\eta_i)^{\beta_i}$, where TF is time. Hence, the defect density increases as a function of time. The total defect density for a set of components (dielectric segments) is the sum of the component-level defect densities.

Let, $J_k, k = 1, \ldots, K$ be disjoint sets of components. For example, J_1 could consist of all dielectric segments in the Metal 1 layer of the D-cache and J_2 could consist of all dielectric segments in the Metal 1 layer of the I-cache. Any such set of components, J_k, can tolerate up to q_k defects. For example, if there are two redundant columns, then $q_k = 2$. If P is the probability of failure, then the survival probability for one collection of components with redundancy is

$$1 - P = \exp\left(-\Sigma_{i\epsilon \text{Jk}}\left(\frac{\text{TF}}{\eta_i}\right)^{\beta_i}\right) * \left(\Sigma_{x=0}^{qk}\frac{\left(\Sigma_{i\epsilon\text{Jk}}\left(\frac{\text{TF}}{\eta_i}\right)^{\beta_i}\right)^x}{x!}\right). \tag{A.7}$$

If there are K blocks with redundancy in the system, then the overall lifetime satisfies the following relationship:

$$1 - P = \exp\left(-\Sigma\left(\frac{\text{TF}}{\eta_i}\right)^{\beta_i}\right) * \left(\Pi_{k=1}^{k}\left(\Sigma_{x=0}^{qk}\frac{\left(\Sigma_{i\epsilon\text{Jk}}\left(\frac{\text{TF}}{\eta_i}\right)^{\beta_i}\right)^x}{x!}\right)\right). \tag{A.8}$$

This is equivalent to the following, which can be used to solve for lifetime, TF, as a function of each probability point:

$$-ln(1-P) = \Sigma_i\left(\frac{\text{TF}}{\eta_i}\right)^{\beta_i} - \Sigma_{k=1}^{k} ln\left(\Sigma_{x=0}^{qk}\frac{\left(\Sigma_{i\epsilon\text{Jk}}\left(\frac{\text{TF}}{\eta_i}\right)^{\beta_i}\right)^x}{x!}\right). \tag{A.9}$$

In addition, the characteristic lifetime under redundancy, η_{chip}, is the solution of the following:

$$1 = \Sigma_i \left(\frac{\eta_{\text{chip}}}{\eta_i}\right)^{\beta_i} - \Sigma_{k=1}^{k} ln \left(\Sigma_{x=0}^{qk} \frac{\left(\Sigma_{i \epsilon \text{Jk}} \left(\frac{\eta_{\text{chip}}}{\eta_i}\right)^{\beta_i}\right)^x}{x!} \right). \tag{A.10}$$

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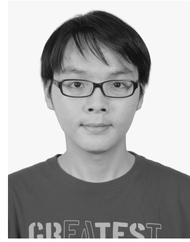
References

[1] T. Pompl, C. Schlunder, M. Hommel, H. Nielen, and J. Schneider, "Practical aspects of reliability analysis for IC design," in *Proc. Design Autom. Conf.*, Jul. 2006, pp. 193–198.
[2] S.-C. Lee, A. S. Oats, and K. M. Chang, "Limitation of low-k reliability due to dielectric breakdown at vias," in *Proc. IEEE IITC*, Jun. 2008, pp. 177–179.
[3] A. Yamaguchi, D. Ryuzaki, J. Yamamoto, H. Kawada, and T. Iizumi, "Characterization of line-edge roughness in Cu/low-k interconnect pattern," *Proc. SPIE, Metrology, Inspection, and Process Control for Microlithography XXI*, vol. 6518, p. 65181P, Apr. 2007.
[4] G. S. Haase and J. W. McPherson, "Modeling of interconnect dielectric lifetime under stress conditions and new extrapolation methodologies for time-dependent dielectric breakdown," in *Proc. 45th Annu. IEEE Int. Rel. Phys. Symp.*, Apr. 2007, pp. 390–398.
[5] J. Kim, E. T. Ogawa, and J. W. McPherson, "Time dependent dielectric breakdown characteristics of low-k dielectric (SiOC) over a wide range of test areas and electric fields," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2007, pp. 399–404.
[6] F. Chen, O. Bravo, K. Chanda, P. McLaughlin, T. Sullivan, J. Gill, J. Lloyd, R. Kontra, and J. Aitken, "A comprehensive study of low-k SiCOH TDDB phenomena and its reliability lifetime model development," in *Proc. 44th Annu. Int. Rel. Phys. Symp.*, Mar. 2006, pp. 46–53.
[7] F. Chen, O. Bravo, D. Harmon, M. Shinosky, and J. Aitken, "Cu/low-k dielectric TDDB reliability issues for advanced CMOS technologies," *Microelectron. Rel.*, vol. 48, nos. 8–9, pp. 1375–1383, Aug./Sep. 2008.
[8] N. Suzumura, S. Yamamoto, D. Kodama, H. Miyazaki, M. Ogasawara, J. Komori, and E. Murakami, "Electric-field and temperature dependencies of TDDB degradation in Cu/low-k damascene structures," in *Proc. Int. Rel. Phys. Symp.*, May 2008, pp. 138–143.
[9] M. Bashir, D. H. Kim, K. Athikulwongse, S. K. Lim, and L. Milor, "Backend low-k TDDB chip reliability simulator," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2011, pp. 65–74.
[10] M. Bashir, L. Milor, D. H. Kim, and S. K. Lim, "Methodology to determine the impact of linewidth variation on chip scale copper/low-k backend dielectric breakdown," *Microelectron. Rel.*, vol. 50, nos. 9–11, pp. 1341–1346, Sep./Nov. 2010.
[11] M. Bashir and L. Milor, "Towards a chip level reliability simulator for copper/low-k backend processes," in *Proc. DATE*, Mar. 2010, pp. 279–282.
[12] M. Bashir and L. Milor, "Analysis of the impact of linewidth variation on low-k dielectric breakdown," in *Proc. IEEE IRPS*, May 2010, pp. 895–902.
[13] M. Bashir and L. Milor, "A methodology to extract failure rates for low-k dielectric breakdown with multiple geometries and in the presence of die-to-die linewidth variation," *Microelectron. Rel.*, vol. 49, nos. 9–11, pp. 1096–102, 2009.
[14] L. Milor and C. Hong, "Area scaling for backend dielectric breakdown," *IEEE Trans. Semicond. Manuf.*, vol. 23, no. 3, pp. 429–441, Aug. 2010.
[15] K. O. Abrokwah, P. R. Chidambaram, and D. S. Boning, "Pattern based prediction for plasma etch," *IEEE Trans. Semicond. Manuf.*, vol. 20, no. 2, pp. 77–86, May 2007.
[16] R. A. Gottscho, C. W. Jurgensen, and D. J. Vitkavage, "Microscopic uniformity in plasma etching," *J. Vac. Sci. Technol.*, vol. 10, no. 5, pp. 2133–2147, 1992.
[17] C.-C. Chen, M. Bashir, L. Milor, D. H. Kim, and S. K. Lim, "Backend dielectric chip reliability simulator for complex interconnect geometries," in *Proc. IEEE IRPS*, Apr. 2012, pp. BD.4.1–BD.4.8.
[18] (2001). *Mibench Benchmark* [Online]. Available: http://www.eecs.umich.edu/mibench/>
[19] (2011). *PrimeTime Power Modeling Tool* [Online]. Available: http://www.synopsys.com/Tools/Implementation/SignOff/PrimeTime/Pages/default.aspx
[20] (2011). *HotSpot Temperature Modeling Tool* [Online]. Available: http://lava.cs.virginia.edu/HotSpot/
[21] (2005). *LEON 3 Processor* [Online]. Available: http://www.gaisler.com/cms/index.php?option=com_content&task=view&id=12&Itemid=53>
[22] Launchbird Design Systems Inc. (2003). *CF FFT* [Online]. Available: http://www.opencores.org
[23] NCSU EDA. (2008). *NCSU Free PDK45*, San Jose, CA, USA [Online]. Available: http://www.eda.ncsu.edu/wiki/FreePDK

Muhammad Muqarrab Bashir received the B.S. degree from the University of Engineering and Technology, Lahore, Pakistan, in 2006, and the M.S and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2008 and 2011 respectively.

He has been with Intel Corporation, Hillsboro, OR, USA, since 2011. His current research interests include interconnect reliability, system level modeling, device modeling, and new paradigms for process yield enhancement.



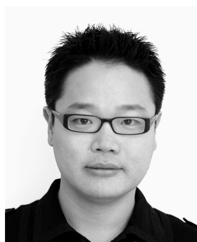
Chang-Chih Chen received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2007. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA. He was a Research Engineer with the Computer Architecture Laboratory, Georgia Tech, from 2010 to 2011, where he was engaged in the security issues of microprocessor systems. His current research interests include system-level modeling and reliability modeling, and yield analysis.

Linda Milor received the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA, in 1992.

She is currently a Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA. She was a Vice President of process technology and product engineering with eSilicon Corporation, a Product Engineering Manager with Advanced Micro Devices, Sunnyvale, CA, USA, and a Faculty Member with the University of Maryland, College Park, MD, USA. She has authored over 100 publications and holds four patents on yield and test of semiconductor integrated circuits.

Dae Hyun Kim received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2002, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2007 and 2012, respectively.

He is currently working on physical layout optimization at Cadence Design Systems, Inc. His current research interests include electronic design automation and computer-aided design for VLSI, high-performance and/or low-power VLSI and computer systems, and 3-D ICs.



Sung Kyu Lim (S'94–M'00–SM'05) received the B.S., M.S., and Ph.D. degrees from the Computer Science Department, University of California, Los Angeles, CA, USA, in 1994, 1997, and 2000, respectively.

He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, in 2001, where he is currently a Full Professor. His current research interests include the architecture, circuit design, and physical design automation for 3-D ICs. His current research interests include 3-D IC reliability, which is featured as a Research Highlight in the Communication of the ACM in 2013. He is the author of *Practical Problems in VLSI Physical Design Automation* (Springer, 2008).

Dr. Lim received the National Science Foundation Faculty Early Career Development Award in 2006. He was on the Advisory Board of the ACM Special Interest Group on Design Automation from 2003 to 2008 and received the Distinguished Service Award in 2008. He was an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS from 2007 to 2009. He has served the Technical Program Committee of several premier conferences in Electronic Design Automation. He received the Best Paper Award from TECHCON in 2011, TECHCON in 2012, and ATS in 2012. His work was nominated for the Best Paper Award at ISPD in 2006, ICCAD in 2009, CICC in 2010, DAC in 2011, DAC in 2012, and ISLPED in 2012. He was a member of the Design International Technology Working Group of the International Technology Roadmap for Semiconductors. He led the Cross-Center Theme on 3-D Integration for the Focus Center Research Program, Semiconductor Research Corporation, from 2010 to 2012.