# Guest Editors' Introduction: Advances in 3-D Integrated Circuits, Systems, and CAD Tools

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**THREE-DIMENSIONAL INTEGRATION HAS** been considered one of the most promising breakthrough technologies achieving higher integration density, better performance, lower power consumption, and smaller form factor. Enabling 3-D integration, however, requires innovation and advancement in manufacturing technology, modeling, design methodologies, and optimization algorithms for physical layout, circuit and system architectures, cooling solutions, testing methodologies, and applications. Thanks to the enormous efforts put into 3-D integration, a few commercial 2.5-D and 3-D products are finally coming into the semiconductor market. These 2.5-D and 3-D products must be just a beginning of the era of 3-D ICs and more general 3-D IC products such as multidie logic-logic-stacked 3-D ICs, many-die-stacked 3-D ICs, and heterogeneous 3-D ICs will be successfully commercialized and appear in the semiconductor market in the future. However, enabling the general 3-D ICs is still very challenging due to various problems such as heat removal, lack of standards and design and analysis tools, and unsatisfactory performance improvement.

This special issue highlights recent investigations regarding 3-D integration. The selected papers cover a wide range of topics on 3-D ICs, from manufacturing process and 3-D integration technology to test methodologies, applications, and optimization algorithms.

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"Physical Design and CAD Tools for 3-D Integrated Circuits: Challenges and Opportunities," by Kim and Lim, gives an overview of 3-D integration technologies (2.5-D, TSV-based 3-D, inductive-coupling-based 3-D, and monolithic 3-D), then presents challenges and opportunities from various perspectives. It also reviews past works on CAD algorithms for 3-D integration and discusses uncharted problems for each 3-D integration technology.

"Fabrication and Assembly of Cu-RDL-based 2.5-D Low-Cost Through Silicon Interposer (LC–TSI)," by Katti et al., presents a low-cost through silicon interposer (LC–TSI) fabrication process. The authors first present an overview of their 2.5-D LC–TSI technology and key challenges to resolve. Then, they provide details on their TSV and Cu-RDL fabrication process, C-o-(C-o-S) assembly, cost reduction, and warpage analysis. Last, they show characterization and measurement results.

"Heat Dissipation Capability of a Package-on-Package Embedded Wafer-Level Package," by Han et al., presents the heat dissipation capability of embedded wafer-level package (eWLP) technology. The authors first show their simulation models and results for thermal analysis of eWLP package and package-on-package (POP) structures. With the models, they analyze thermal effects of passivation materials and find a main heat dissipation path. Then, they propose passive cooling solutions (top cap and package lid) for better heat dissipation.

"A DfT Architecture and Tool Flow for 3-D SICs with Test Data Compression, Embedded Cores, and Multiple Towers," by Papameletis et al., proposes a



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design-for-test (DfT) architecture for efficient testing of 3-D ICs. The goal of this paper is to extend an existing DfT architecture to support multiple dies, test data compression, and embedded cores and implement it using existing commercial software. The authors first review the original DfT architecture for 3-D ICs and present how they extend it for test data compression. Then, they describe how to extend the architecture to handle multiple towers for 2.5-D ICs and embedded cores for hierarchical 3-D SoC designs. Last, the authors present how to use existing EDA tool flows to implement the extended DfT architecture and generate test patterns.

"A 2.5-D Memory-Logic Integration with Data-Pattern-Aware Memory Controller," by Xu et al., presents silicon interposer-based 2.5-D integration of core and memory chips. To maximize the utilization of the channels through TSVs and interposer routing between the core and memory chips, the authors use bandwidth balancing based on space-time multiplexing of the channels and core clustering. The authors first compare 3-D and 2.5-D ICs and show that 3-D ICs seriously suffer from thermal runaway when many layers (more than four) are stacked. Use of the 2.5-D architecture with shared memory and space-time channel multiplexing that the authors propose for many-core-memory integration improves the quality of service significantly.

"Hierarchical Test Integration Methodology for 3-D ICs," by Chou et al., proposes a hierarchical test methodology for 3-D ICs that can handle multiple dies in a single 3-D IC, multiple 3-D chips in a single package, and dies tested by built-in self-test (BIST). With all the details on the proposed hierarchical test architecture, master and slave control interfaces, and test instructions for these interfaces, the authors show how to test each 3-D IC mounted on an interposer and handle BIST circuits. They also present measurement results obtained from a test chip for better understanding of the proposed test integration method.

"3D-WiRED: A Novel WIDE I/O DRAM with Energy-Efficient 3-D Bank Organization" by Thakkar and Pasricha, proposes a new wide I/O DRAM architecture to reduce access latency and energy consumption. The authors deeply analyze timing and energy of the wide I/O DRAM to identify latency and energy bottlenecks. Based on the detailed analysis, they propose a new wide I/O DRAM architecture to reduce the latency and energy bottlenecks, which is achieved by reorganization of subarchitectures and an extensive use of through silicon vias.

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