

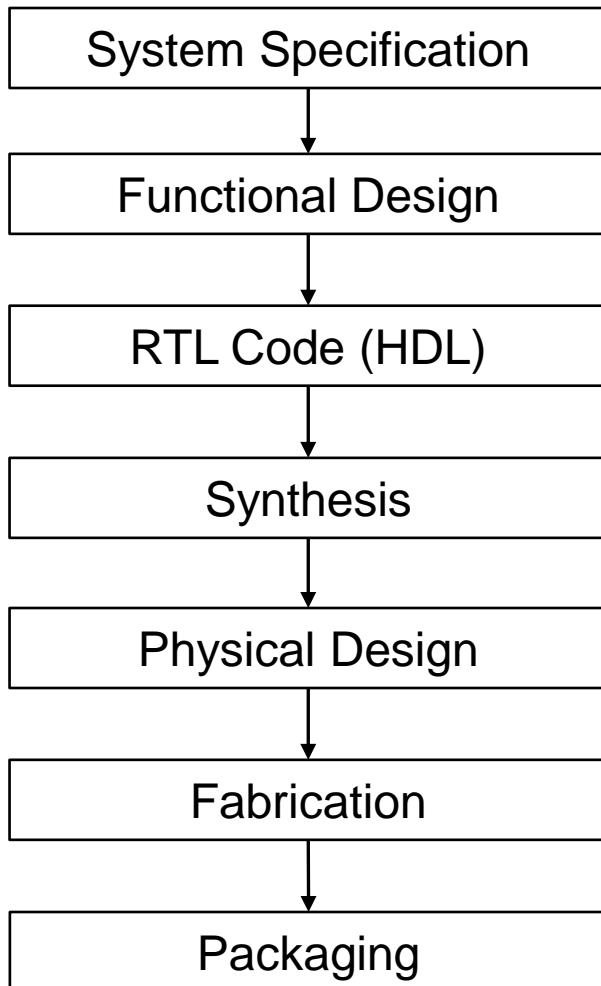
EE 434

ASIC and Digital Systems

Prof. Dae Hyun Kim
School of Electrical Engineering and Computer Science
Washington State University

Preliminaries

VLSI Design

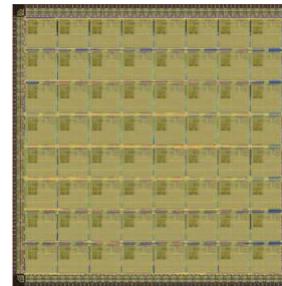


Freq Area Power
64-bit integer multiplier / 1GHz / 0.1mm² / 0.1mW

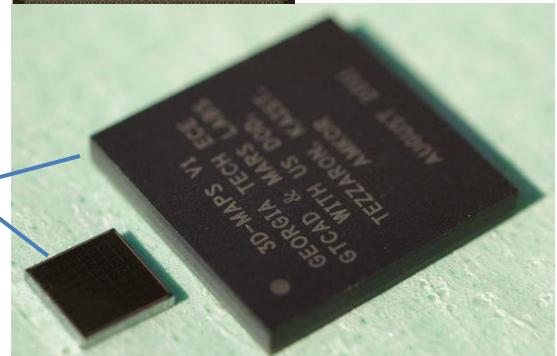
C/C++, Verilog, VHDL, ...

```
module imul_64 (a, b, clk, out64);  
input a, b, clk; output out64; ... endmodule
```

Netlist



Layout



Bare die

Chip

From RTL Code to a Chip

RTL Code (HDL)

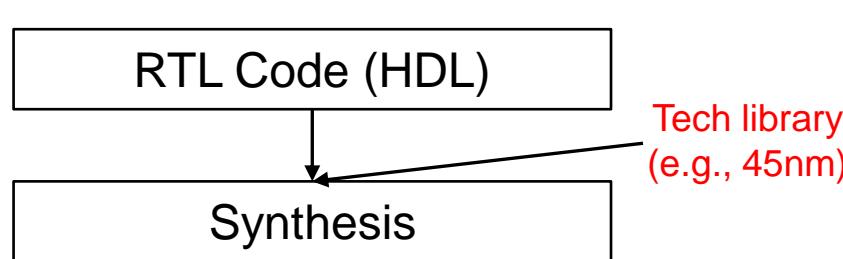
```
module mul64 (in_1, in_2, clk, out_1);
    input [31:0] in_1, in_2;
    input clk;
    output [63:0] out_1;

    reg [63:0] int_stage1;
    reg [63:0] int_stage2;

    always @ (posedge clk)
    begin
        ...
    end

endmodule
```

From RTL Code to a Chip

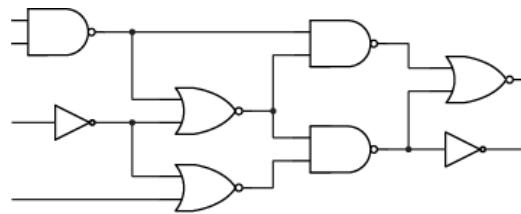


```
module mul64 (in_1, in_2, clk, out_1);
    input [31:0] in_1, in_2;
    input clk;
    output [63:0] out_1;

    reg [63:0] int_stage1;
    reg [63:0] int_stage2;

    always @ (posedge clk)
    begin
        ...
    end

endmodule
```



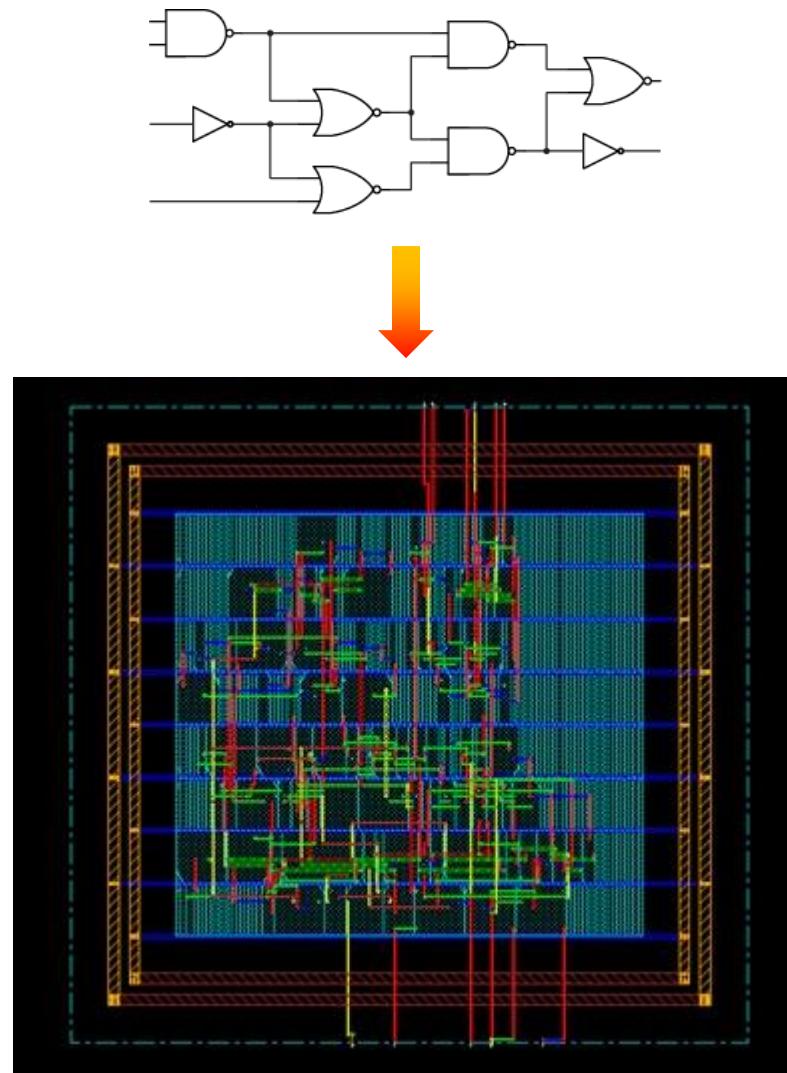
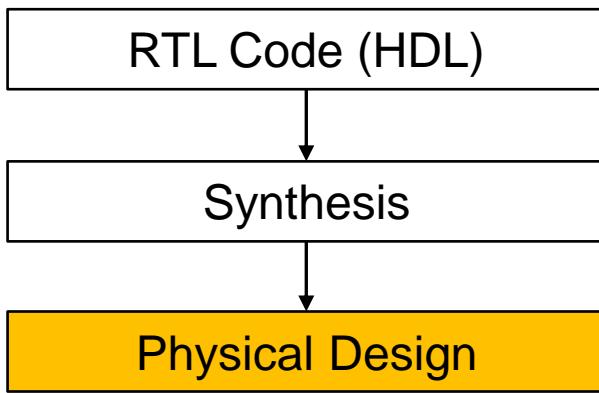
Tech-specific logic gates

```
module mul64 (in_1, in_2, clk, out_1);
    input [31:0] in_1, in_2;
    input clk;
    output [63:0] out_1;

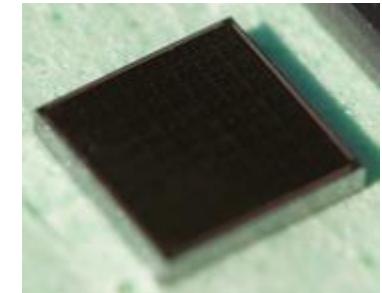
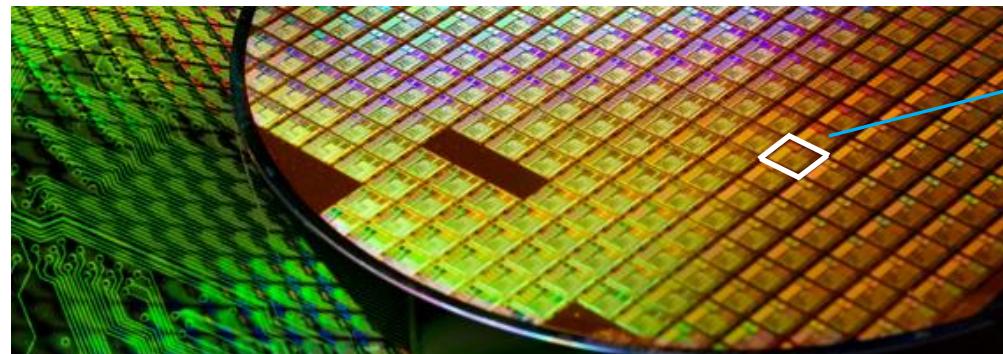
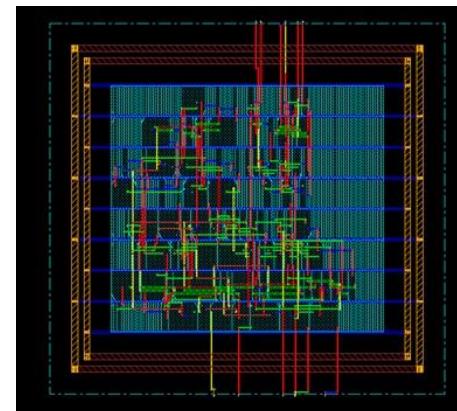
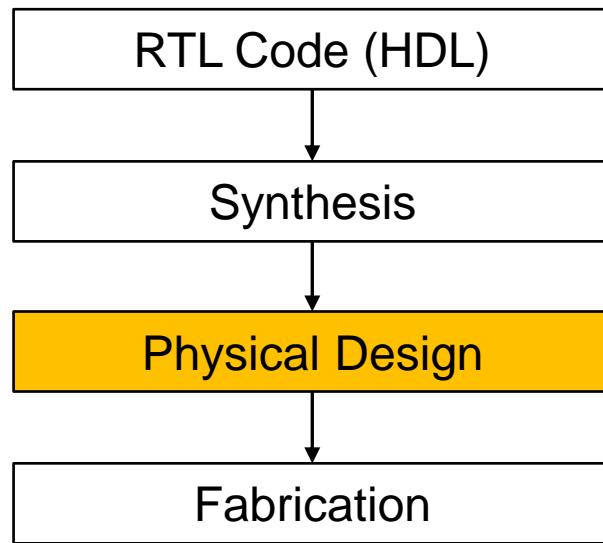
    NAND2_X1 (.A(in_1[0]), .B(in_2[0]), .Z(n1));
    FA_X1 (.A(in_1[0]), .B(in_2[0]), .CI(1'b0), .S(n2), .CO(n3));
    ...

endmodule
```

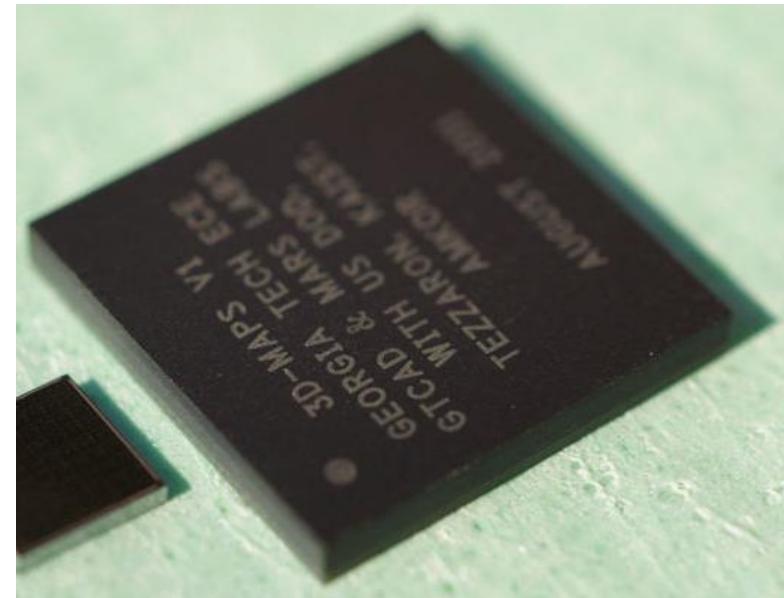
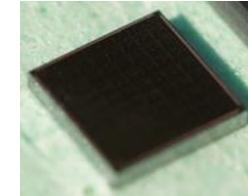
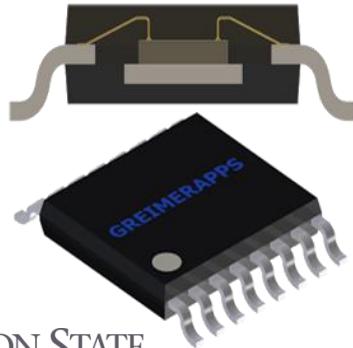
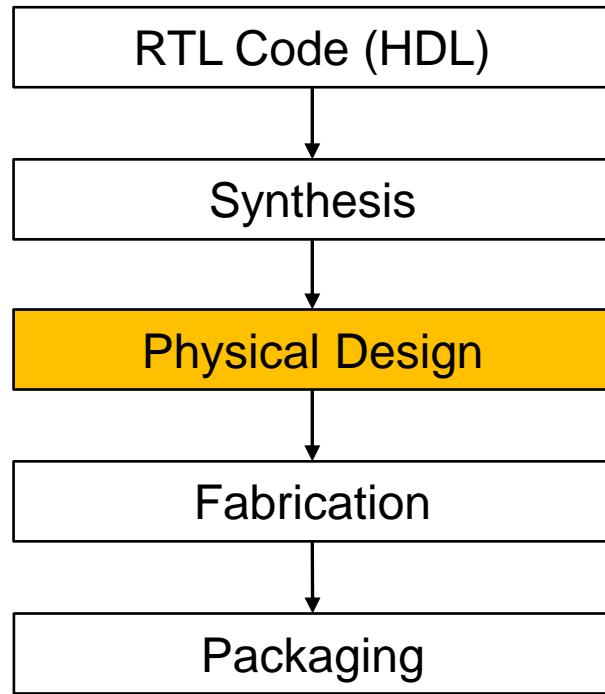
From RTL Code to a Chip



From RTL Code to a Chip

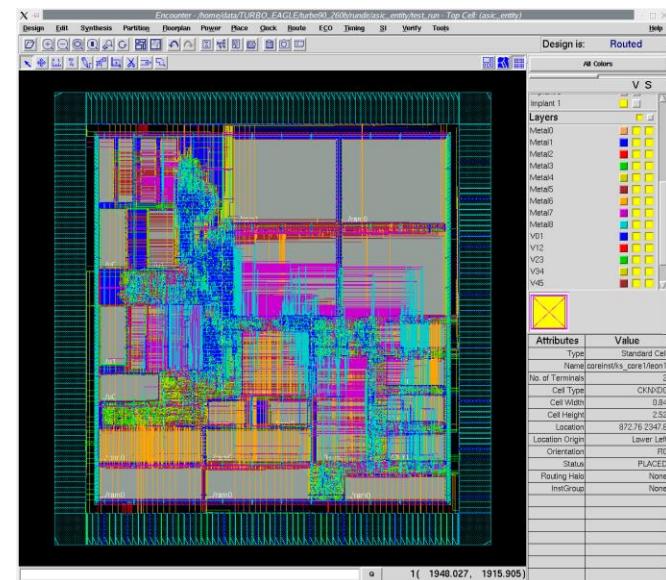
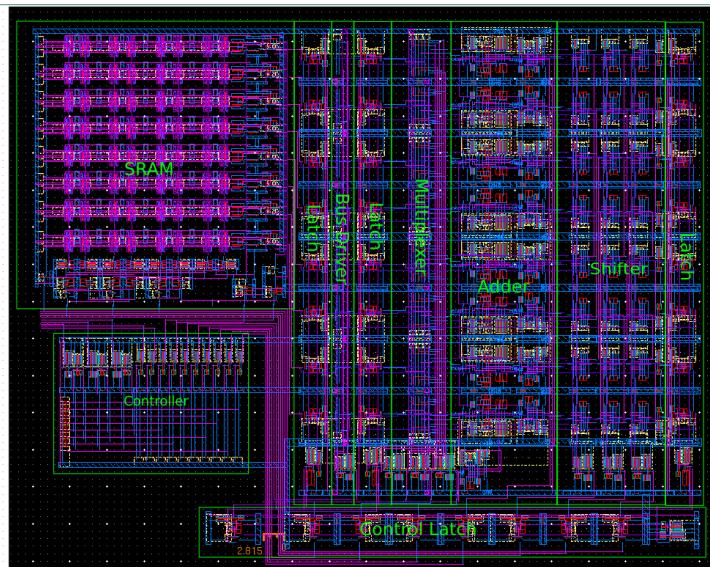


From RTL Code to a Chip



VLSI Design

	Full custom	ASIC
Design	Manual	Automatic
TRs	Manually drawn	Standard-cell based
Placement & Routing	Custom	Automatic
Development time	Several months	A few days ~ weeks



Standard-Cell-Based Design

- Provides
 - good performance
 - low power
 - small area
 - ...
- Other design styles
 - FPGA
 - PLA
 - ...

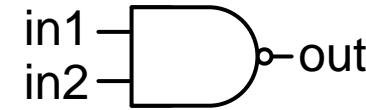
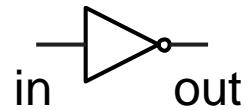
Standard-Cell-Based Design

- Standard cells
 - A set of logic gates
 - Have the same height.
 - Width varies.
 - Pre-characterized for timing and power analysis.

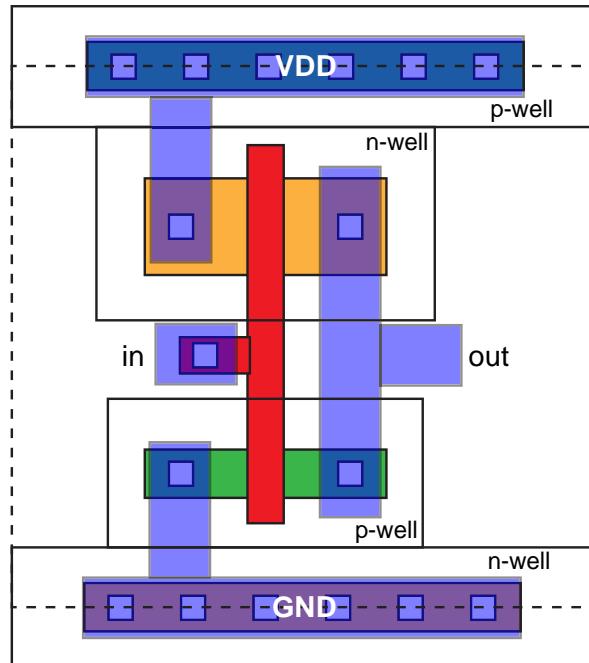
INV

NAND2

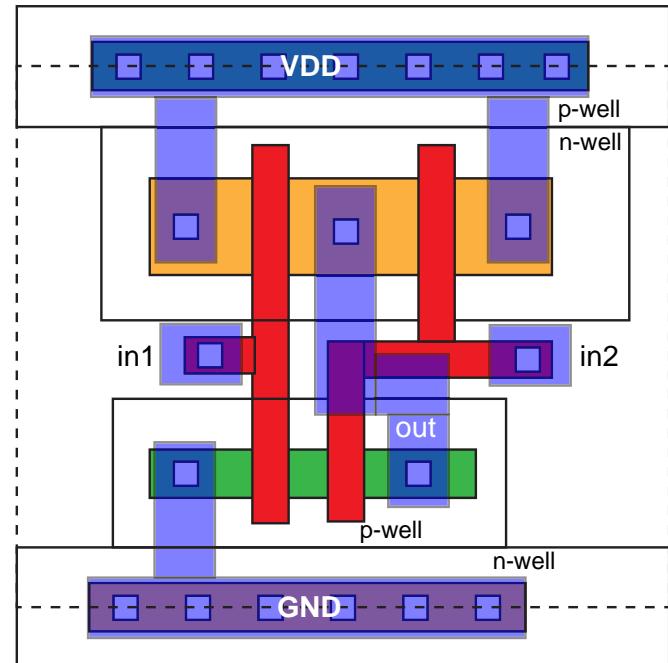
Standard Cells (Layout)



- █ n+ (n-implant)
- █ p+ (p-implant)
- contact
- █ poly (gate)
- █ metal 1
- - - cell boundary

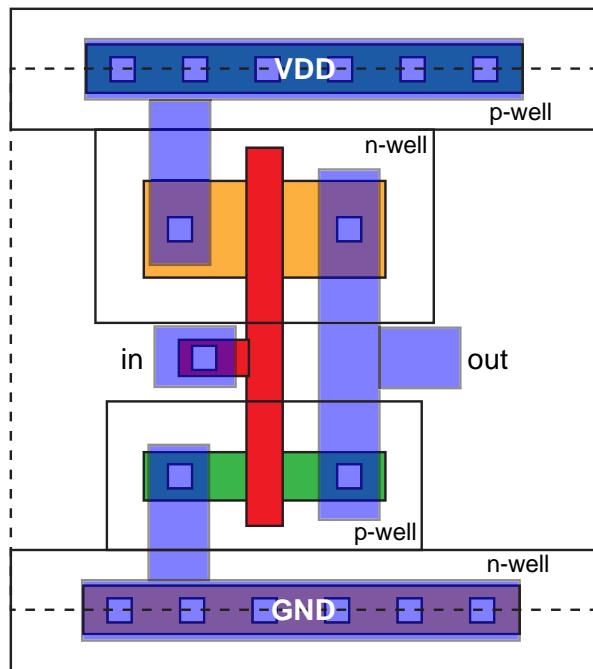


INV

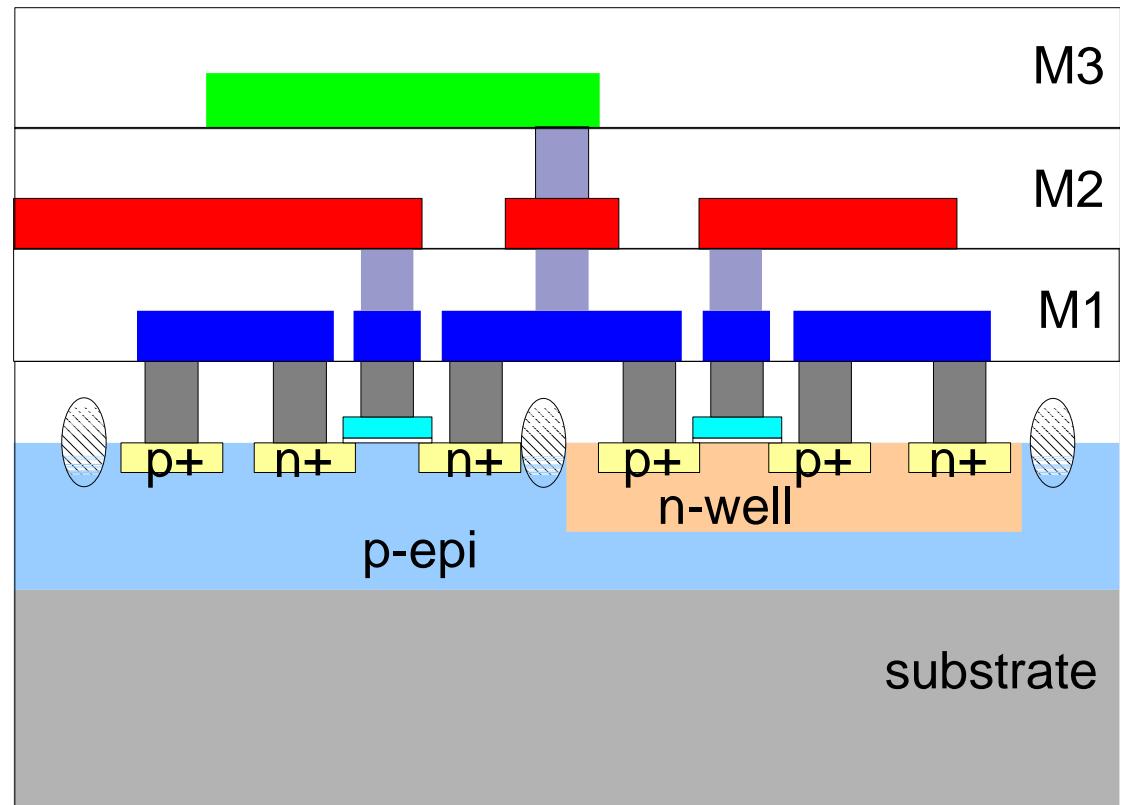


NAND2

Standard Cells (Layout)

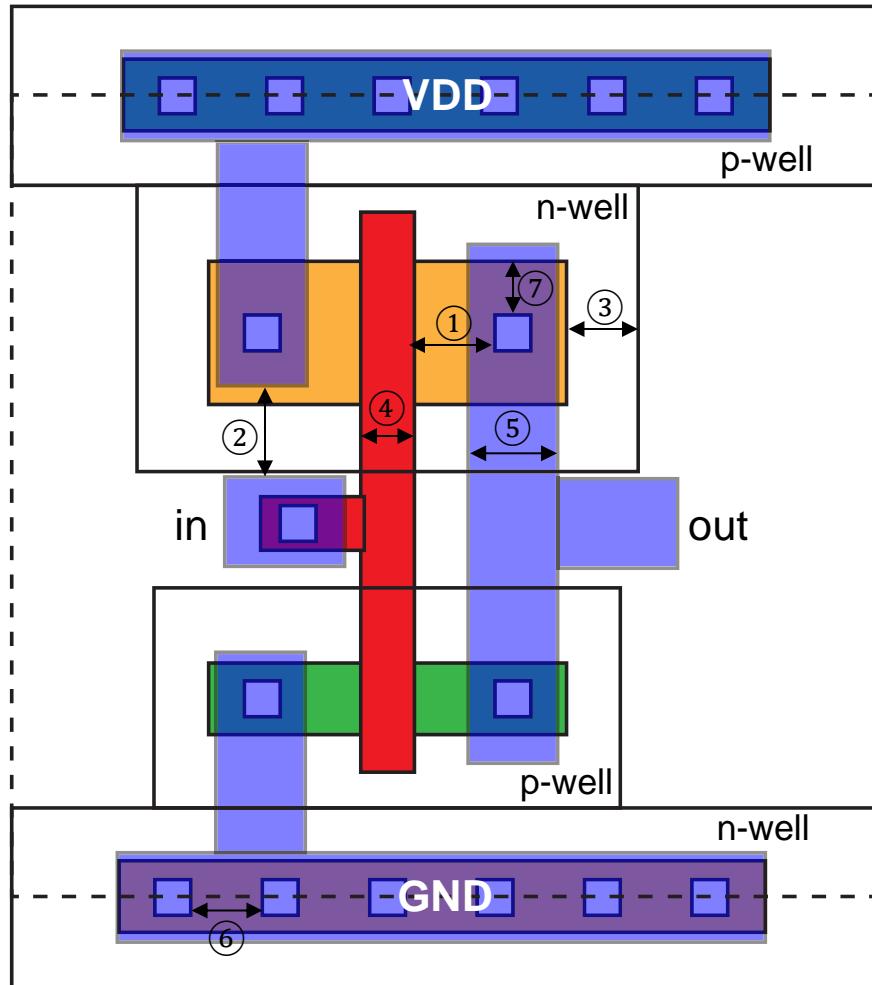


Top-down view

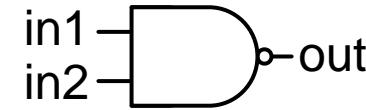
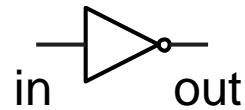


Side view

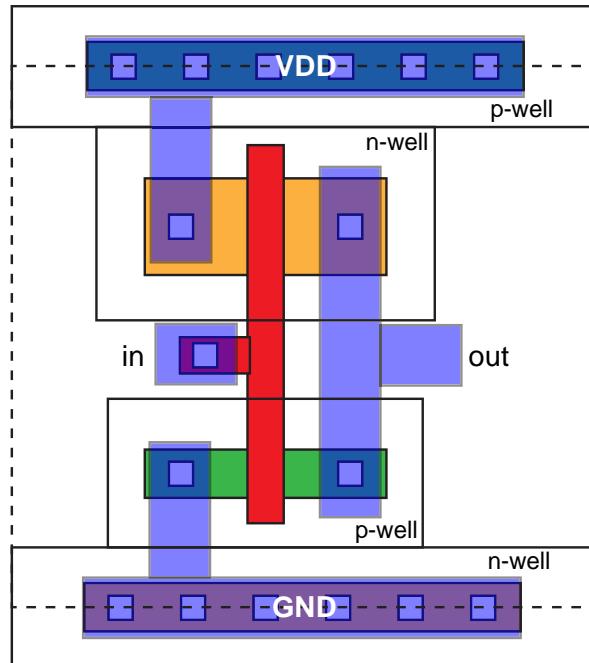
Design Rules



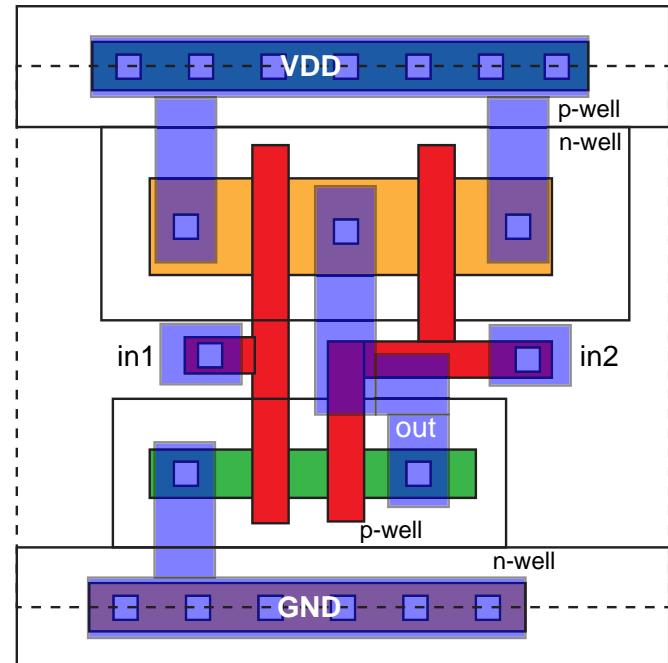
Standard Cells (Layout)



- █ n+ (n-implant)
- █ p+ (p-implant)
- contact
- █ poly (gate)
- █ metal 1
- - - cell boundary

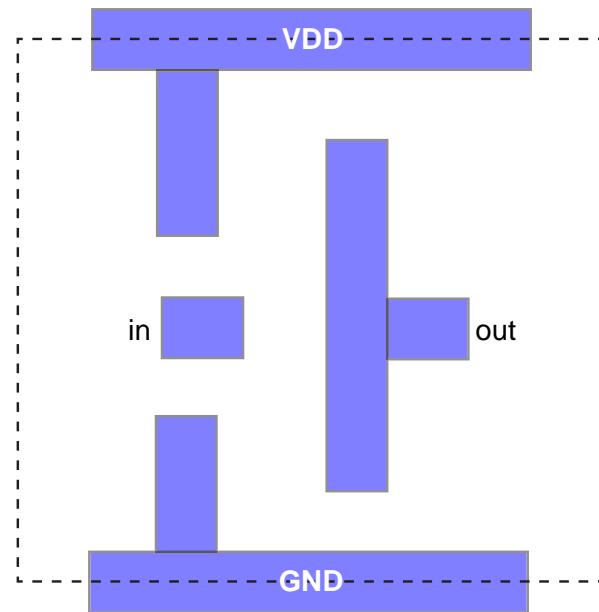
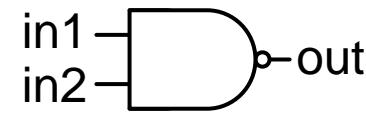
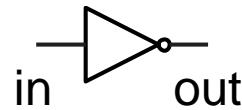


INV

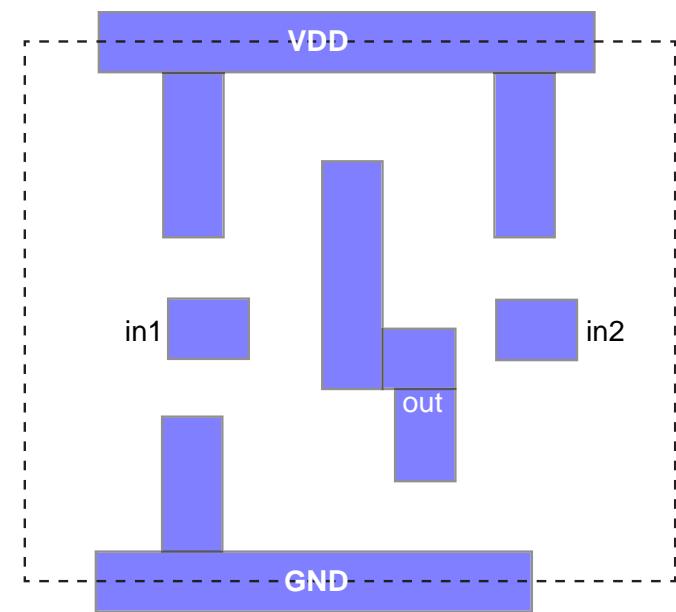


NAND2

Standard Cells (Abstract)

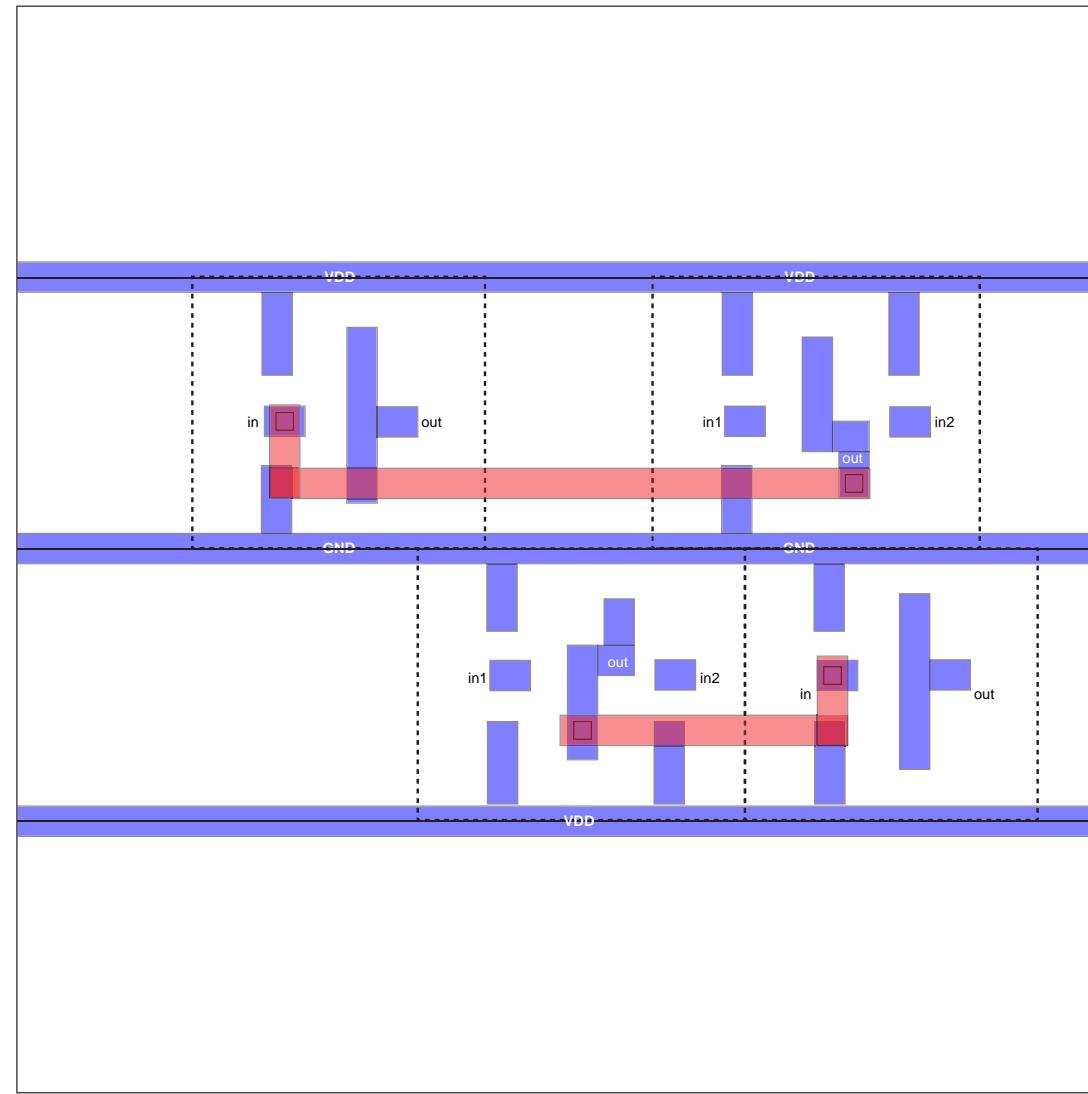
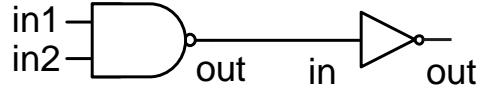


INV



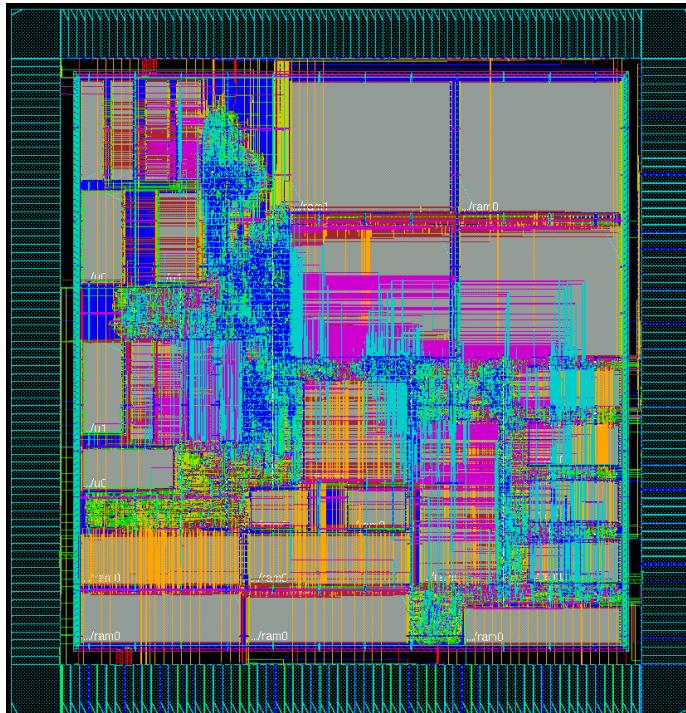
NAND2

Standard-Cell-Based Design



Standard-Cell-Based Design

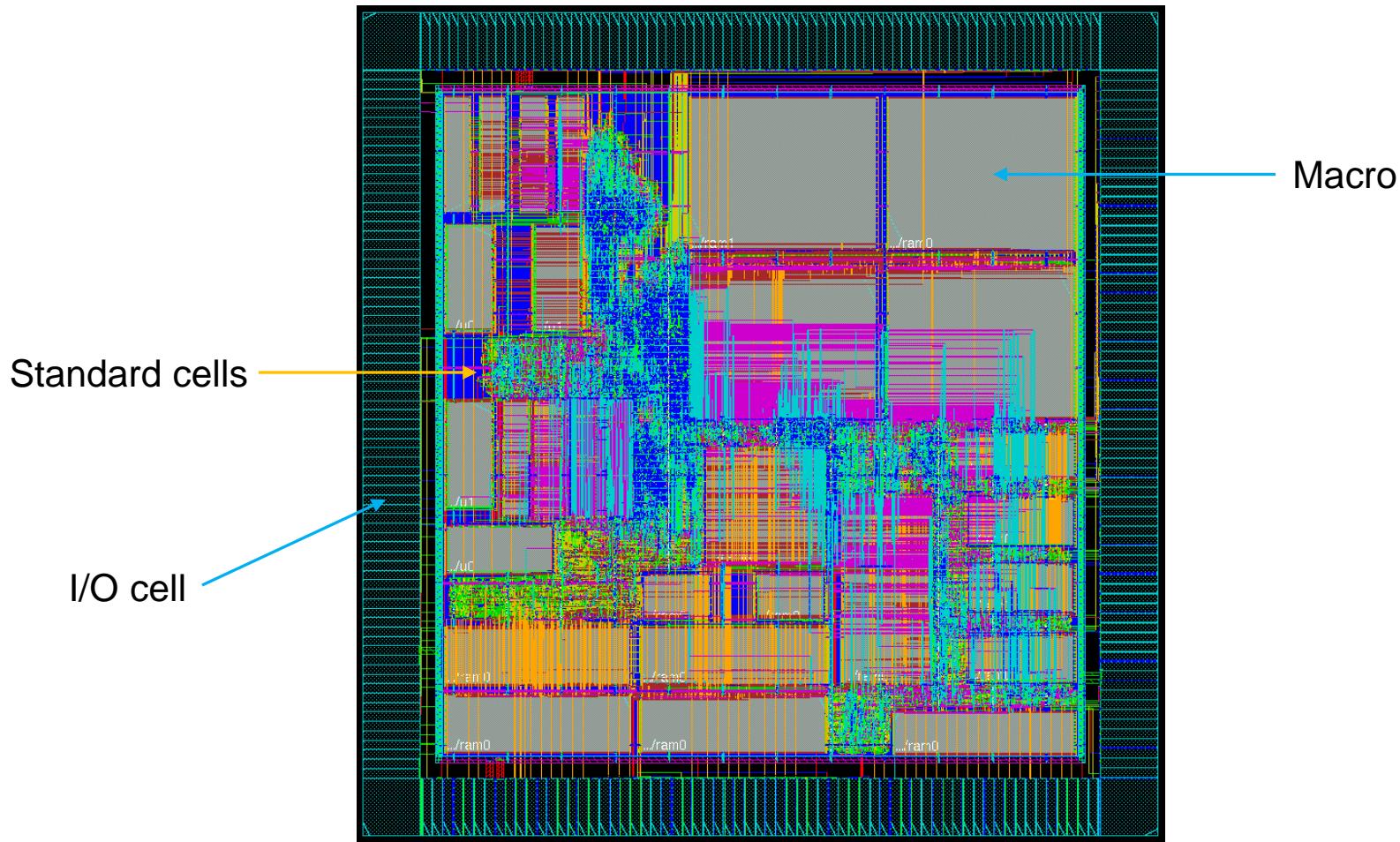
- Deal with
 - Standard cells (pre-drawn and pre-characterized)
 - Routing layers (M1, via12, M2, via23, ...)



Standard-Cell-Based Design

- Intellectual Property (IP) blocks
 - Pre-created blocks
 - Memory
 - Arithmetic
 - Cryptographic
 - DSP
 - Controller
 - ...

Standard-Cell-Based Design



Delay Calculation & Timing Analysis

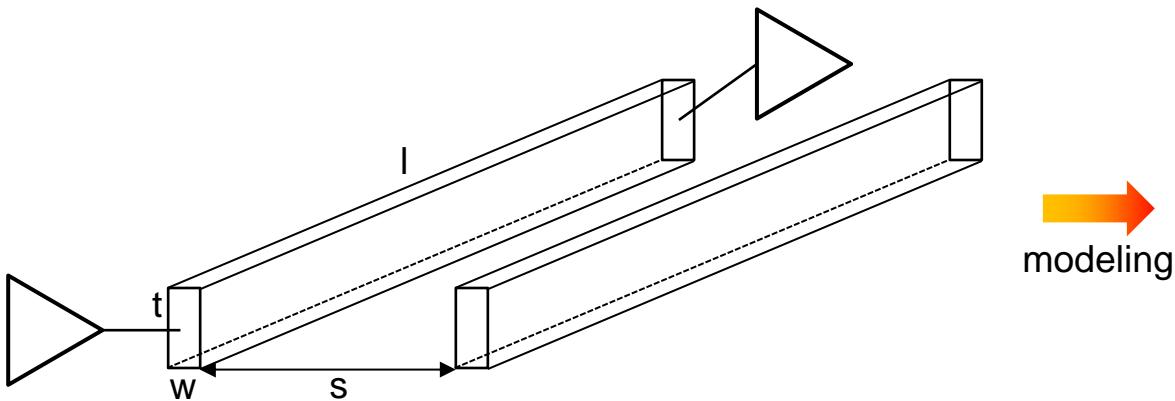
- Pre-characterized cells

The diagram illustrates the calculation of delay from a timing characterization table. On the left, two input parameters are shown: "Input transition (ns)" and "Output capacitance (fF)". Arrows point from these inputs to the first two columns of a table. The table rows are labeled "Index_1" and "Index_2". The third column contains numerical values. A blue arrow points to the value in the 3rd column of the 2nd row, labeled "3rd". Another blue arrow points to the value in the 5th column of the 2nd row, labeled "5th". A red box highlights the value "3.709790" in the 3rd column of the 2nd row. A red arrow points from this highlighted value to the text "Delay (29ps)" at the bottom. The table structure is as follows:

Input transition (ns)	index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");	Index_2
Output capacitance (fF)	index_2 ("0.365616,1.854900,3.709790,7.419590,14.839200,29.678300,59.356700");	
	values ("0.00683090,0.0100142,0.0139116,0.0216539,0.0370876,0.0679222,0.129575", "0.00801780,0.0112344,0.0151696,0.0229509,0.0384185,0.0692724,0.130935", "0.0110663,0.0155786,0.0201499,0.0279195,0.0433427,0.0741885,0.135850", "0.0127253,0.0190883,0.0256634,0.0364481,0.0533390,0.0839029,0.145413", "0.0128360,0.0209729,0.0293903,0.0433808,0.0656528,0.0997348,0.160709", "0.0112031,0.0210972,0.0313125,0.0483362,0.0756855,0.118141,0.182879", "0.00772654,0.0192683,0.0312780,0.0512843,0.0834863,0.133996,0.210841");	
	}	

Delay Calculation

- Interconnect delay

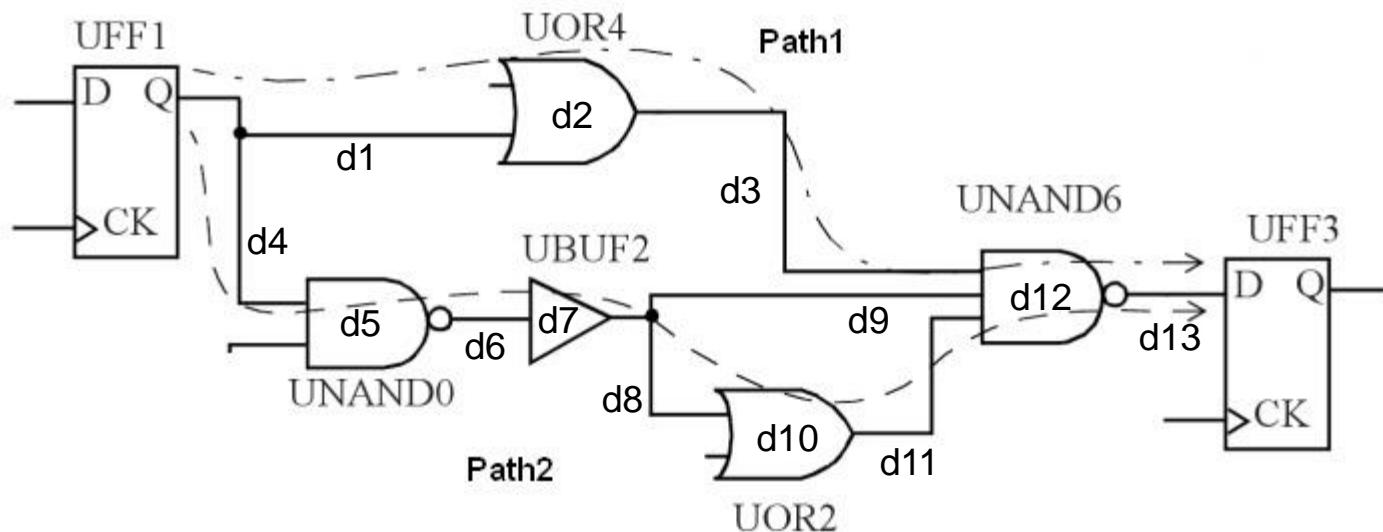


$$R = \rho \frac{l}{t \cdot w}$$

$$C = \epsilon \frac{t \cdot l}{s}$$

$$\text{Delay} \propto RC \propto l^2$$

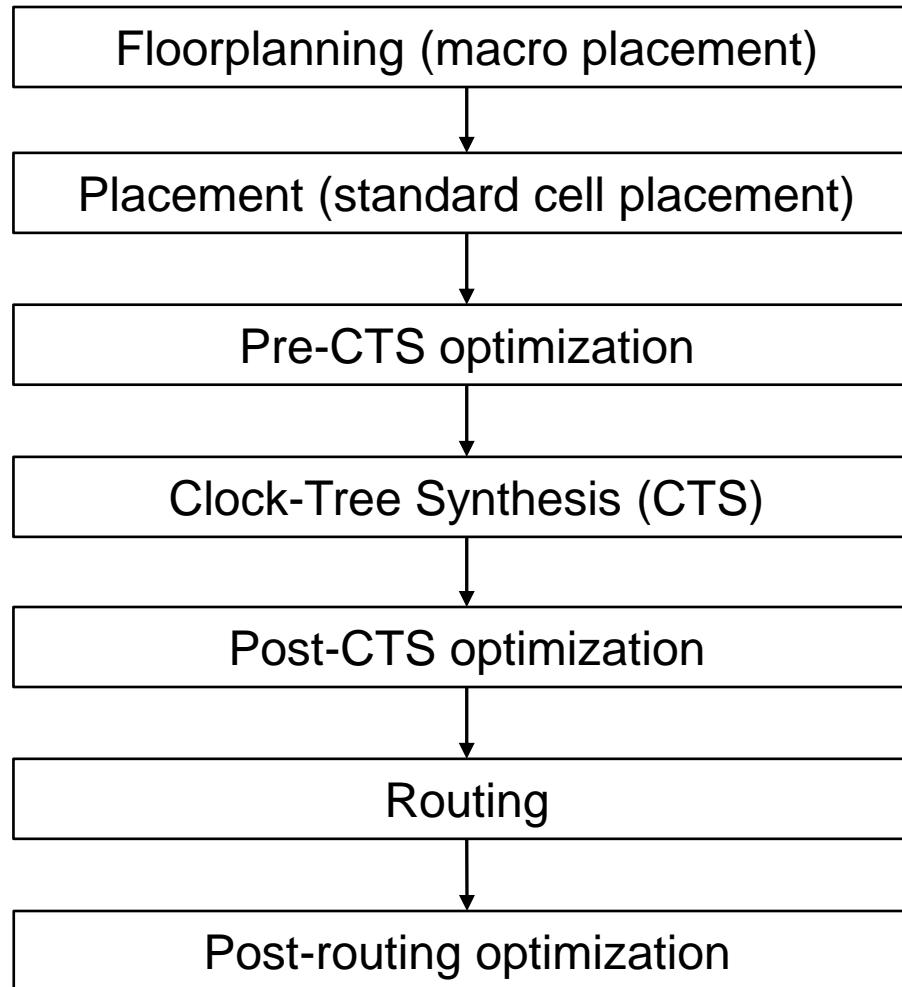
Timing Analysis



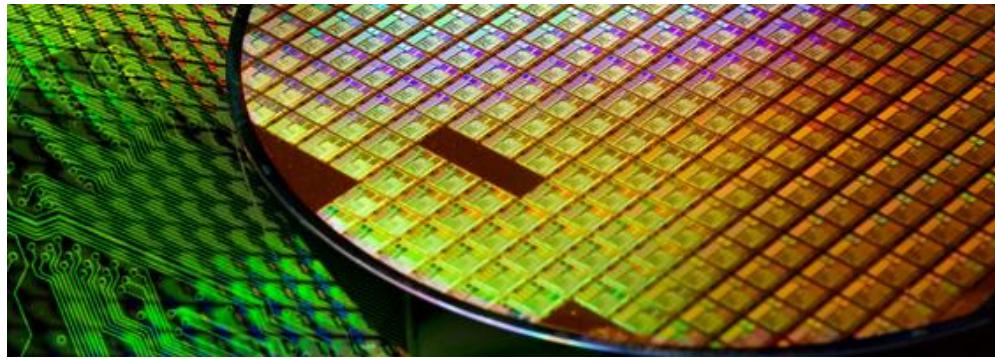
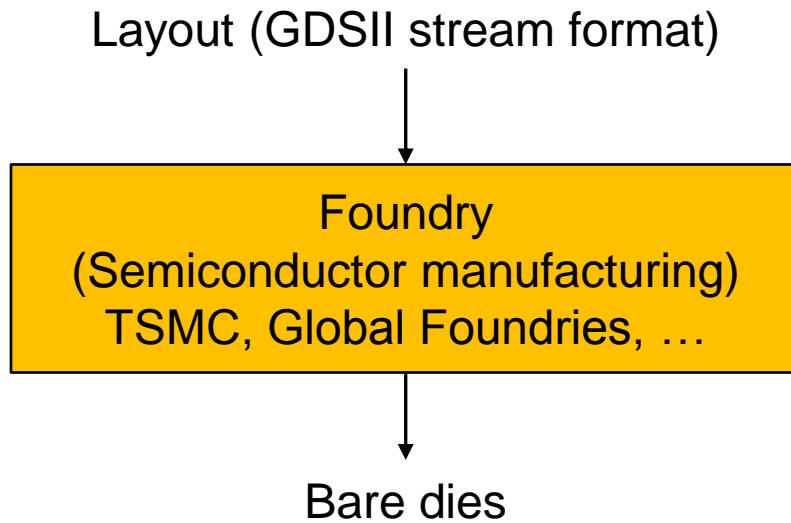
Standard-Cell-Based Design

- What should we do?
 - Find the locations of the macros.
 - Find the locations of the standard cells.
 - Route the macros and the standard cells.
 - Power/ground
 - Signal
 - Clock
 - Bus
 - Extract parasitic RC.
 - Analyze the final layout.
 - Timing (clock frequency)
 - Power consumption (dynamic / leakage)
 - Area
 - Power integrity
 - Signal integrity
 - Thermal

Standard-Cell-Based Design

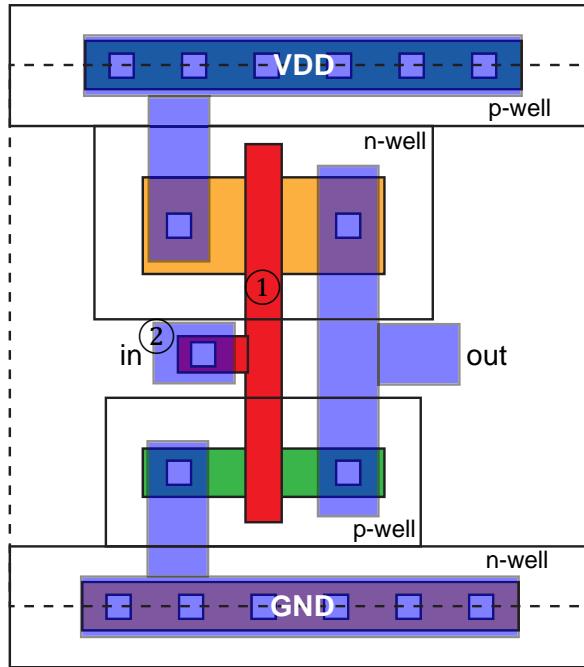


Semiconductor Manufacturing



Semiconductor Manufacturing

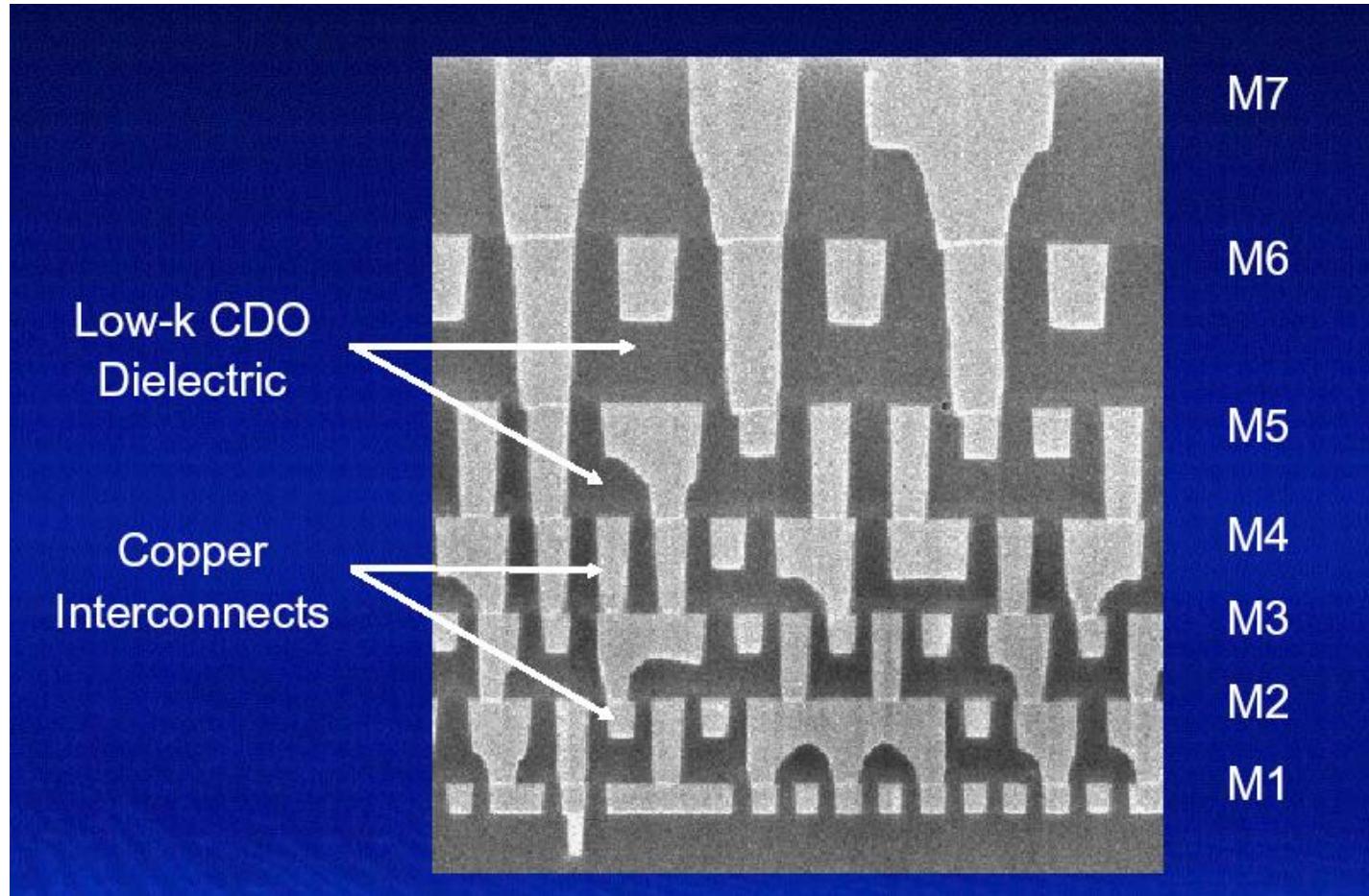
- Input
 - Layout (GDSII stream format)
 - A set of geometric objects



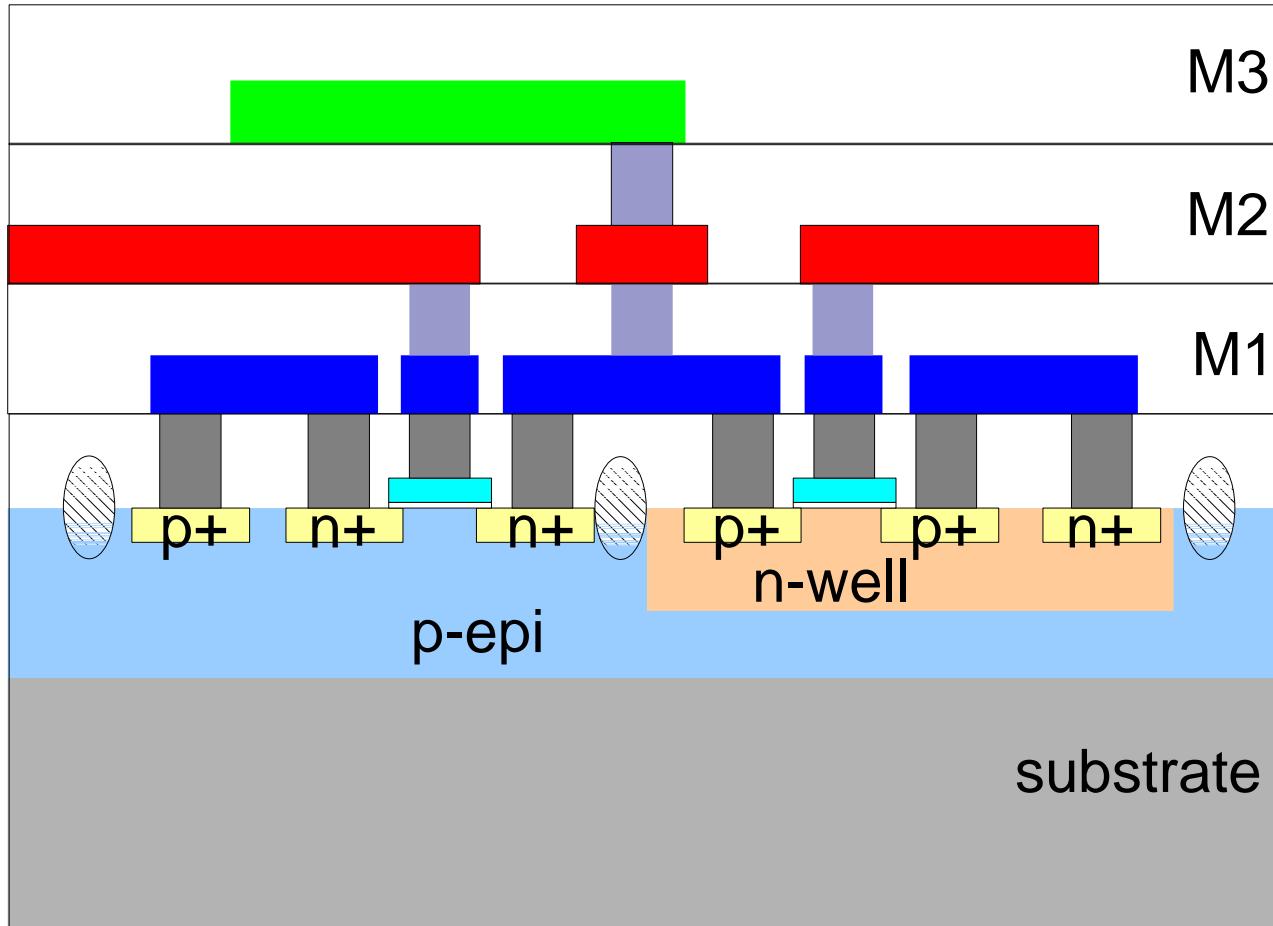
①: Layer id 3, polygon { 50, 40, 70, 40, 70, 220, 50, 220, 50, 140, 20, 140, 20, 110, 50, 110, 50, 40 }

②: Layer id 7, rectangle { 10, 105, 40, 150 }

Semiconductor Manufacturing



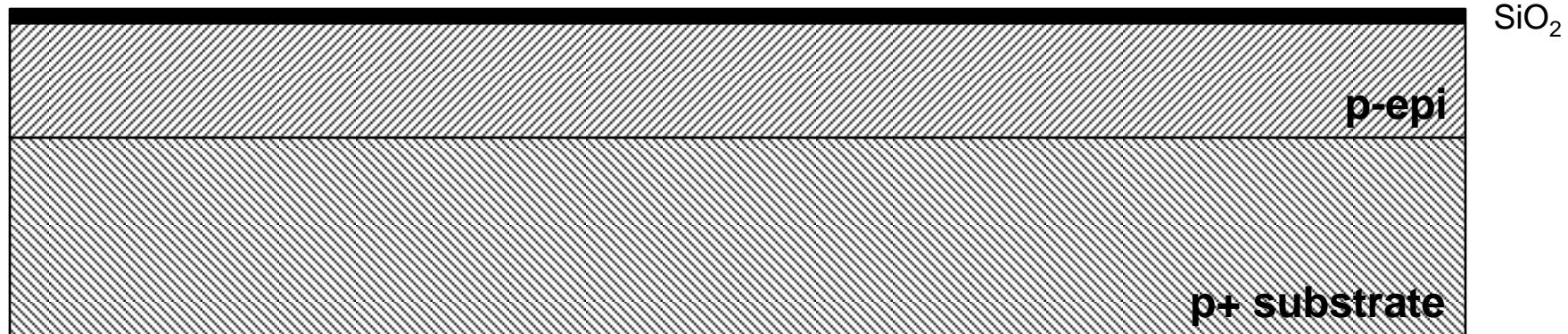
Semiconductor Manufacturing



Semiconductor Manufacturing

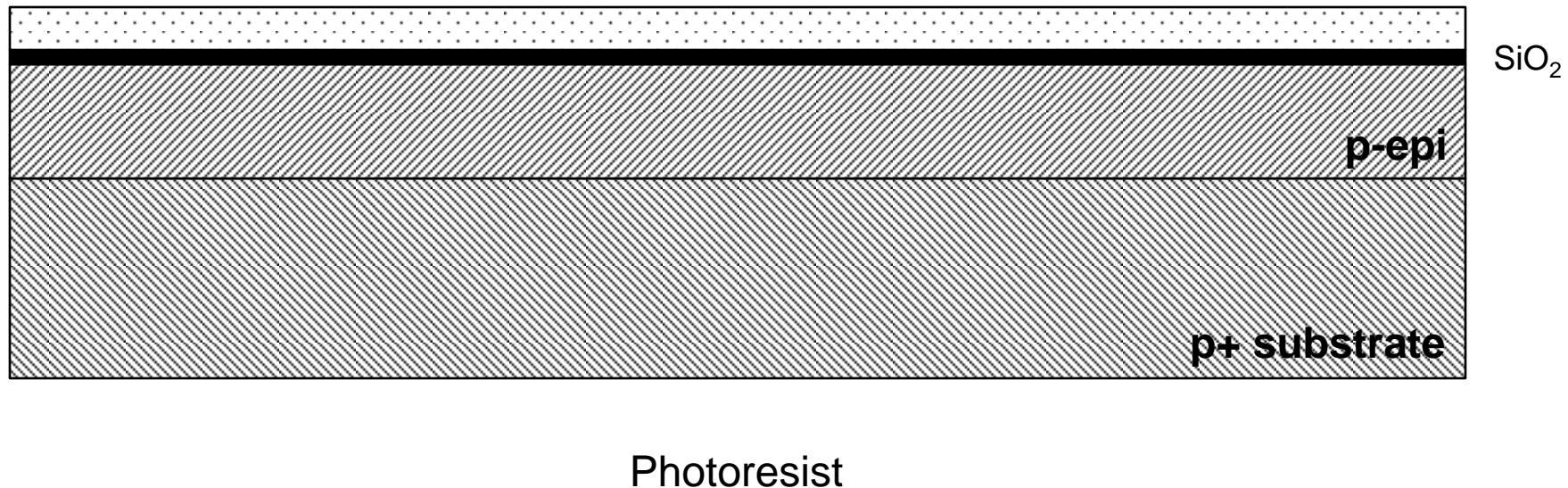


Semiconductor Manufacturing

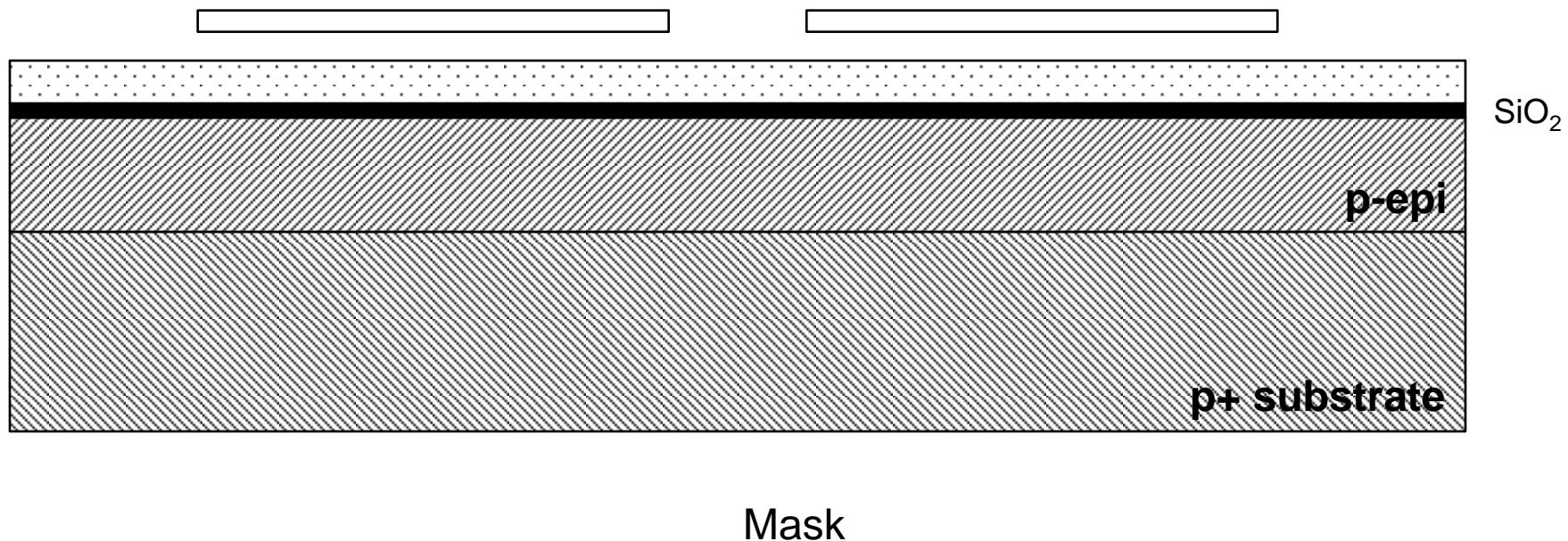


Gate-oxide deposition

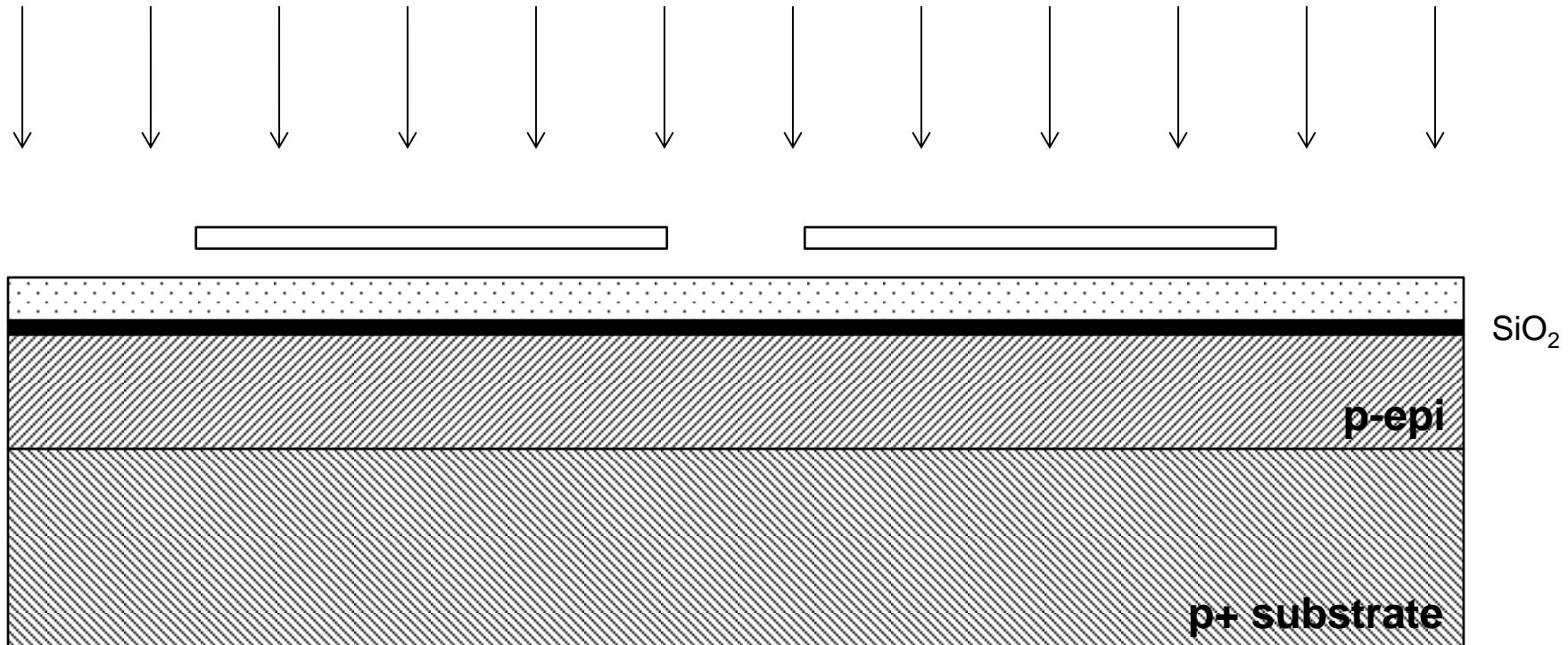
Semiconductor Manufacturing



Semiconductor Manufacturing

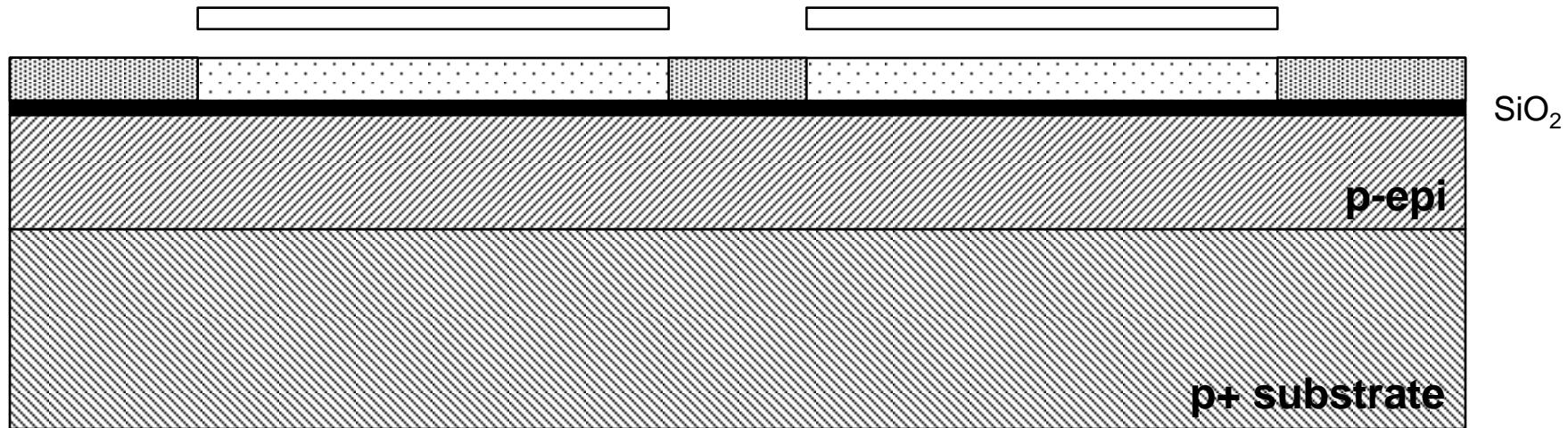


Semiconductor Manufacturing



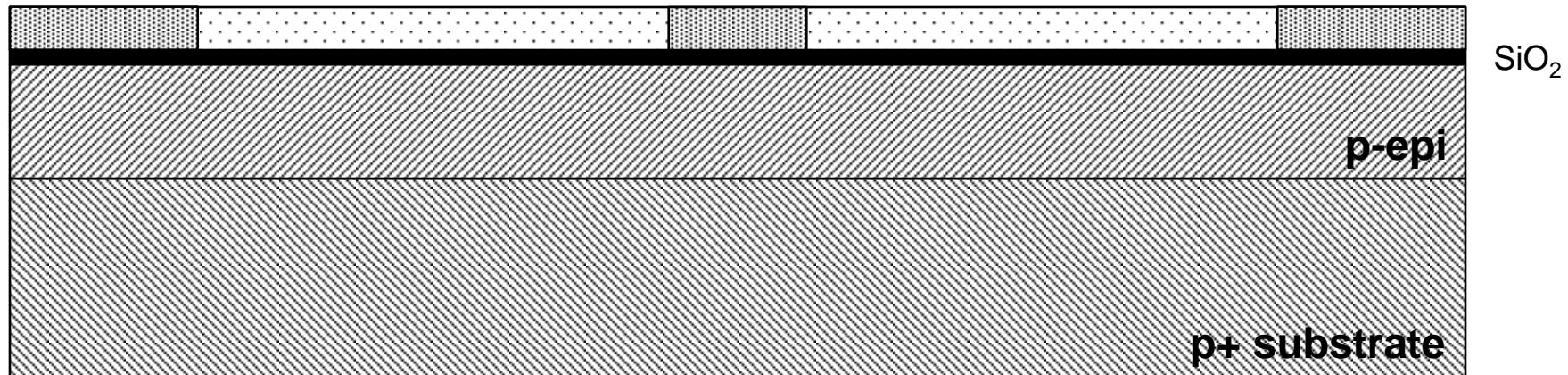
Expose (photolithography)

Semiconductor Manufacturing



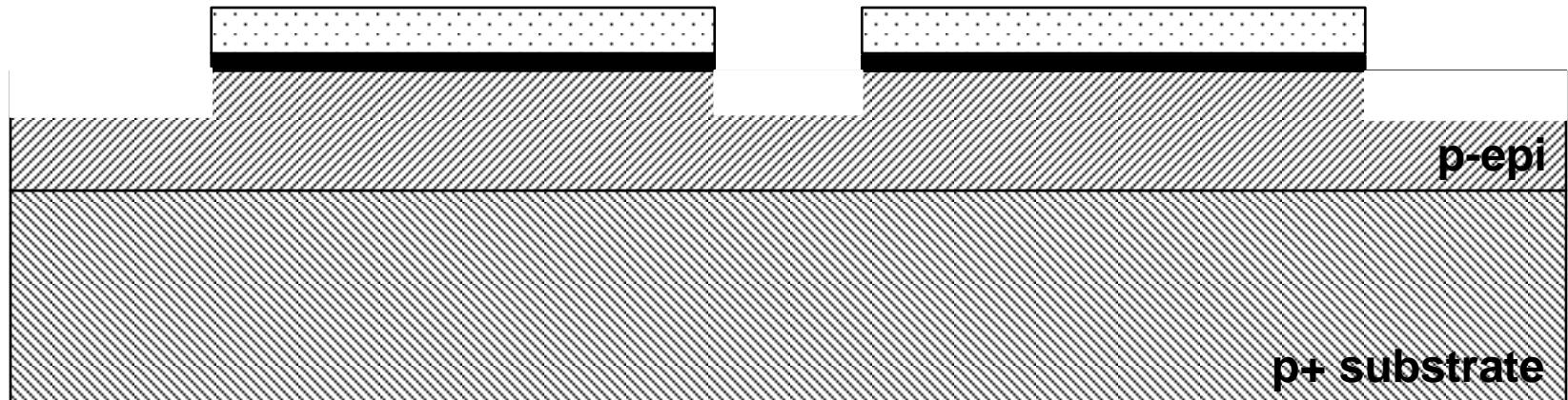
After photolithography

Semiconductor Manufacturing



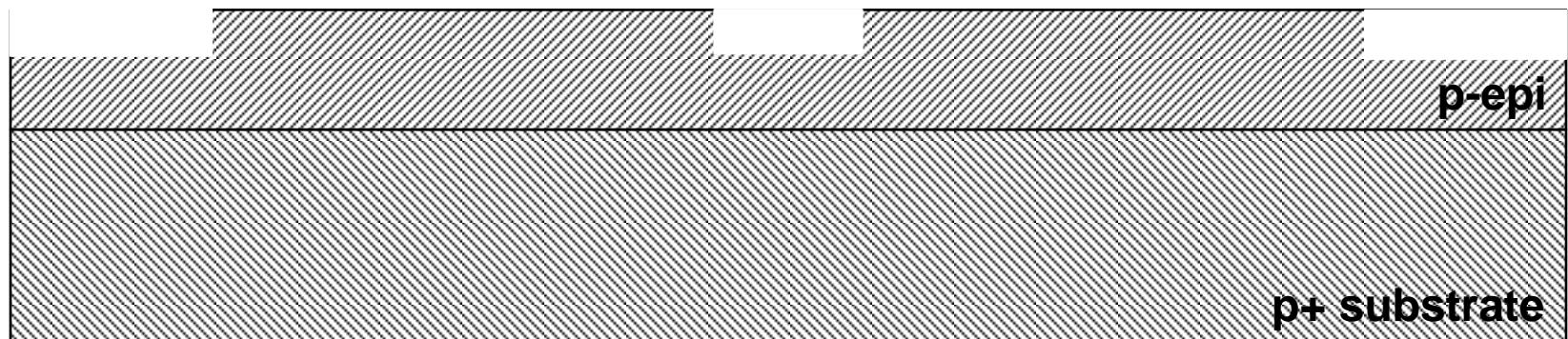
Remove mask

Semiconductor Manufacturing



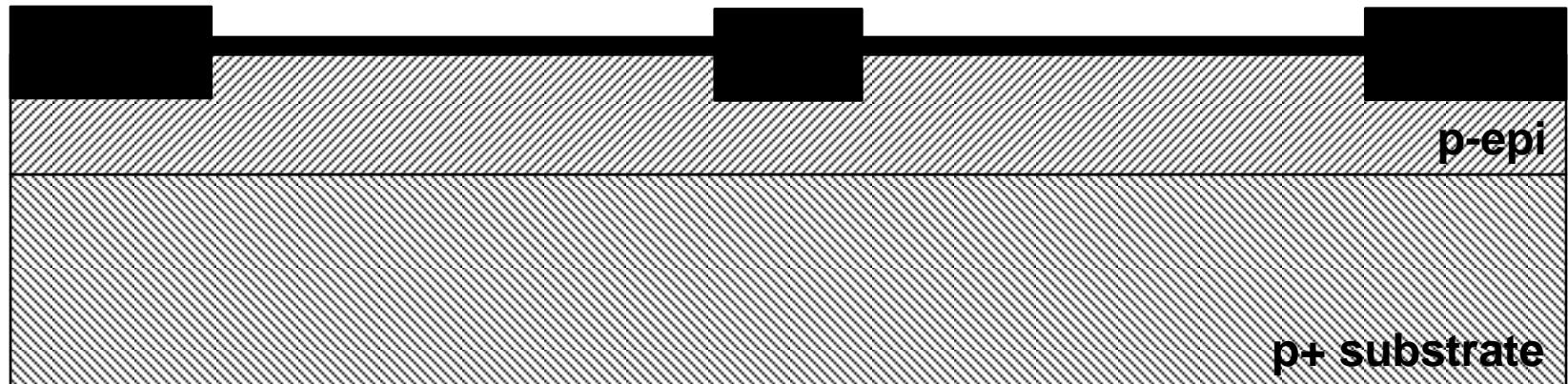
Etching

Semiconductor Manufacturing



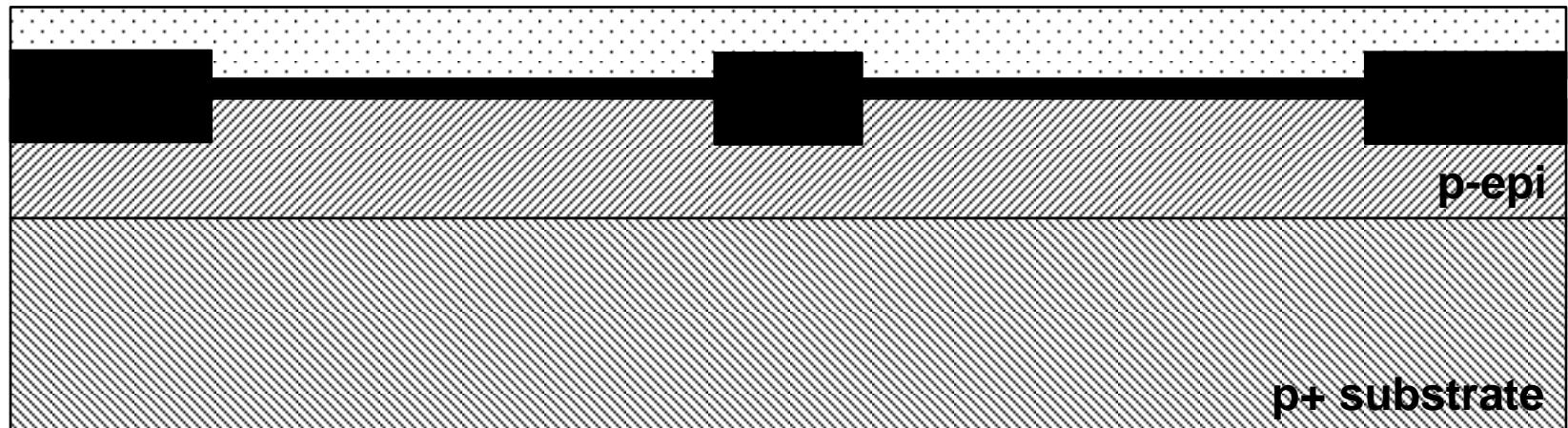
Etching

Semiconductor Manufacturing



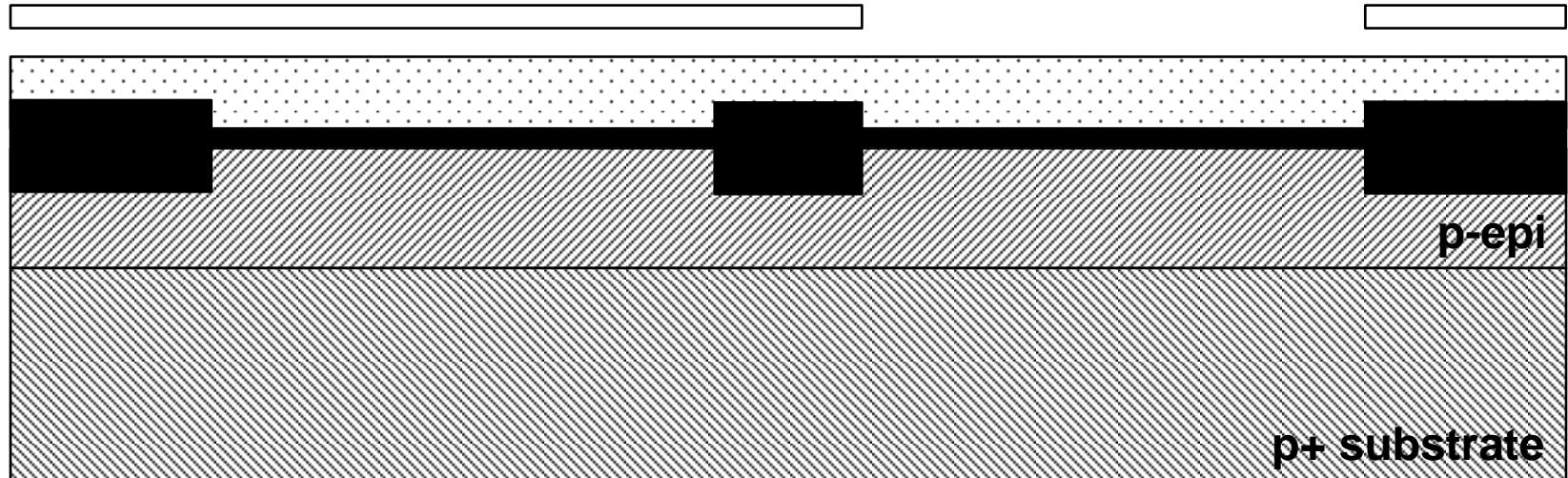
Oxide deposition

Semiconductor Manufacturing



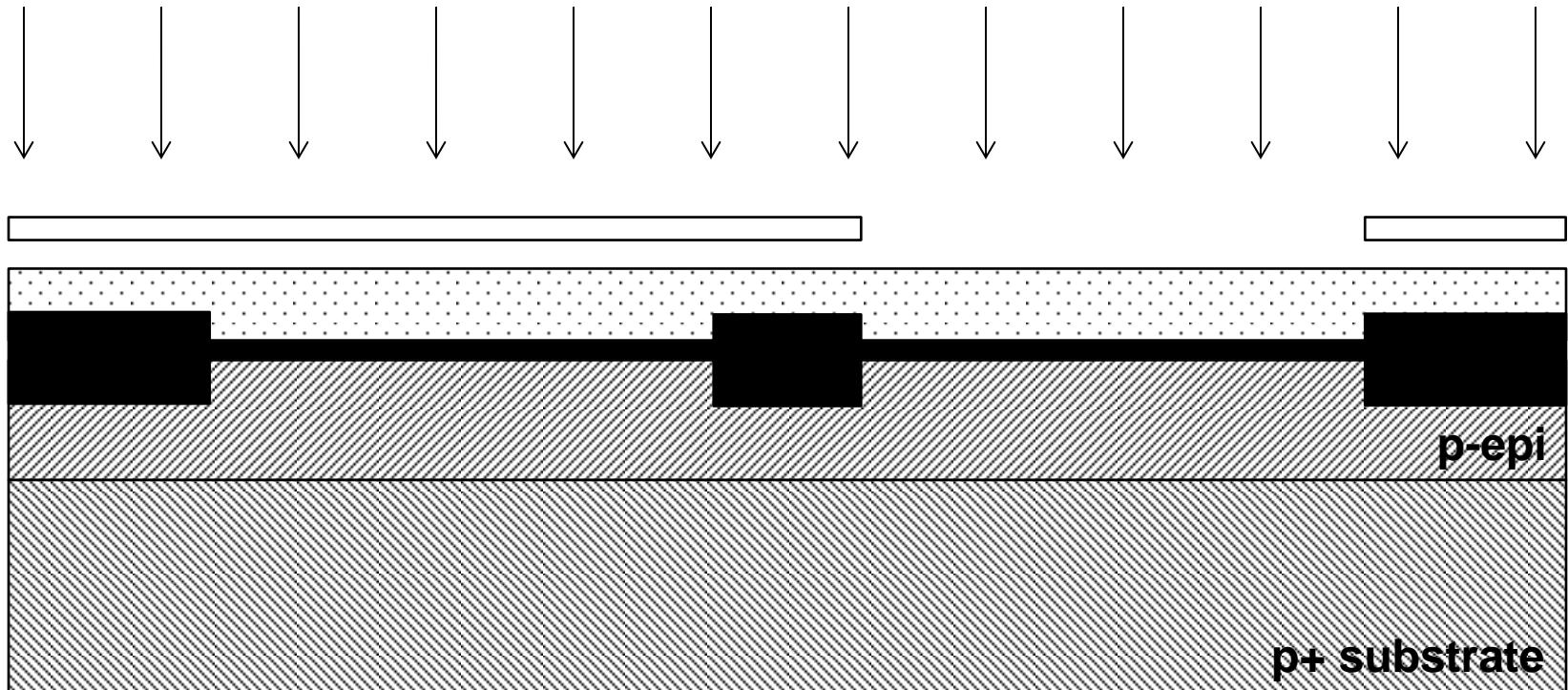
Photoresist

Semiconductor Manufacturing



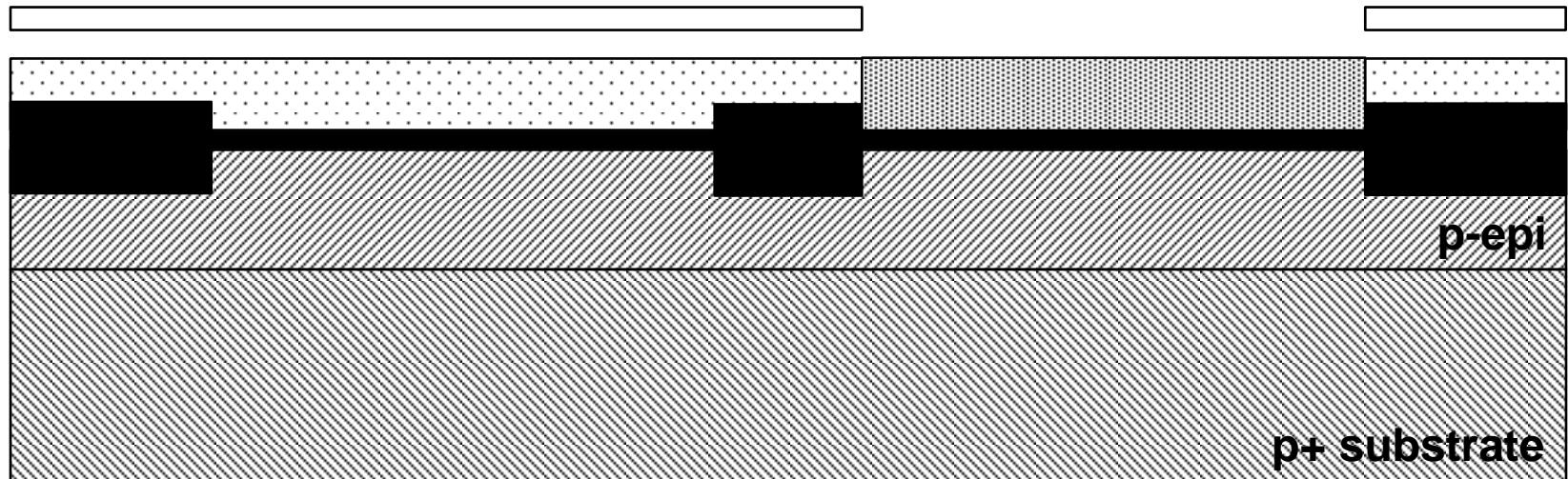
Mask

Semiconductor Manufacturing



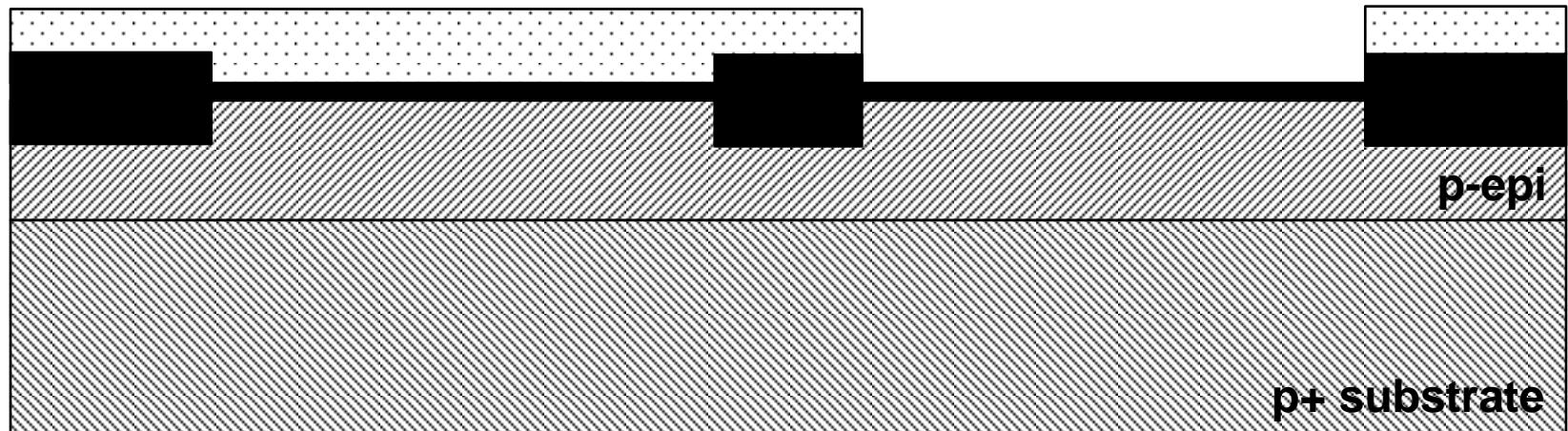
Photolithography

Semiconductor Manufacturing



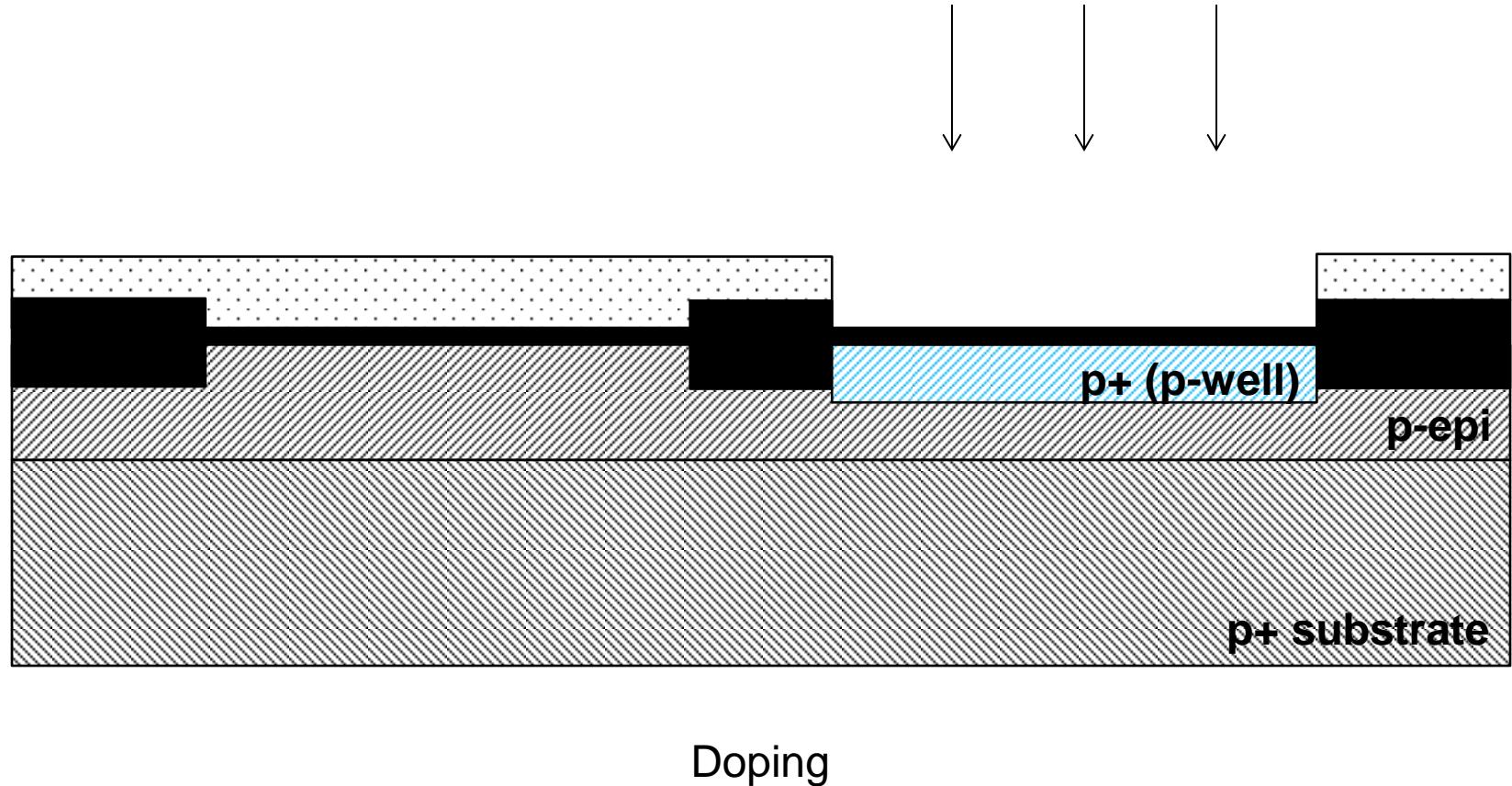
After photolithography

Semiconductor Manufacturing



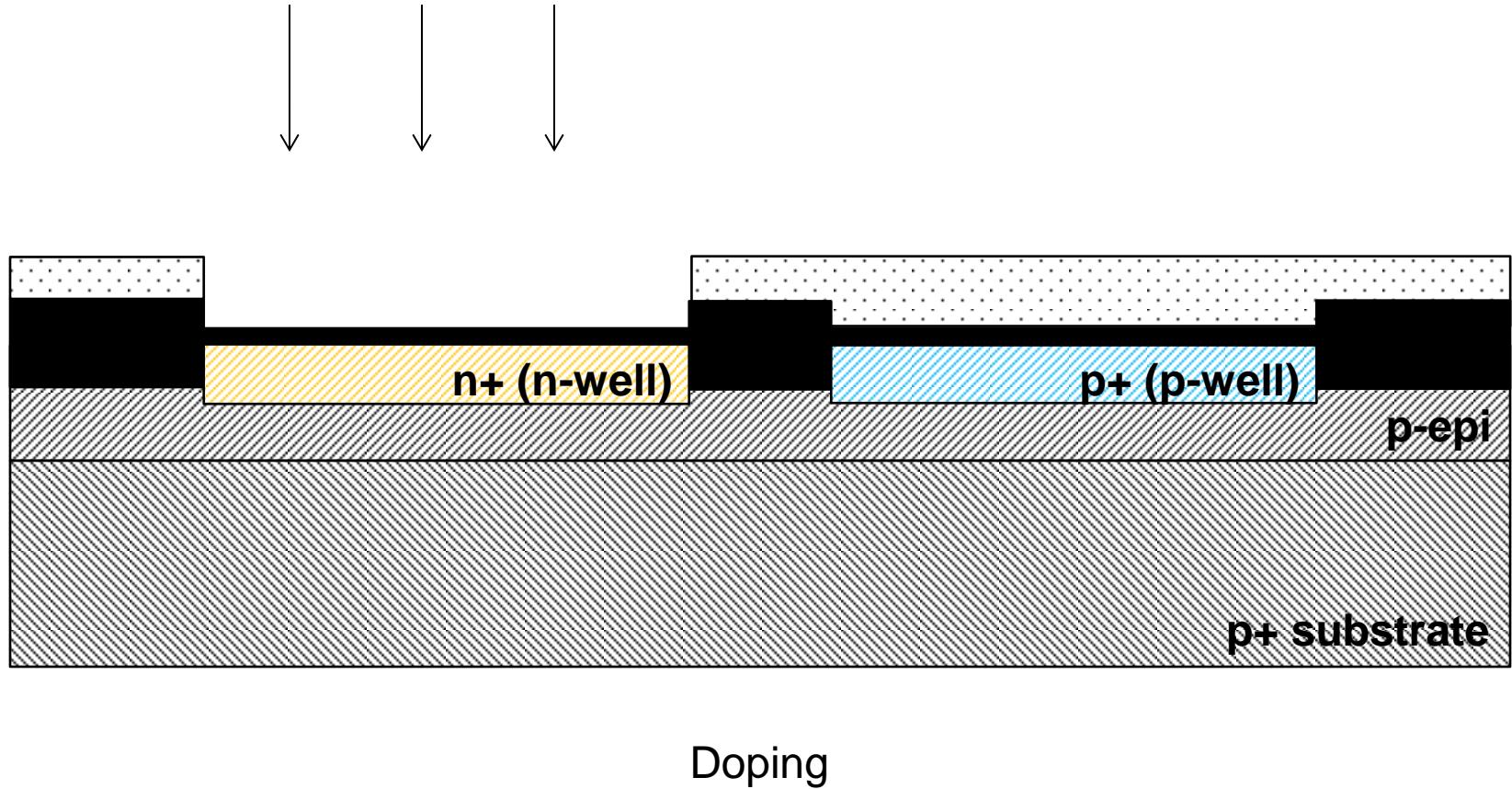
Etch

Semiconductor Manufacturing



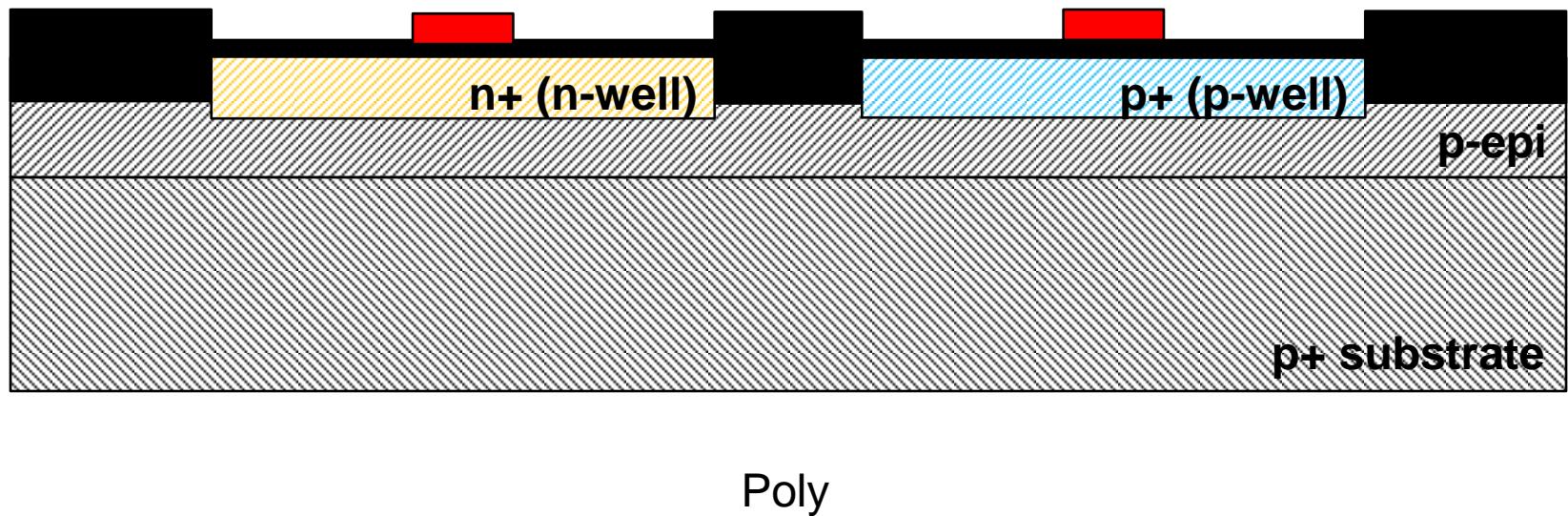
Doping

Semiconductor Manufacturing

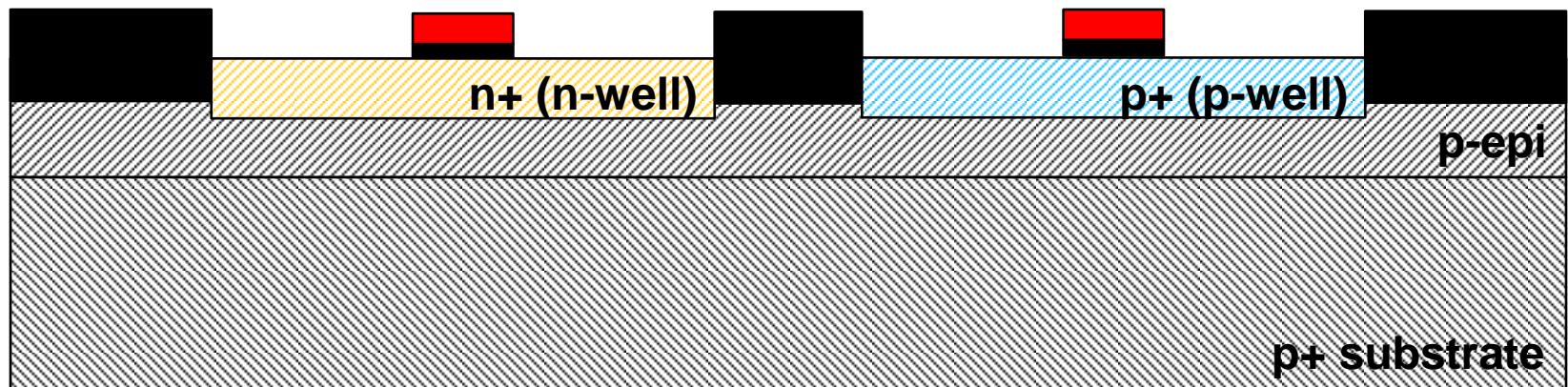


Doping

Semiconductor Manufacturing

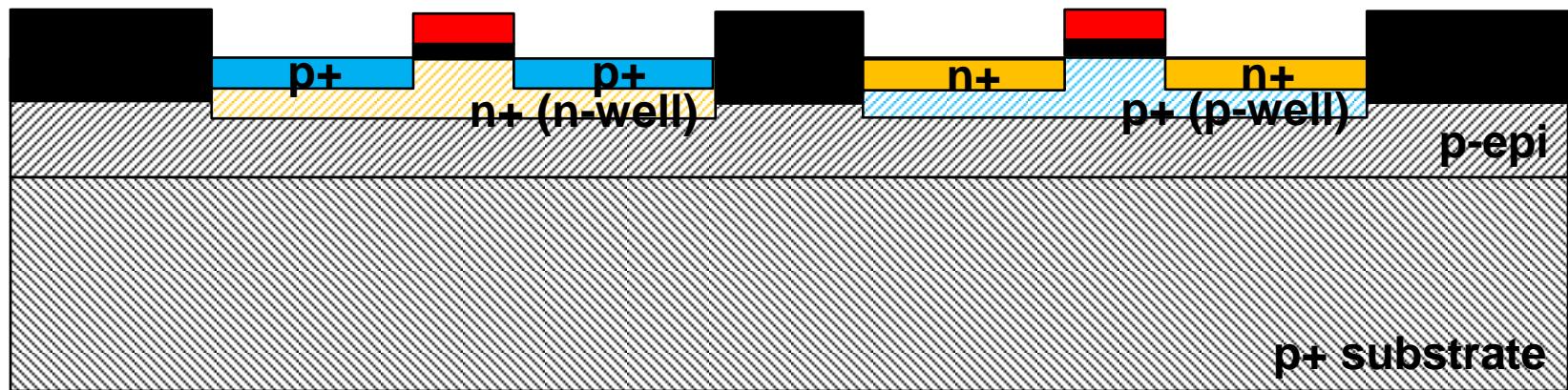


Semiconductor Manufacturing



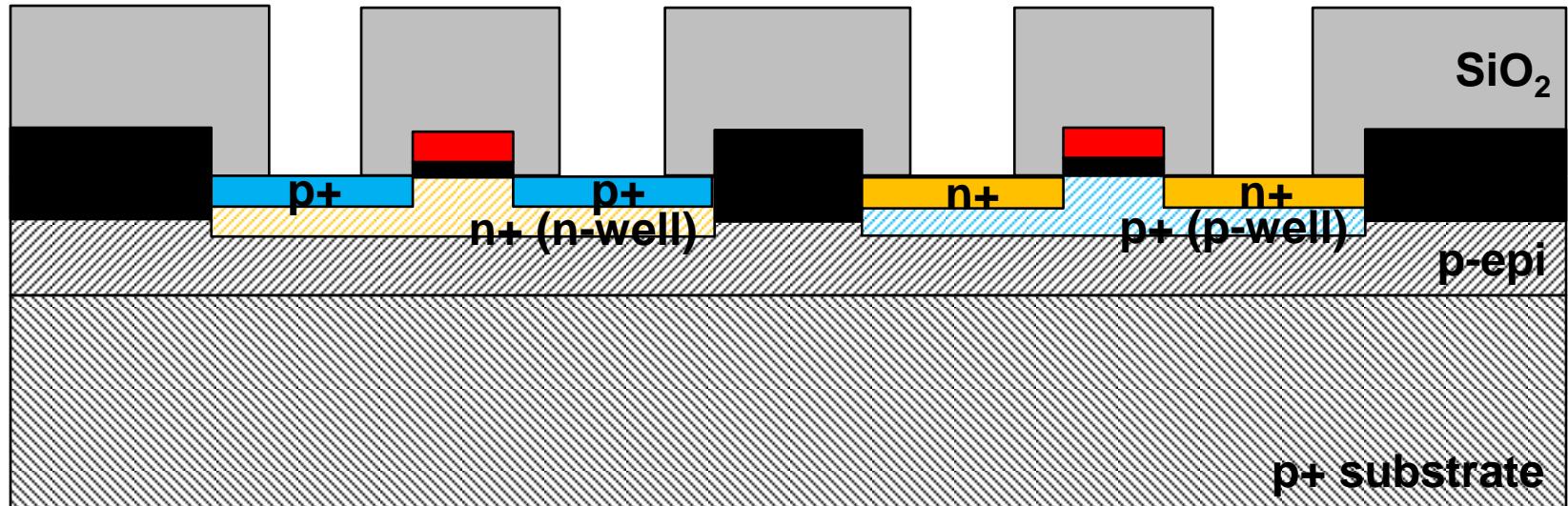
Etch

Semiconductor Manufacturing

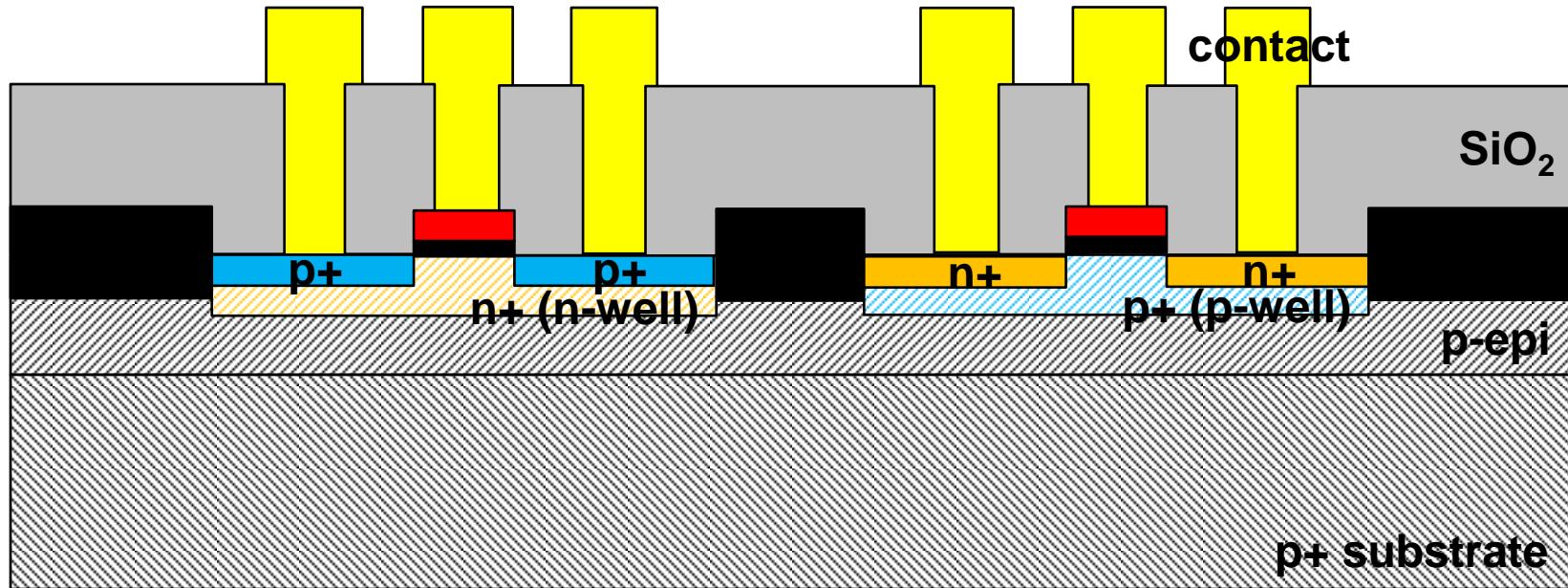


Doping

Semiconductor Manufacturing

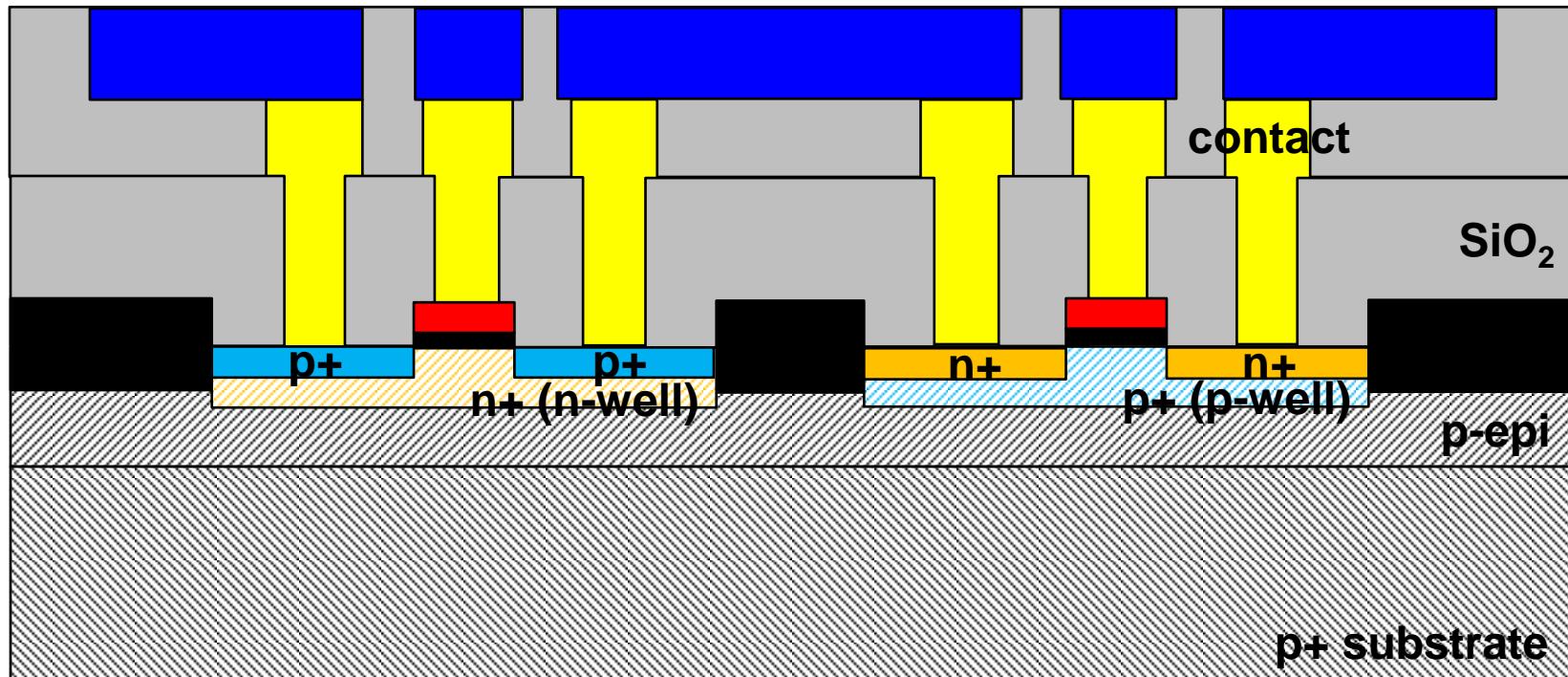


Semiconductor Manufacturing

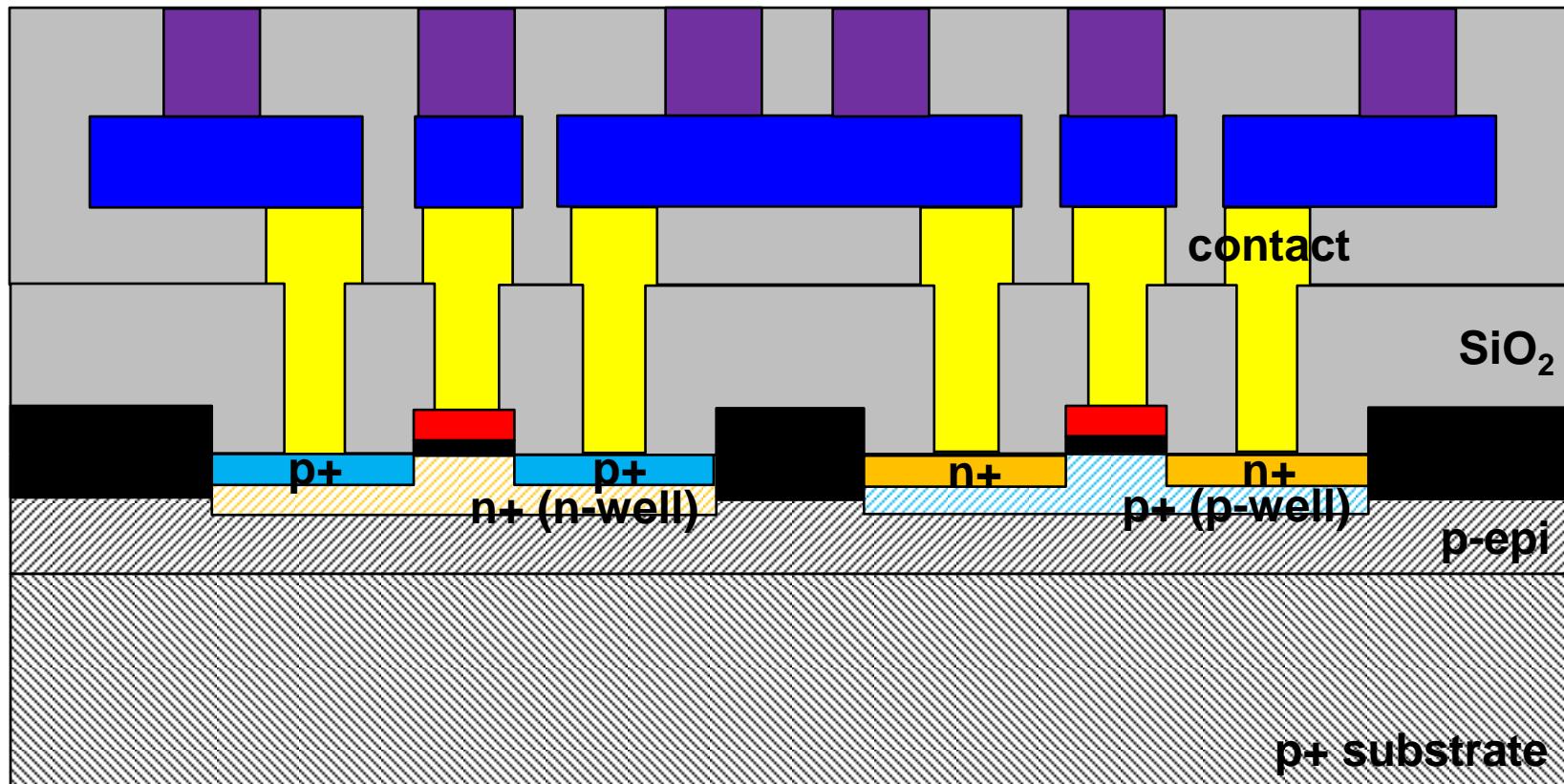


Contact

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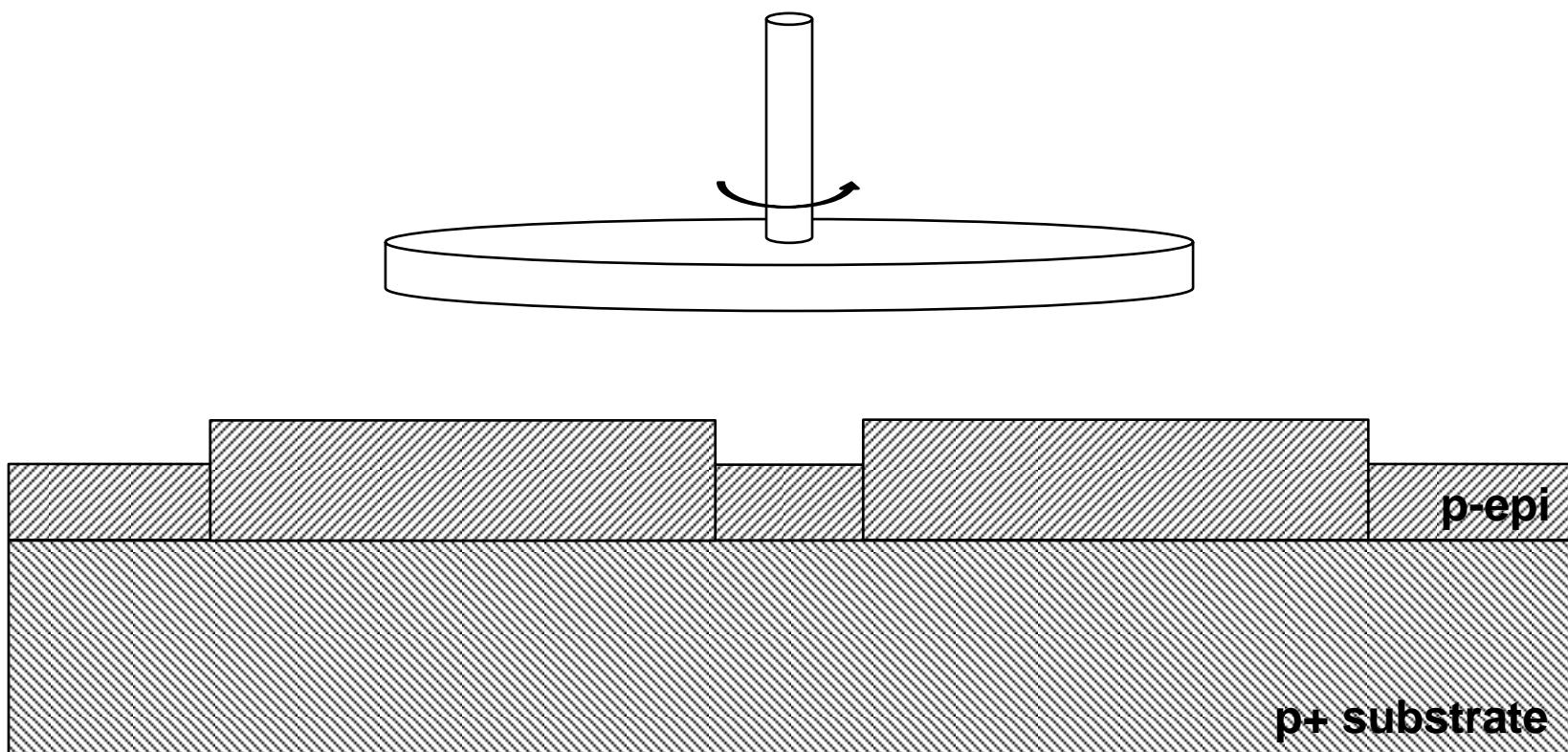


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