EE434
ASIC & Digital Systems

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Spring 2016

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Lecture 1

Course Overview & Introduction to VLSI

Theme of the Course

- How to design, analyze, and test a complex application-specific integrated circuit (ASIC)

- At the end of this semester, you will be able to
  - Understand how a VLSI chip works
  - Design complex digital VLSI circuits and systems
  - Understand basic theories behind VLSI
  - Analyze VLSI circuits and systems
  - Test VLSI circuits and systems

Target of the Course

- We will follow a bottom-up approach
- We are not going to discuss much about devices
- Rather we will learn more system level issues, both design and analysis
- But to appreciate the problems related to the design of a big digital system we need to learn about circuits and gates

Broad Categories

- Four broad topics
  - Circuit Design Styles
    - CMOS and other circuit families, delay, power, clock, interconnects
  - Implementation Methods
    - Custom & Semicustom design
    - Standard cell-based design
    - FPGAs
  - Physical design of CMOS VLSI circuits and systems
    - VHDL/Verilog
    - Design
    - Analysis
    - Optimization
  - Testing

Schedule

- Week 1 (1/11,13,15): Introduction to VLSI, VHDL
- Week 2 (1/20, 22): VHDL, Verilog
- Week 3 (1/25,27,29): CMOS transistors, switches, gates
- Week 4 (2/1, 3, 5): CMOS inverter, combinational logic
- Week 5 (2/8, 10, 12): CMOS design styles, sequential logic
- Week 6 (2/17, 19): Characterization and performance estimation
- Week 7 (2/22, 24, 26): Characterization and performance estimation (continued)
- Week 8 (2/29, 3/2, 4): Midterm 1, layout, simulation, optimization
- Week 9 (3/7, 9, 11): Interconnects, timing analysis
- Week 10 (3/14 – 18): Spring break
- Week 11 (3/21, 23, 25): Memory, design methodologies, datapath design
- Week 12 (3/28, 30, 4/1): Synthesis, physical design, arithmetic units
- Week 13 (4/4, 6, 8): Midterm 2, testing
- Week 14 (4/11, 13, 15): Testing
- Week 15 (4/18, 20, 22): Testing
- Week 16 (4/25, 27, 29): Testing
- 5/5 (Thu): Final exam (1pm)

References

- FPGA-BASED System Design by Wayne Wolf, Prentice Hall, 2004, ISBN 0-13-142461-0
- Analysis and Design of Digital Integrated Circuits by Hodges, Jackson, and Saleh, 3/E, 2003, McGraw Hill, ISBN 0072283653
- CMOS VLSI Design: A Circuits and Systems Perspective by Weste and Harris, 4/E, 2010, Addison-Wesley, ISBN 0321547748
- Digital Integrated Circuits by Rabaey, Chandrakasan, and Nikolic, 2E, 2003, Prentice Hall, ISBN 0130909963
- Introduction to VLSI Circuits and Systems by Uyemura, 1E, 2001, Wiley, ISBN 0471127043
- CMOS Logic Circuit Design by Uyemura, 1999, Springer, ISBN 0387781641
- Application-Specific Integrated Circuits by Smith, 1997, Addison-Wesley, ISBN 0201500221
- Digital Systems Testing and Testable Design, 1990, IEEE Press, ISBN 0-7803-1062-4

- Extra reading materials will be supplied in the class.

Assignments

- There will be several homework assignments.
  - Due dates will be mentioned when handed out.
  - Late submission penalty: -5% per day. -80% max.

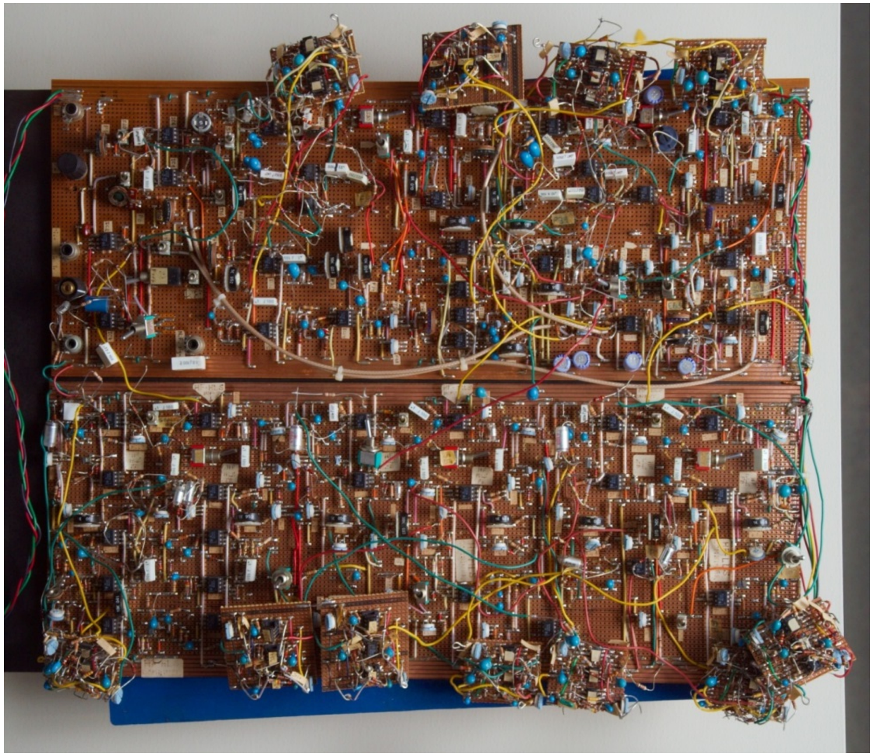
- Lab and HW are very important parts of this course.
  - Lab assignments will involve HDL coding
    - No worries! You will learn VHDL/Verilog step by step.
  - You will learn Synopsys and Cadence tools
    - No worries! Detailed tutorials will be provided.
  - EME 205 is the lab for this course
  - You will be allowed to work any time in the lab
  - TA will be available only in fixed hours

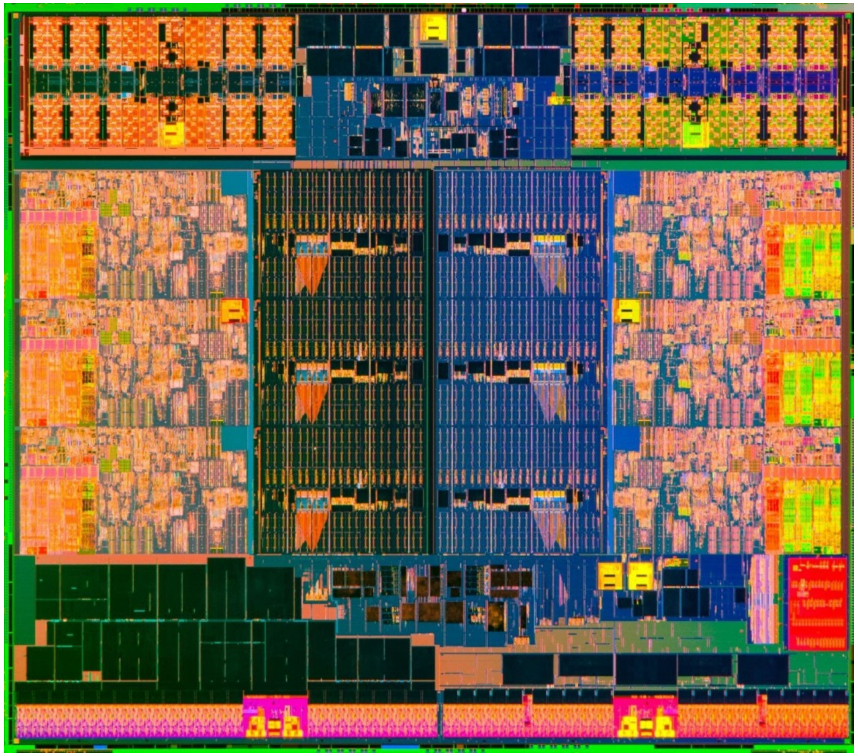
Course Website

- Important announcements will be posted in the course website
  - www.eecs.wsu.edu/~ee434

Discrete Components vs. VLSI

	Discrete components	Integrated circuits
# transistors	10^2	10^9





What is an ASIC?

- **Application Specific Integrated Circuits**

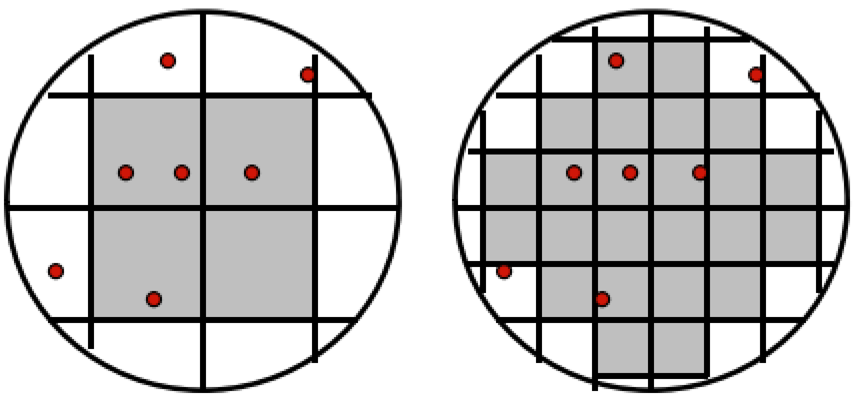
- **Integrated Circuits**
  - **All components, passive and active are integrated on a single semiconductor substrate**
    - **Higher speed**
    - **Lower power**
    - **Physically smaller**

- **Integration reduces manufacturing cost**

Yield

- Defects

Yield = 1/4



Yield = 19/24

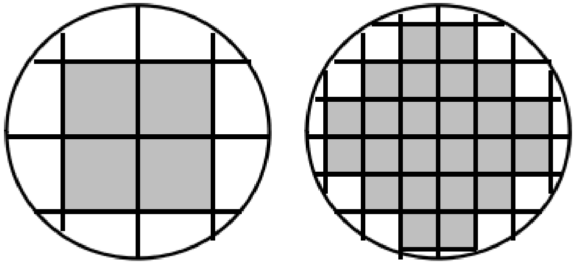
Yield

- Cost (die) = $\dfrac{\text{Cost (wafer)}}{\text{\# good dies per wafer}} = \dfrac{\text{Cost (wafer)}}{(\text{\# dies per wafer})\cdot(\text{die yield})}$

- Yield = $\dfrac{\text{\# good dies per wafer}}{\text{total \# dies per wafer}}$

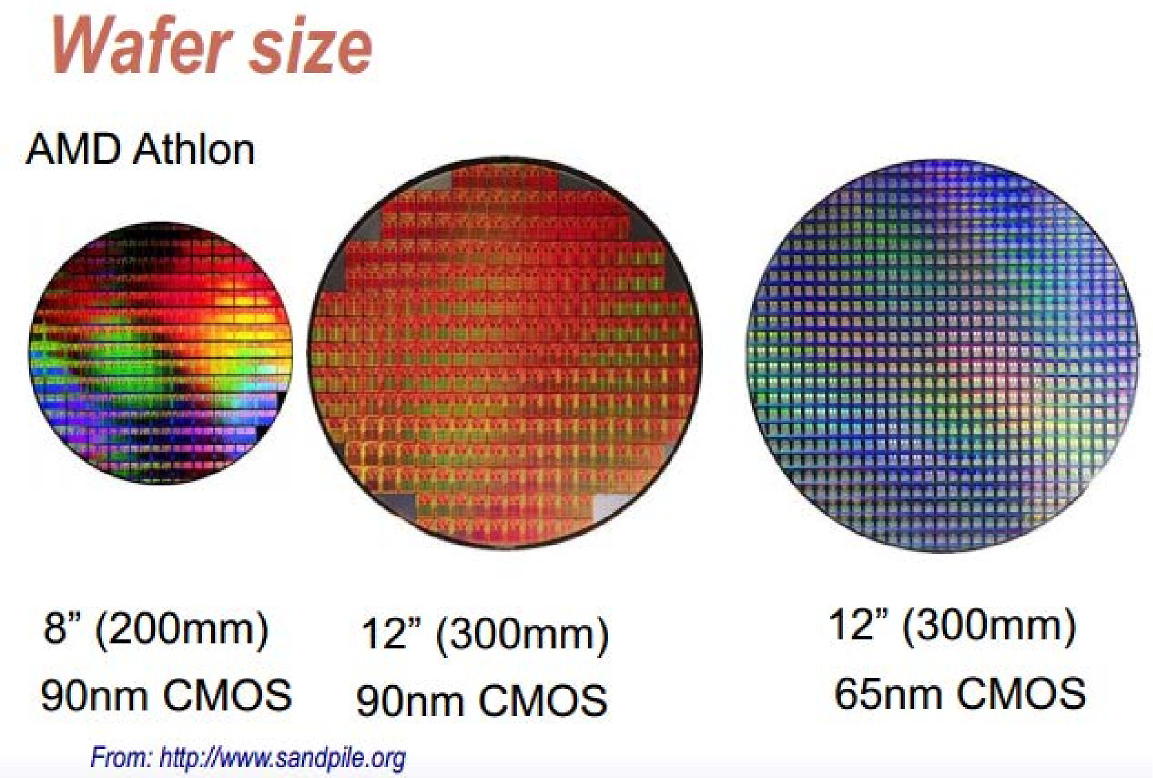
- # dies per wafer = $\dfrac{\pi(\text{wafer diameter}/2)^2}{\text{die area}} - \dfrac{\pi(\text{wafer diameter})}{\sqrt{2\cdot\text{die area}}}$

- # dies per unit wafer area = $\dfrac{1}{\text{die area}} - \dfrac{\sqrt{2}}{(\text{wafer radius})\sqrt{\text{die area}}}$



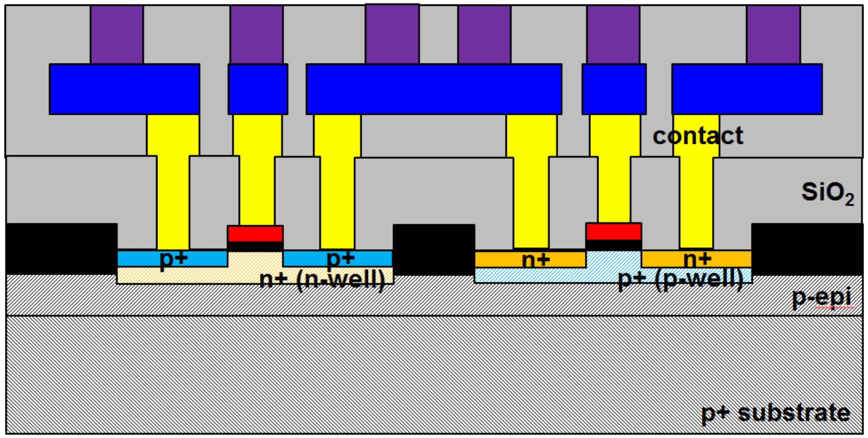
Yield

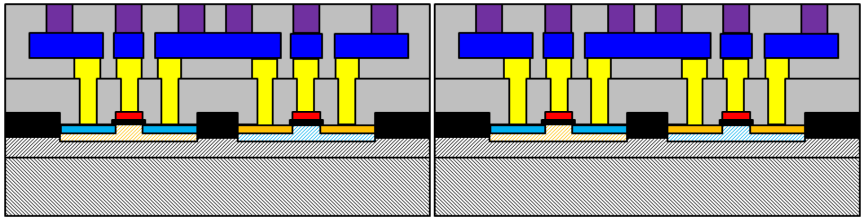
- Need for larger wafer size



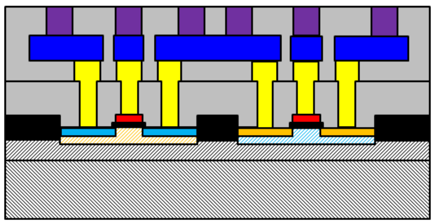
Technology Scaling

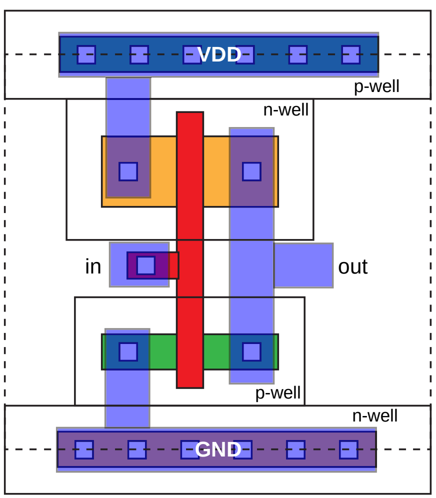
- Integration of more transistors in the same area
  - Higher yield
  - Lower cost
  - More functionality
  - Lower power consumption
- Parasitic RC?



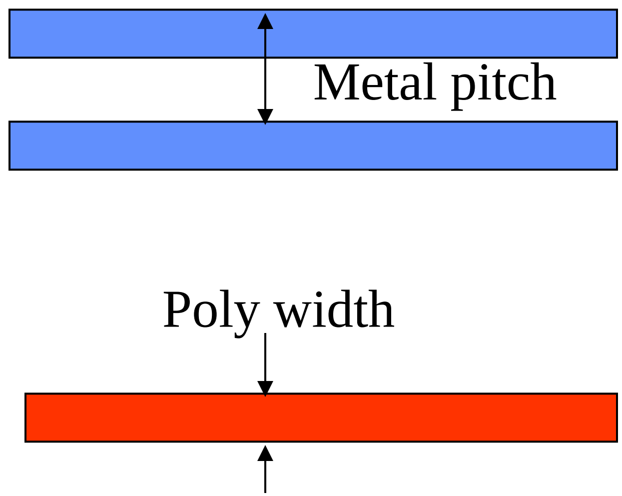


MOS Transistor Scaling
(1974 to present)





Scaling factor **s**=**0.7** per node (0.5x per 2 nodes)



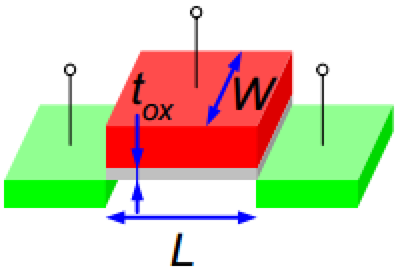
Technology Node set by 1/2 pitch (interconnect)

Gate length (transistor)

Ideal Technology Scaling (constant field)

Quantity	Before Scaling	After Scaling
Channel Length	L	$L' = L * s$
Channel Width	W	$W' = W * s$
Gate Oxide thickness	t_{ox}	$t'_{ox} = t_{ox} * s$
Junction depth	x_j	$x'_j = x_j * s$
Power Supply	V_{dd}	$V_{dd}' = Vdd * s$
Threshold Voltage	V_{th}	$V'_{th} = V_{th} * s$
Doping Density, p n+	N_A N_D	$N_A' = N_A / s$ $N_D' = N_D / s$

Technology Scaling (Device)



- Area: W $\cdot L \rightarrow \boldsymbol{s^2} W \cdot L$

- Capacitance
  - $W \cdot L \cdot c_{ox} = (W \cdot L) \cdot \frac{\varepsilon_{ox}}{t_{ox}} \rightarrow (s^2 WL) \cdot \frac{\varepsilon_{ox}}{s \cdot t_{ox}} = (\boldsymbol{s} WL) \cdot \frac{\varepsilon_{ox}}{t_{ox}}$

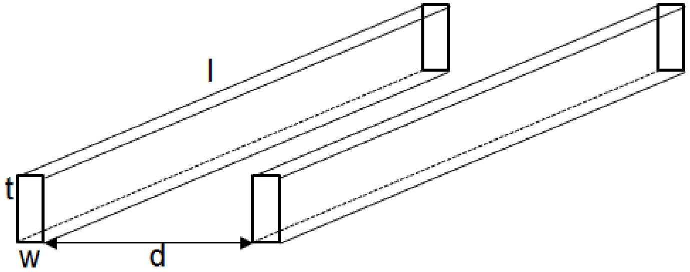
- Transistor delay
  - $t_p \propto \frac{C_L V_{DD}}{k(V_{DD}-V_T)^2} \rightarrow \frac{(sC_L)(sV_{DD})}{\left(\mu \cdot c_{ox} \cdot \frac{W}{L}\right)(sV_{DD}-sV_T)^2} = \frac{(sC_L)(sV_{DD})}{(\mu \cdot \frac{\varepsilon_{ox}}{s \cdot t_{ox}} \cdot \frac{sW}{sL})(sV_{DD}-sV_T)^2} = \boldsymbol{s}(\frac{C_L V_{DD}}{k(V_{DD}-V_T)^2})$

- Power consumption
  - $P \propto \alpha f C_L {V_{DD}}^2 \rightarrow \alpha(\frac{f}{s})(sC_L)(s^2 {V_{DD}}^2) = \boldsymbol{s^2}(\alpha f C_L V_{DD})$

- Power / Area = **1**

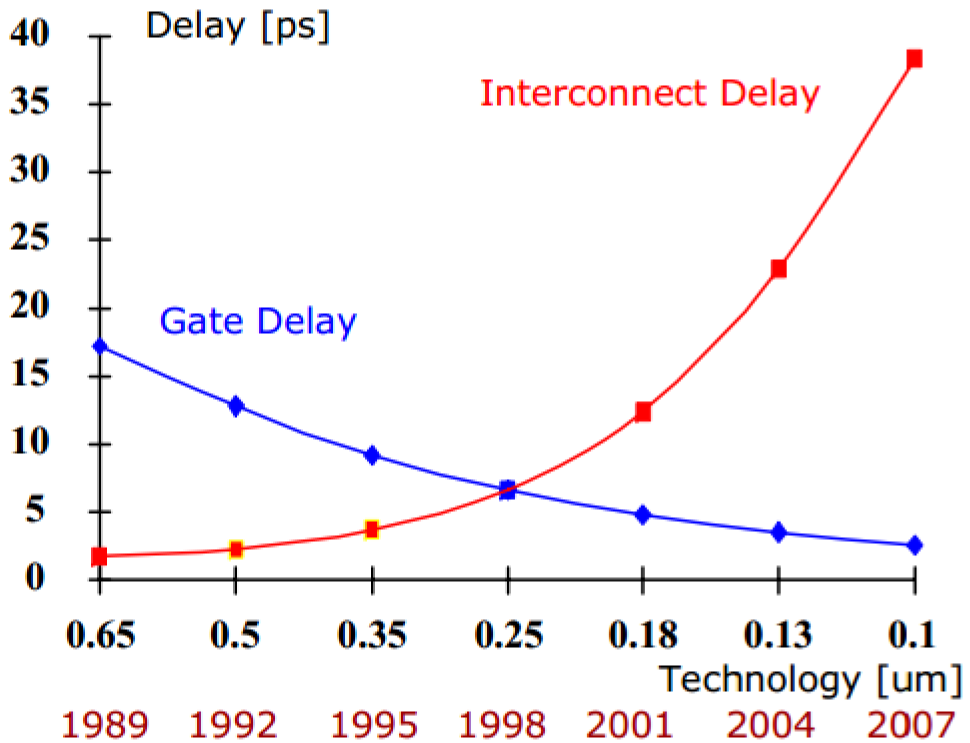
Technology Scaling (Interconnect)

- Width: W $\rightarrow \boldsymbol{s}W$
- Thickness: t $\rightarrow \boldsymbol{s}t$
- Spacing: $d \rightarrow \boldsymbol{s}d$
- Length: $l \rightarrow \boldsymbol{s}l$



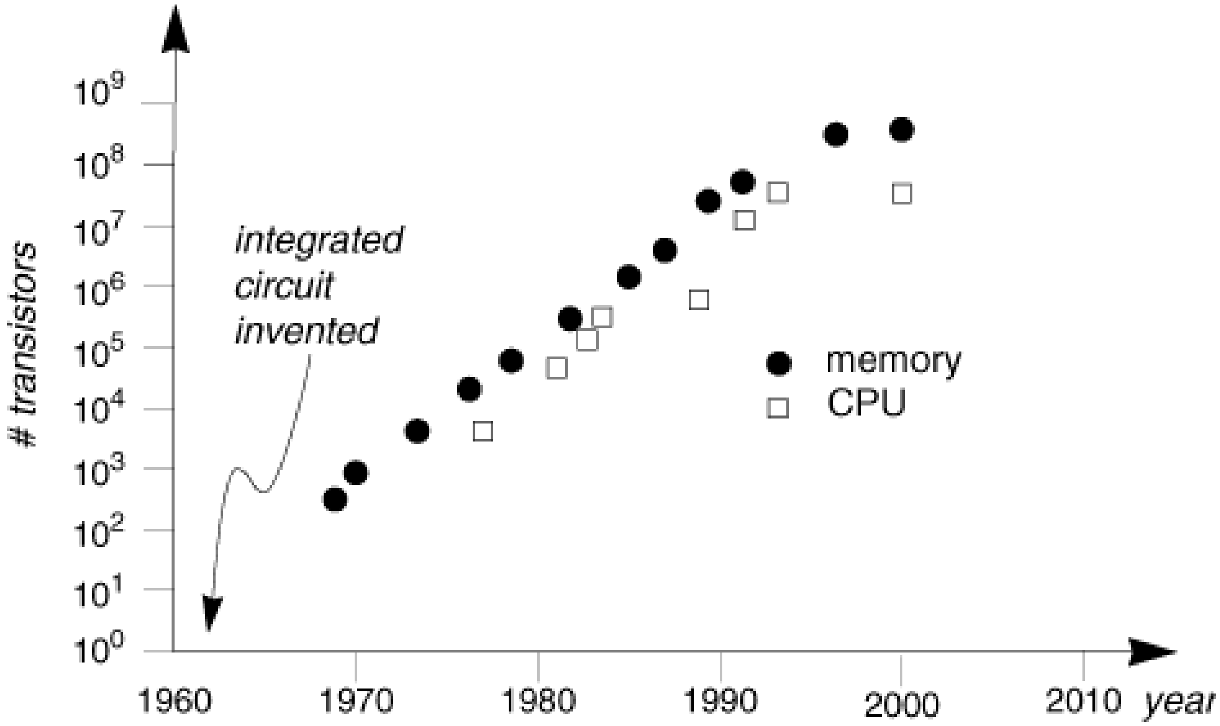
- Resistance: $\rho\frac{l}{tw} = \rho\frac{sl}{(st)(sw)} = \frac{1}{\boldsymbol{s}}\rho\frac{l}{tw}$
- Capacitance: $\varepsilon\frac{tl}{d} = \varepsilon\frac{(st)(sl)}{sd} = \boldsymbol{s}\varepsilon\frac{tl}{d}$
- Interconnect delay: $\propto RC = 1$

Technology Scaling



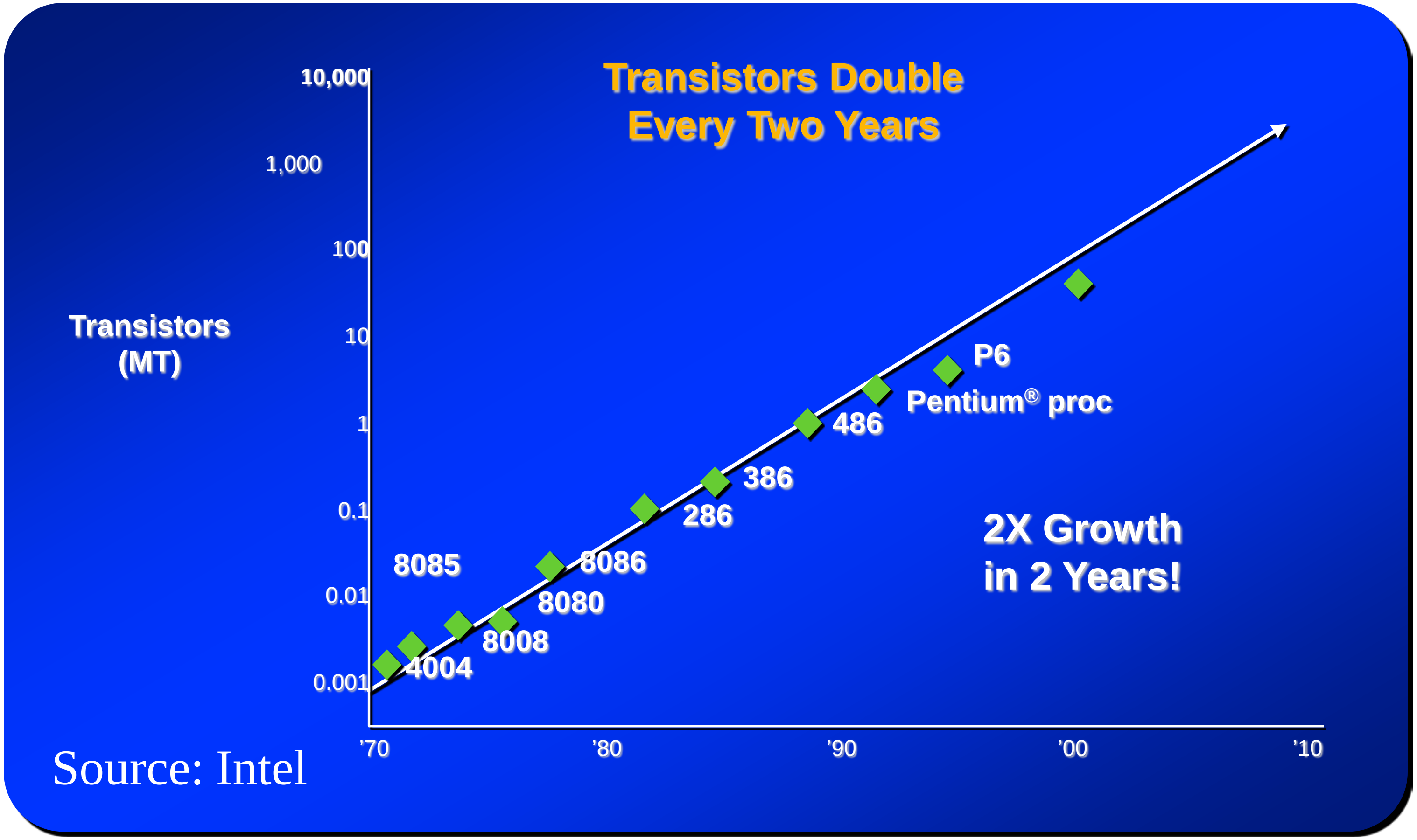
Source: SIA Roadmap

Moore’s Law



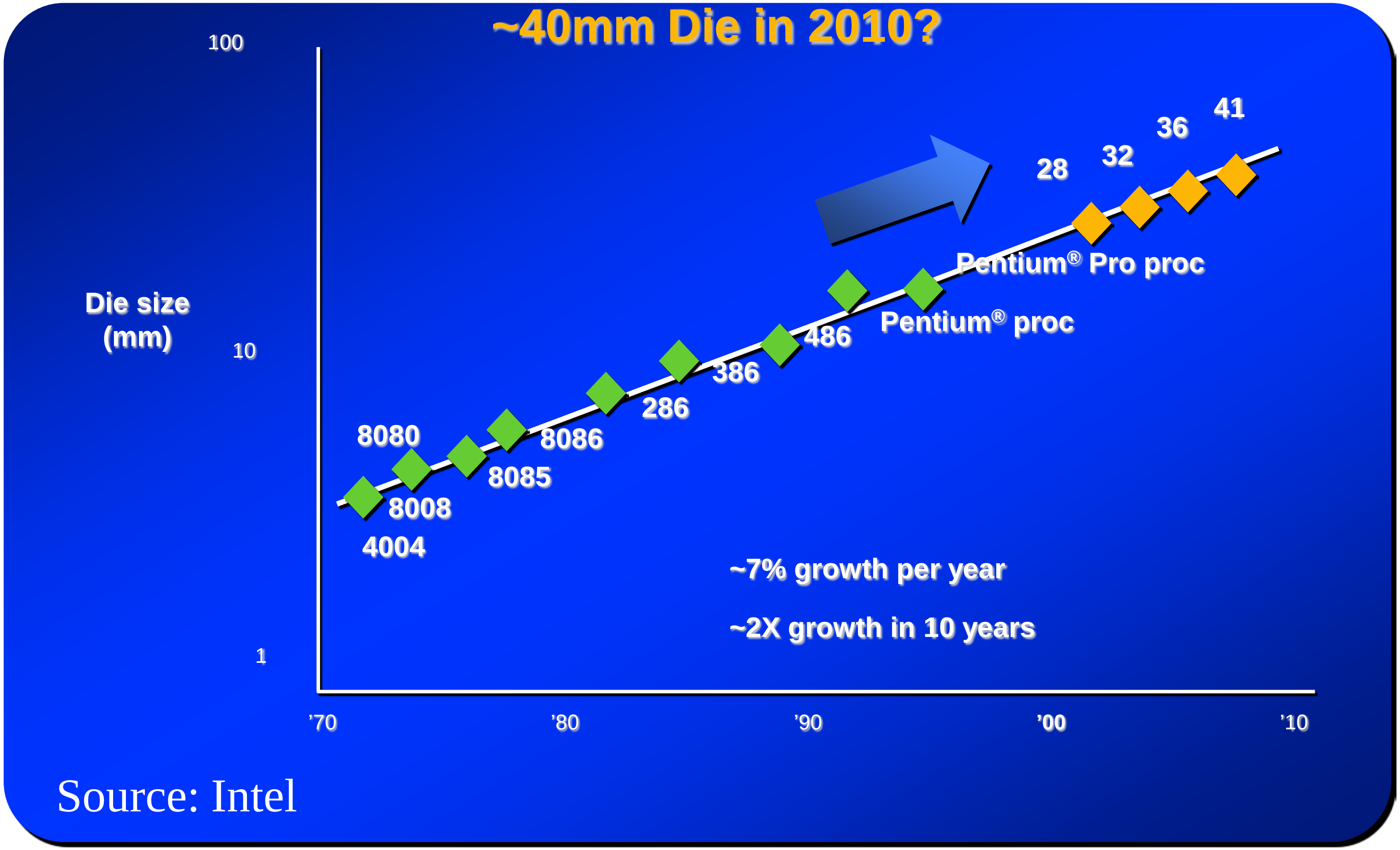
- Number of transistors per chip would double every 18 months.

MPU Trends - Moore's Law

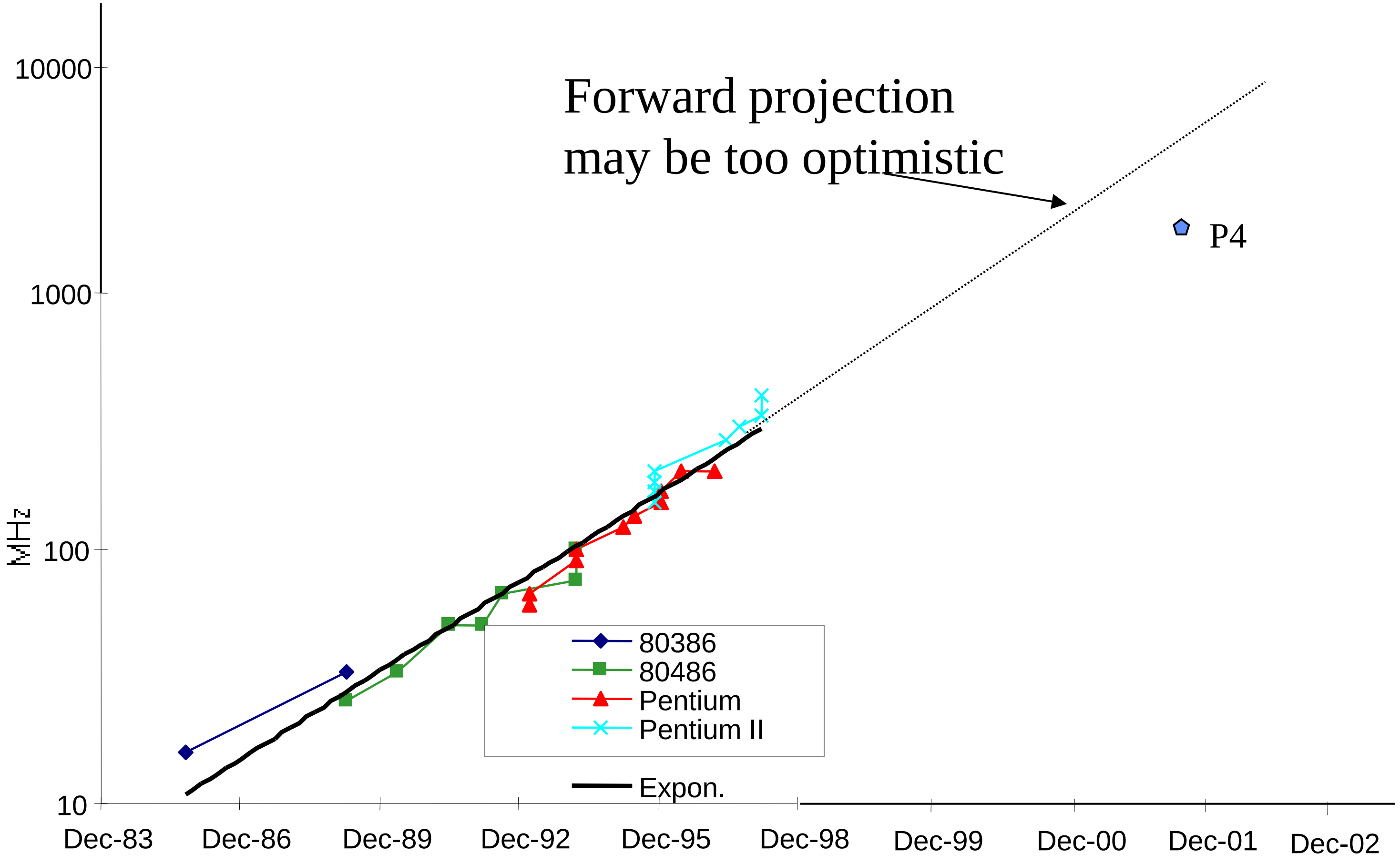


Source: Intel

More MPU Trends

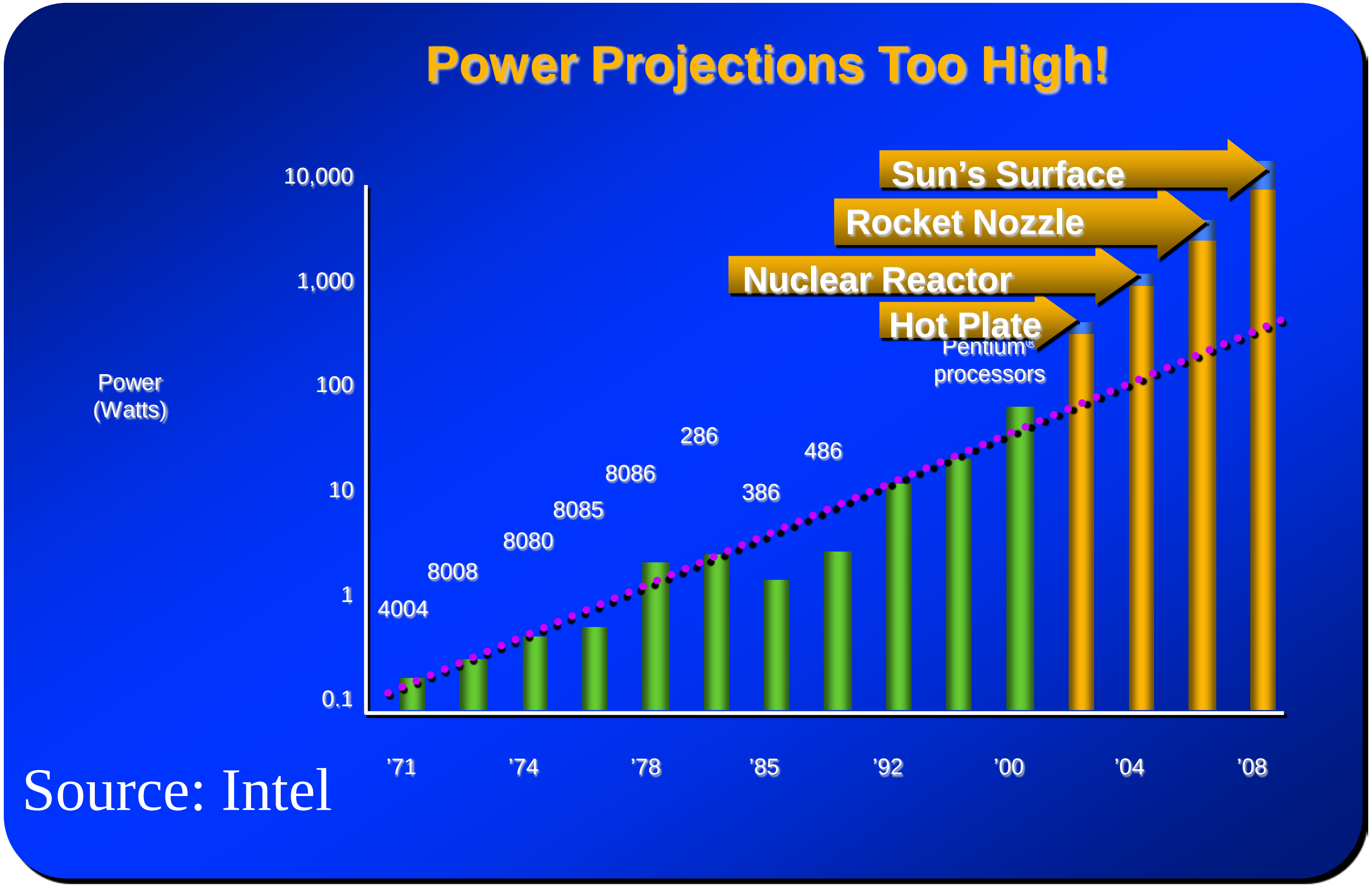


MPU Clock Frequency Trend



Intel: Borkar/Parkhurst

What about power in the future?



Recent Trends

- 1.5GHz Itanium chip (Intel), 410M tx, 374mm^2 , 130W@1.3V
- 1.1 GHz POWER4 (IBM), 170M tx, 115W@1.5V
  - if these trends continue, power will become unmanageable
- 150Mhz Sony Graphics Processor, 7.5M tx (logic) + 280M tx (memory) = 288M tx, 400mm^2 10W@1.8V
  - if trend continues, most designs in the future will have a high percentage of memory
- Single-chip Bluetooth transceiver (Alcatel), 400mm^2, 150mW@2.5V
  - required 30 designers over 2.5 years (75 person-years)
  - if trend continues, it will be difficult to integrate larger systems on a single chip in a reasonable time
- **Intel's 80-core chip**
  - In 65-nm technology with 80 single-precision, floating point cores delivers performance in excess of a teraflops while consuming less than 100 w
  - Tilera Corporation (Dedicated Multi-core company)
  - Multi-core design will dominate

Technology Nodes 1999-2019

1999	2001	2004	2007	2010	2013	2016	2019
180nm	130nm	90nm	65nm	45nm	32nm	22nm	16nm

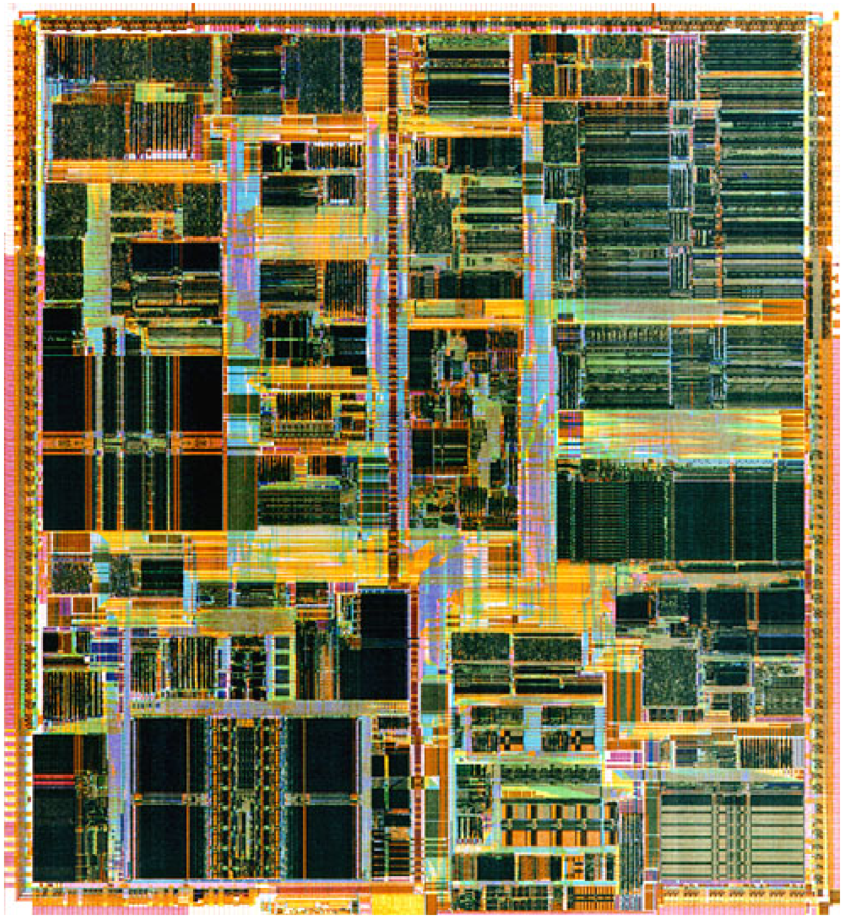
0.7x 0.7x

0.5x

N-1 N N+1

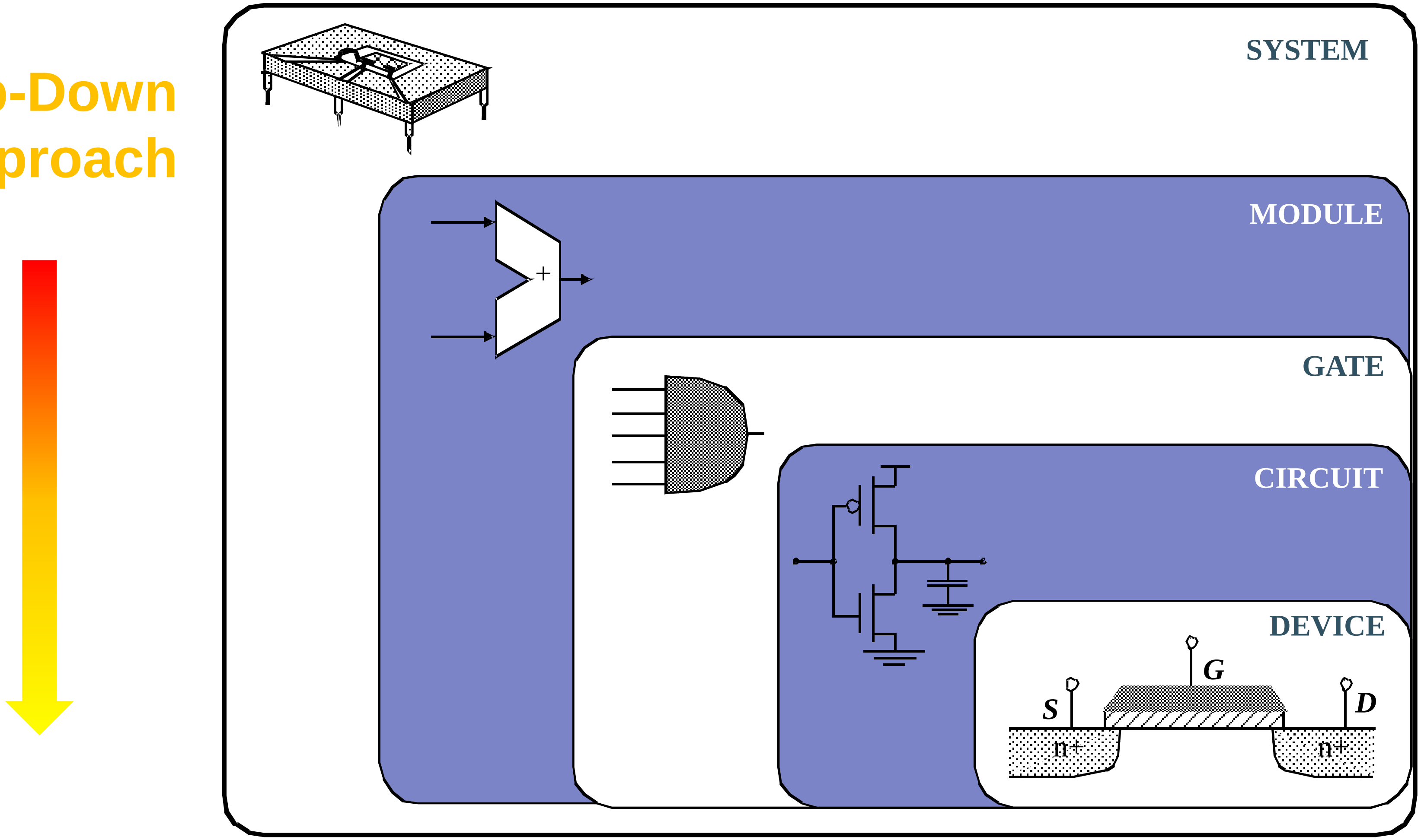
Two year cycle between nodes until 2001, then 3 year cycle begins.

Intel Pentium (IV) microprocessor



Design Abstraction Levels

Top-Down Approach



ASIC Realization Process

Customer's need

Determine requirements

Write specifications

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer