EE434
ASIC & Digital Systems

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Lecture 3

More on CMOS Gates

Ref: Textbook chapter 2

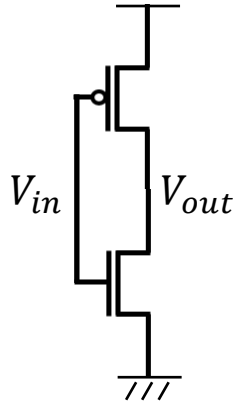
Some of the slides are adopted from Digital Integrated Circuits by Jan M Rabaey

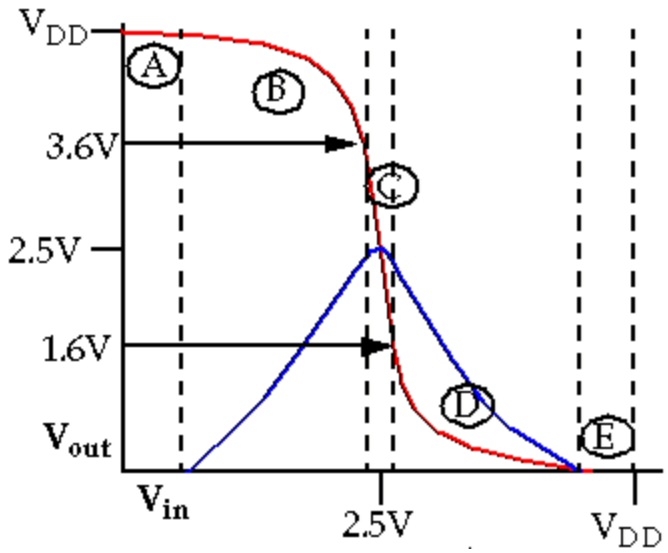
CMOS Inverter – DC Characteristics

- Why do we study the DC characteristics of a CMOS inverter?
  - Analyze a CMOS inverter by hand calculation
  - Understand how the transistors operate in a CMOS inverter
  - Understand the influence of β_n and β_p
  - Understand Noise Margin

CMOS Inverter – DC Characteristics

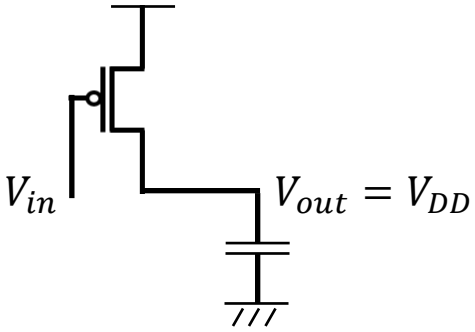
- Region A) $0 \leq V_{in} \leq V_{tn}$
- Region B) $V_{tn} \leq V_{in} < \frac{V_{DD}}{2}$
- Region C) $V_{in} = \frac{V_{DD}}{2}$
- Region D) $\frac{V_{DD}}{2} < V_{in} \leq V_{DD} - |V_{tp}|$
- Region E) $V_{DD} - |V_{tp}| < V_{in}$

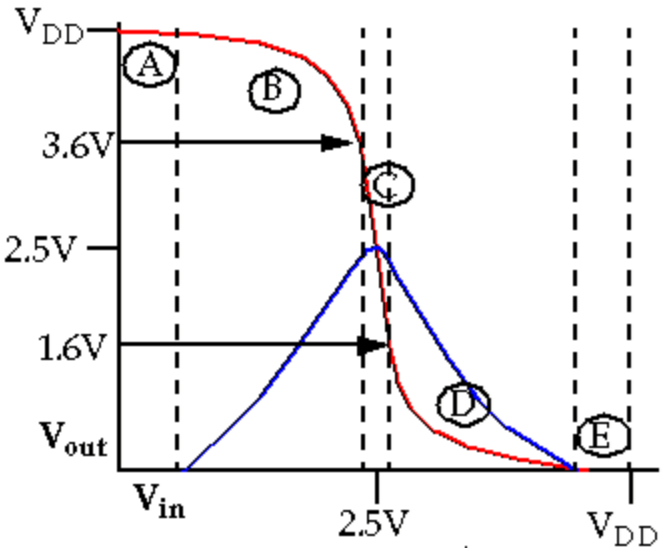




CMOS Inverter – DC Characteristics

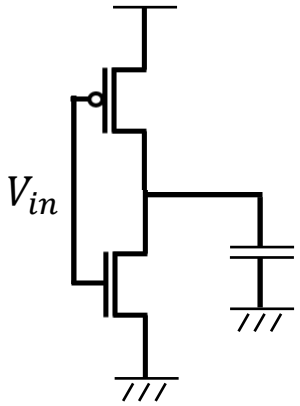
- Region A) $0 \leq V_{in} \leq V_{tn}$
  - NMOS: Cut-off
  - PMOS: Linear

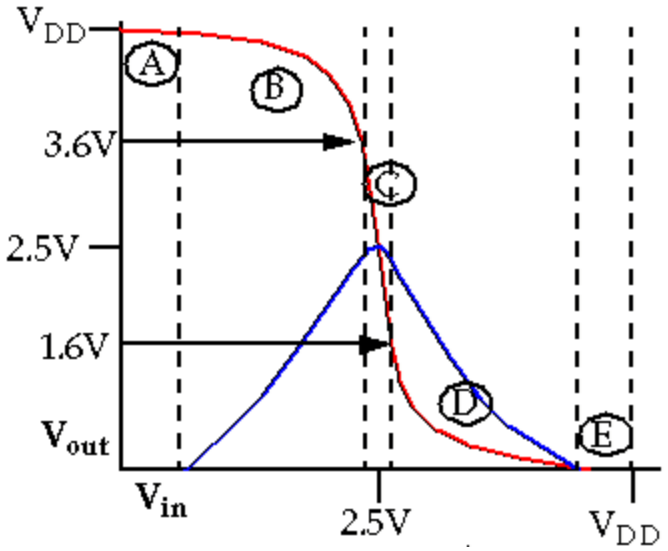




CMOS Inverter – DC Characteristics

- Region B) $V_{tn} \leq V_{in} < \frac{V_{DD}}{2}$
  - NMOS: Saturated
  - PMOS: Linear

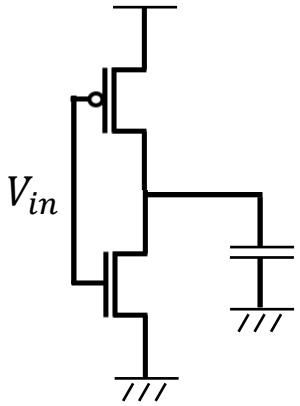


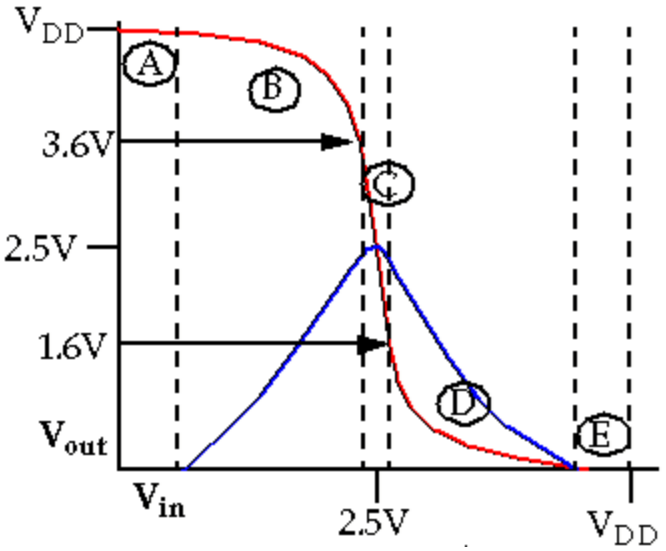


$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{tn})^2}$$

CMOS Inverter – DC Characteristics

- Region C) $V_{in} = \frac{V_{DD}}{2}$
  - NMOS: Saturated
  - PMOS: Saturated

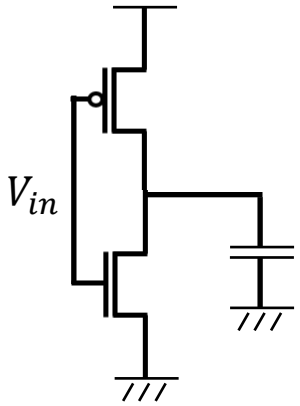


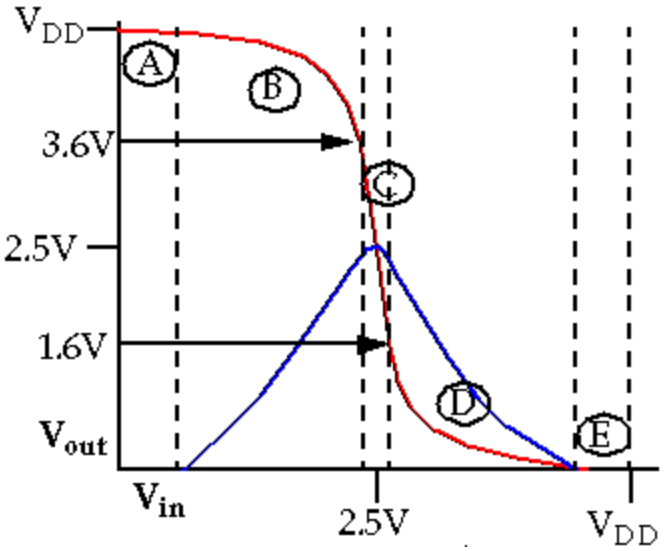


$$V_{in} - V_{tn} < V_{out} < V_{in} - V_{tp}$$

CMOS Inverter – DC Characteristics

- Region D) $\frac{V_{DD}}{2} < V_{in} \leq V_{DD} - |V_{tp}|$
  - NMOS: Linear
  - PMOS: Saturated

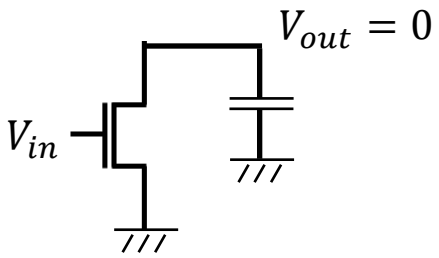


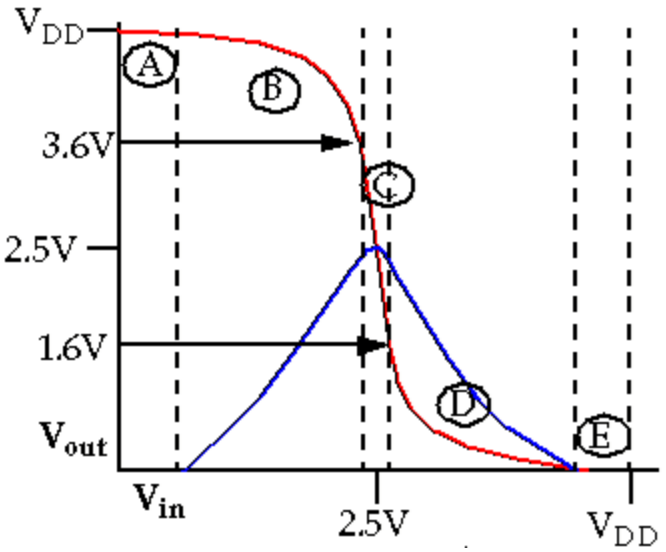


$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - V_{tp})^2}$$

CMOS Inverter – DC Characteristics

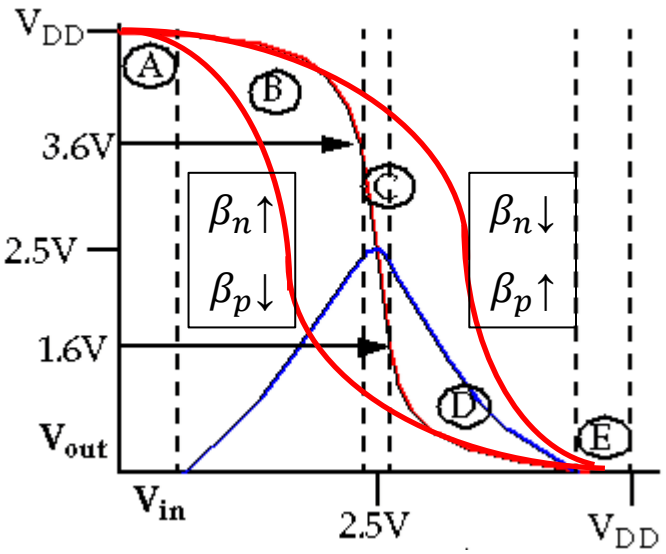
- Region E) $V_{DD} - |V_{tp}| < V_{in}$
  - NMOS: Linear
  - PMOS: Cut-off





CMOS Inverter – DC Characteristics

- β_n and β_p

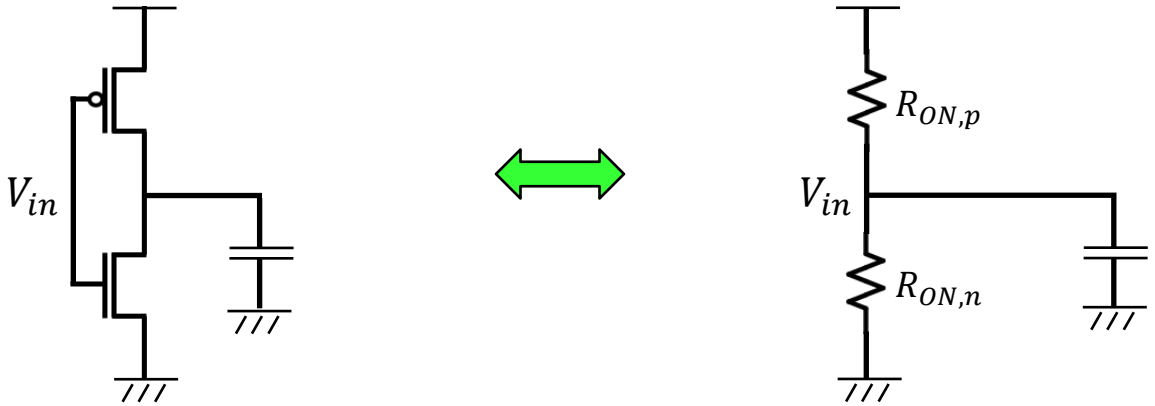


Region B) $V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{tn})^2}$

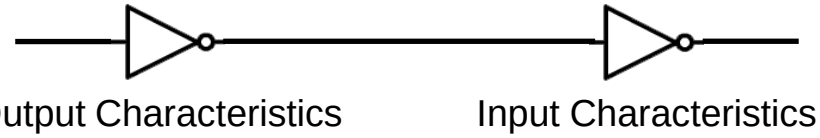
Region D) $V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - V_{tp})^2}$

CMOS Inverter – DC Characteristics

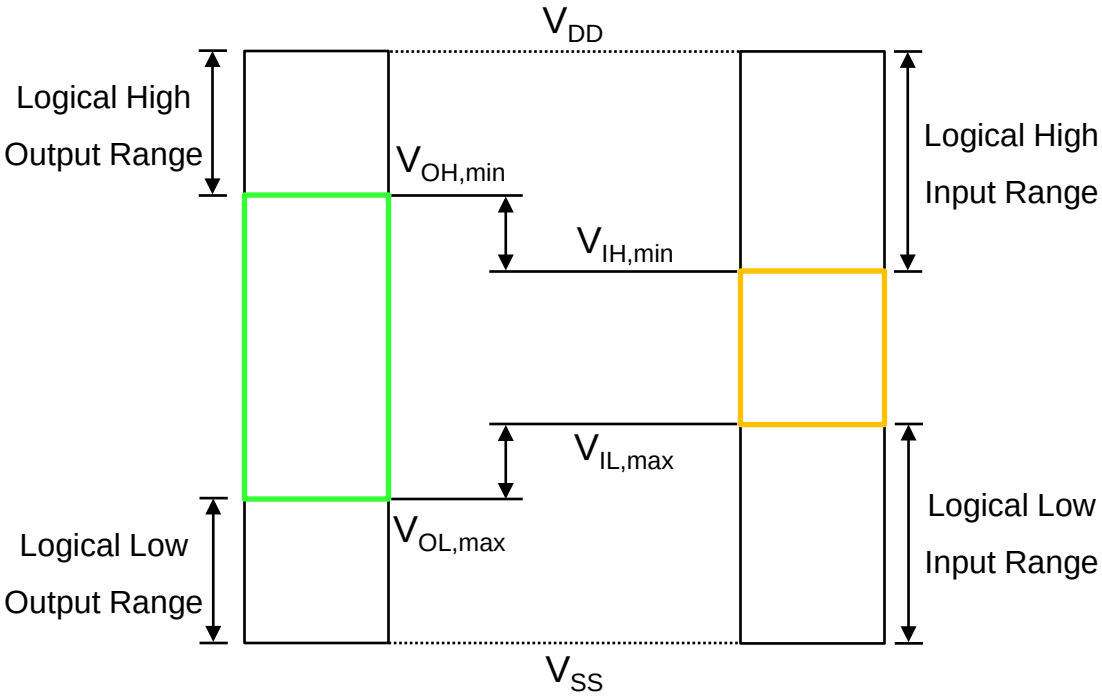
- Intuitive analysis

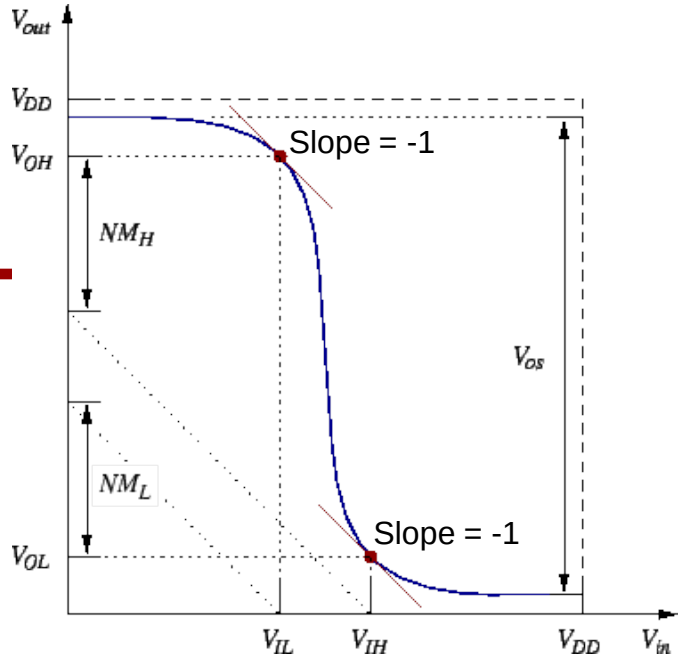


Noise Margin



Output Characteristics Input Characteristics





$V_{IH,min}$: minimum high input voltage

$V_{IL,max}$: maximum low input voltage

$V_{OH,min}$: minimum high output voltage

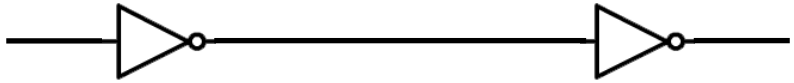
$V_{OL,max}$: maximum low output voltage

Low noise margin = $NM_L = |V_{IL,max} - V_{OL,max}|$

High noise margin = $NM_H = |V_{OH,min} - V_{IH,min}|$

Noise Margin

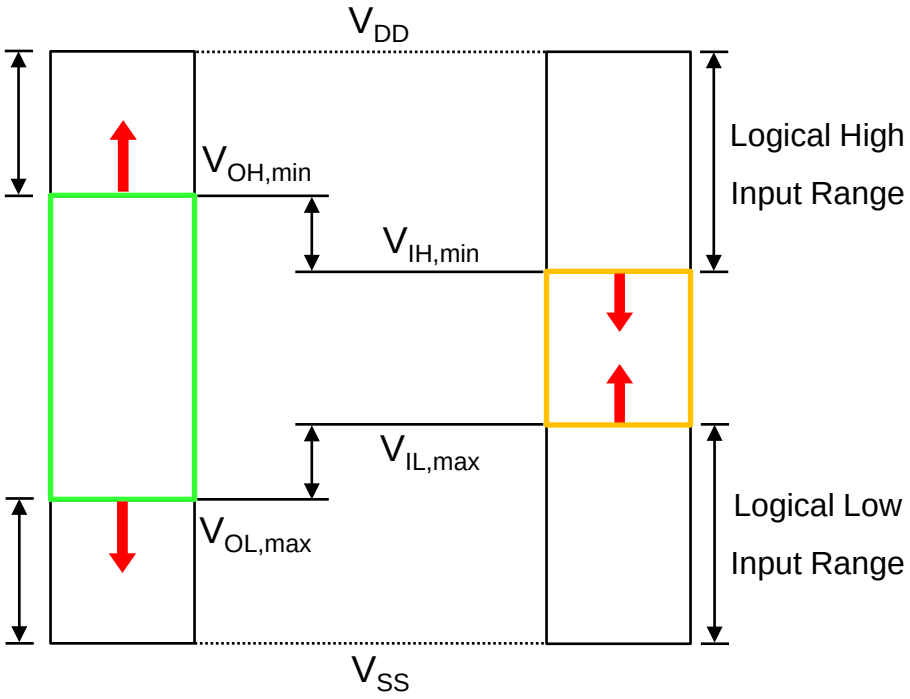
- How to increase the noise margin



Output Characteristics Input Characteristics

Low noise margin = $NM_L = |V_{IL,max} - V_{OL,max}|$

High noise margin = $NM_H = |V_{OH,min} - V_{IH,min}|$



$V_{IH,min}$: minimum high input voltage

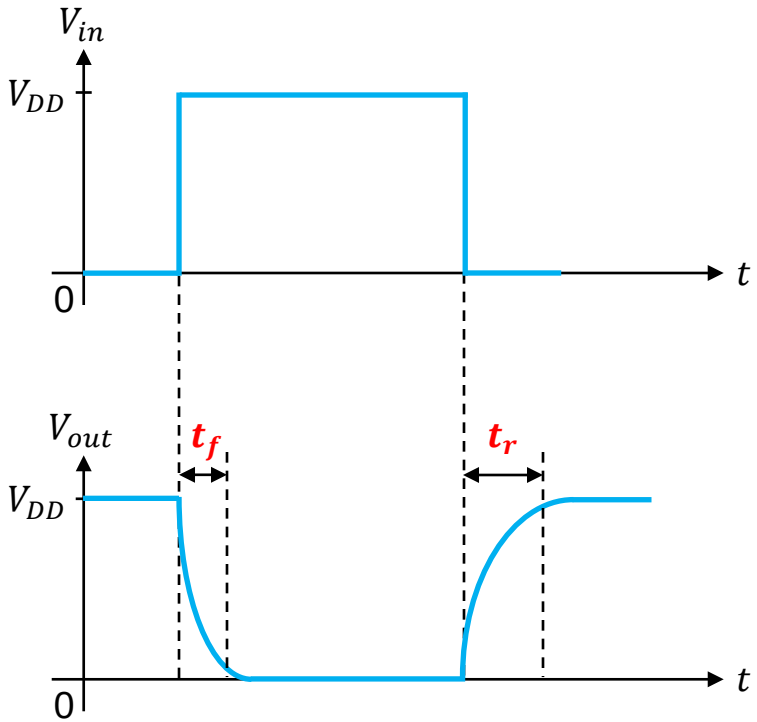
$V_{IL,max}$: maximum low input voltage

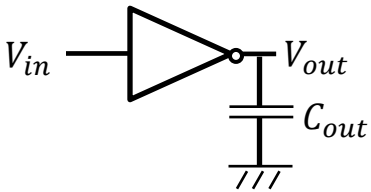
$V_{OH,min}$: minimum high output voltage

$V_{OL,max}$: maximum low output voltage

CMOS Inverter – Switching Characteristics

- Fall time & Rise time





CMOS Inverter – Switching Characteristics

- Fall time calculation
  - Natural response

$$V_{out}(t) = V_{DD}e^{-\frac{t}{R_n C_{out}}} = V_{DD}e^{-\frac{t}{\tau_n}}$$

$$t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}(t)}\right)$$

  - τ_n: NMOS time constant

- Fall time

$$t_f = t_{0.1V_{DD}} - t_{0.9V_{DD}} = \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right) = \tau_n \ln(9) \approx 2.2\tau_n$$

CMOS Inverter – Switching Characteristics

- Rise time calculation
  - Step response

$$V_{out}(t) = V_{DD}(1 - e^{-\frac{t}{R_p C_{out}}}) = V_{DD}(1 - e^{-\frac{t}{\tau_p}})$$

$$t = \tau_p \ln\left(\frac{V_{DD}}{V_{DD} - V_{out}(t)}\right)$$

  - τ_p: PMOS time constant

- Rise time

$$t_r = t_{0.9V_{DD}} - t_{0.1V_{DD}} = \tau_p \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_p \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right) = \tau_p \ln(9) \approx 2.2\tau_p$$

CMOS Inverter – Switching Characteristics

- Maximum signal frequency

$$f_{max} = \frac{1}{t_r + t_f} = \frac{1}{2.2(\tau_p + \tau_n)}$$

- Example
  - $R_p = 500\Omega$
  - $R_n = 500\Omega$
  - $C_{out} = 20fF$

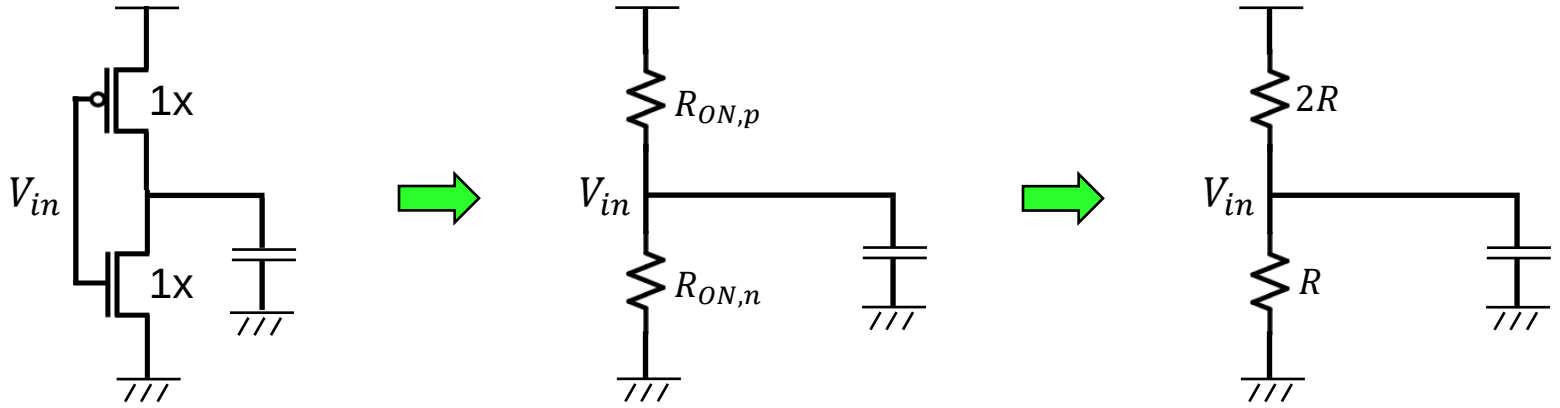
  - $\tau_p = 10ps$
  - $\tau_n = 10ps$
  - $f_{max} = 23GHz$

CMOS Inverter – Switching Characteristics

- Speed vs. area trade-off
  - $\beta_n = \mu_n c_{ox} \frac{W_n}{L_n}$
  - $\beta_p = \mu_p c_{ox} \frac{W_p}{L_p}$
  - $R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})}$
  - $R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)}$
  - $\tau_n = R_n C_{out}$
  - $\tau_p = R_p C_{out}$

Transistor Sizing

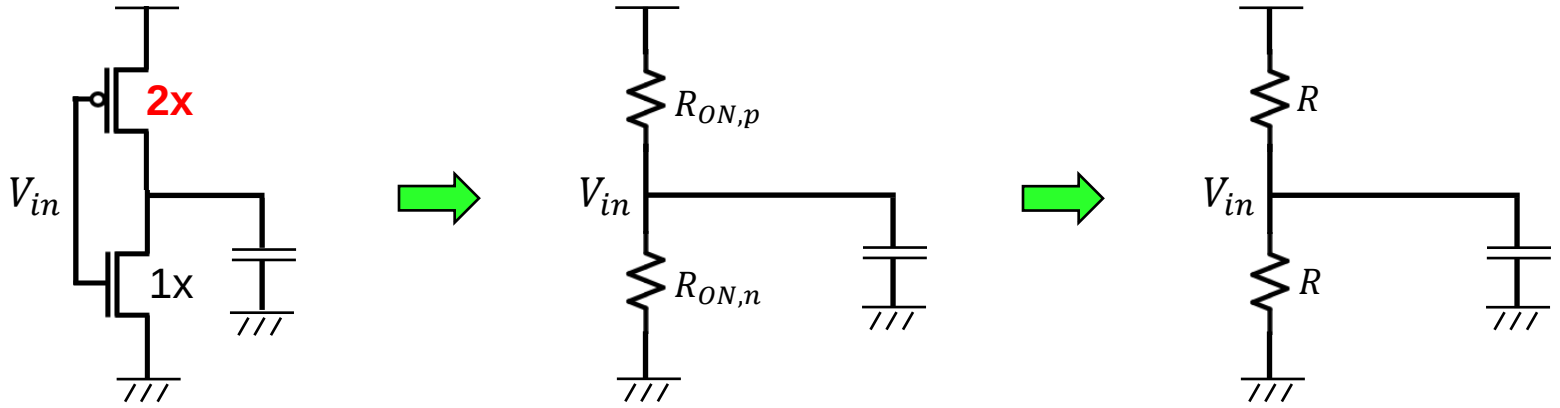
- Achieve perfectly-balanced switching characteristics in the worst case.
- Satisfy target constraints ($\tau = RC$).
- Assumption: $\mu_n = 2 \cdot \mu_p$



$$\tau_n = RC$$
$$\tau_p = 2RC$$

Transistor Sizing

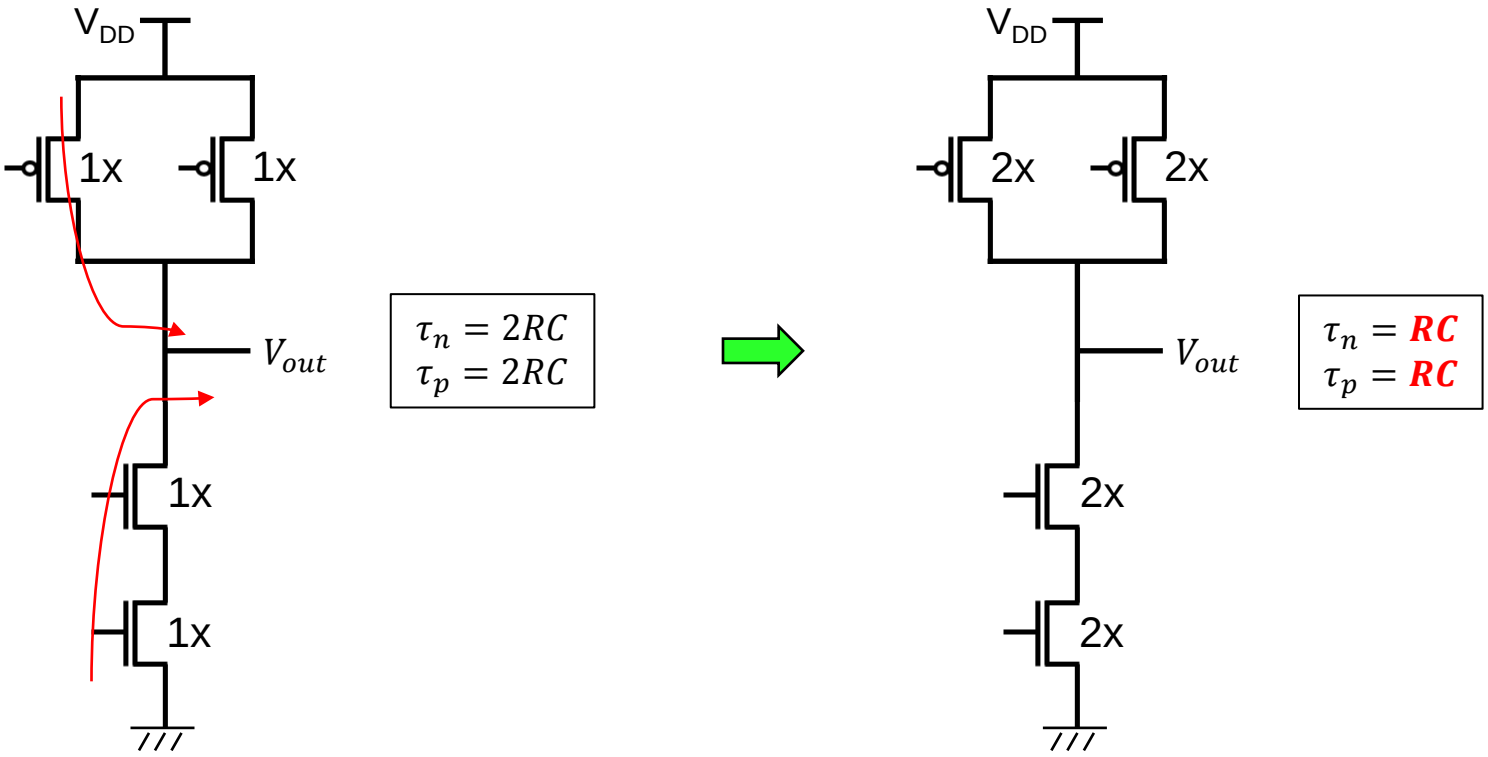
- Achieve perfectly-balanced switching characteristics in the worst case.
- Satisfy target constraints ($\tau = RC$).
- Assumption: $\mu_n = 2 \cdot \mu_p$



$$\tau_n = RC$$
$$\tau_p = \boldsymbol{RC}$$

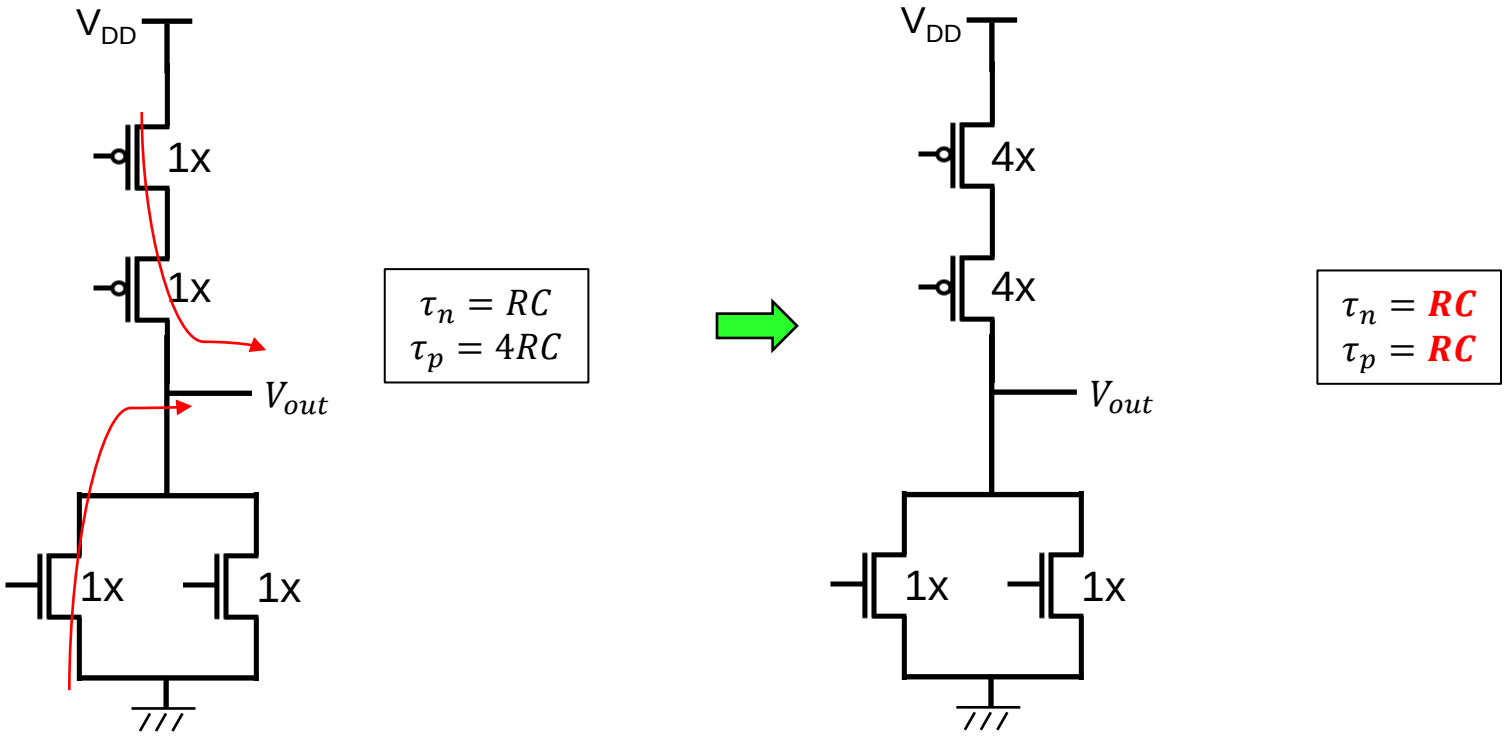
Transistor Sizing

- NAND2



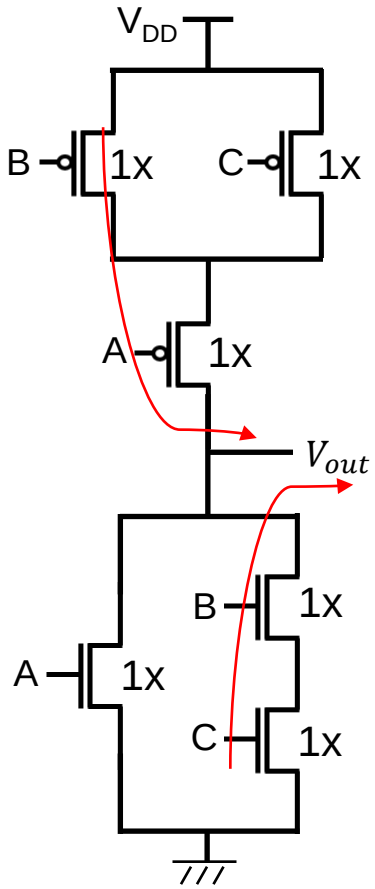
Transistor Sizing

- NOR2

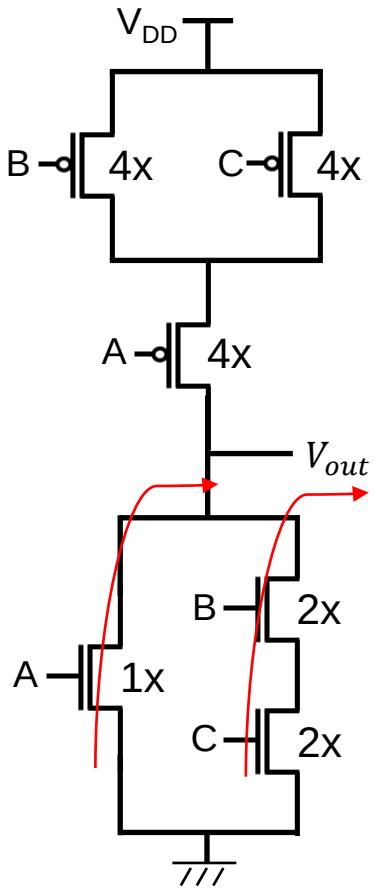


Transistor Sizing

- $F = \overline{A + B \cdot C}$



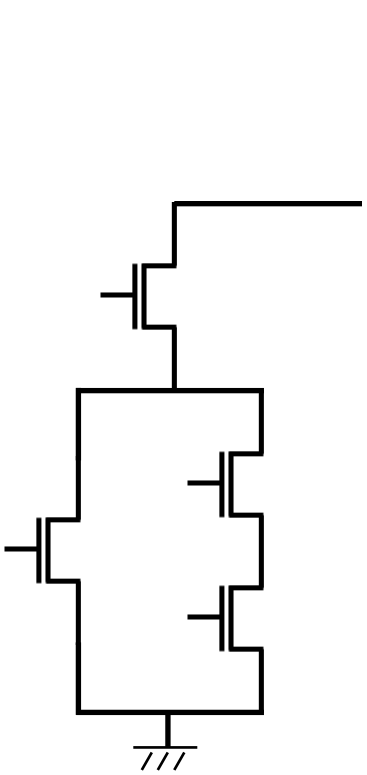
$\tau_n = 2RC$
$\tau_p = 4RC$

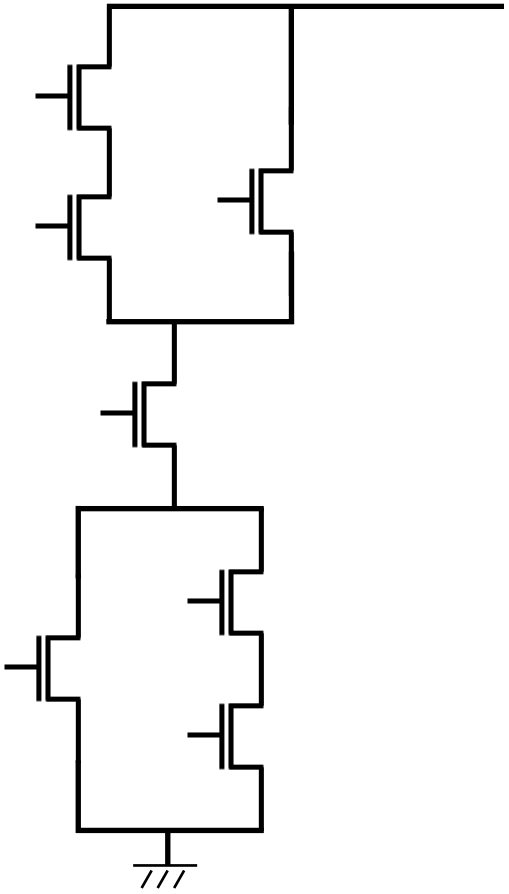


$\tau_n = \boldsymbol{RC}$
$\tau_p = \boldsymbol{RC}$

Transistor Sizing

- Examples (target: $\tau = RC$)



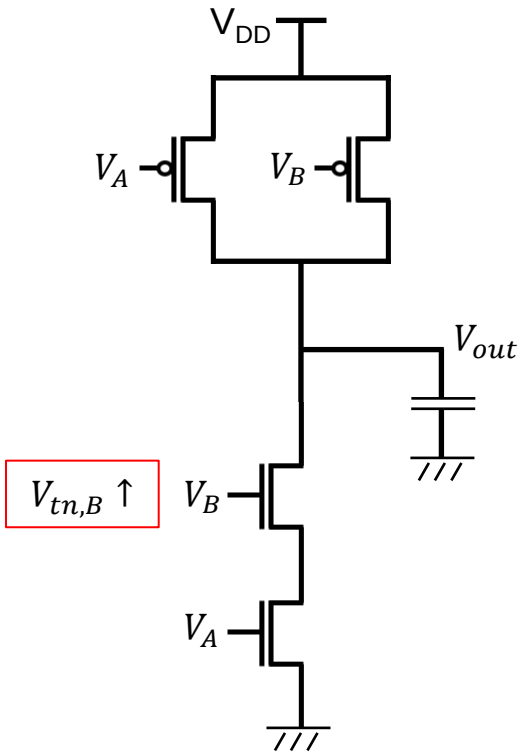


CMOS NAND/NOR – DC Characteristics

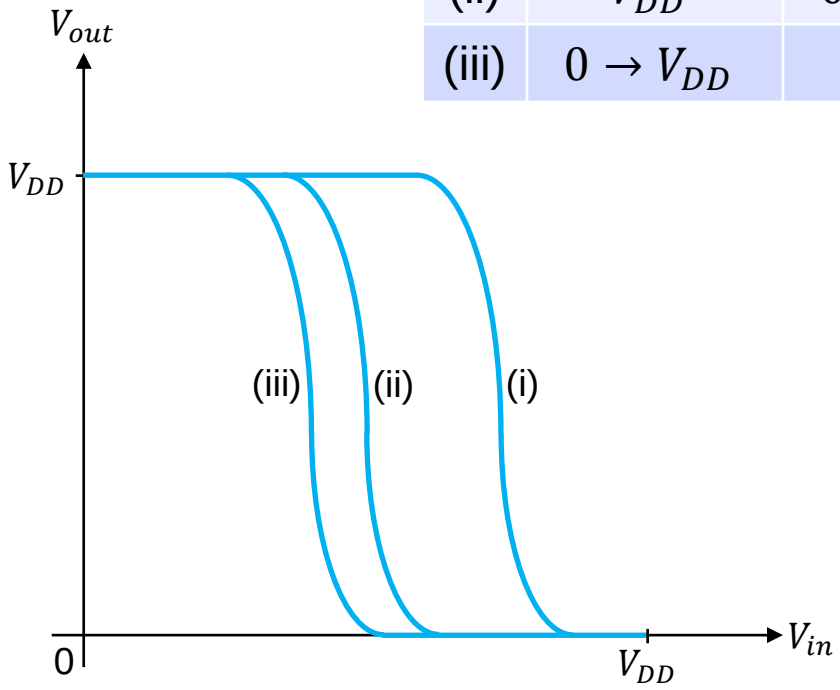
- CMOS NAND
- CMOS NOR

CMOS NAND/NOR – DC Characteristics

- CMOS NAND



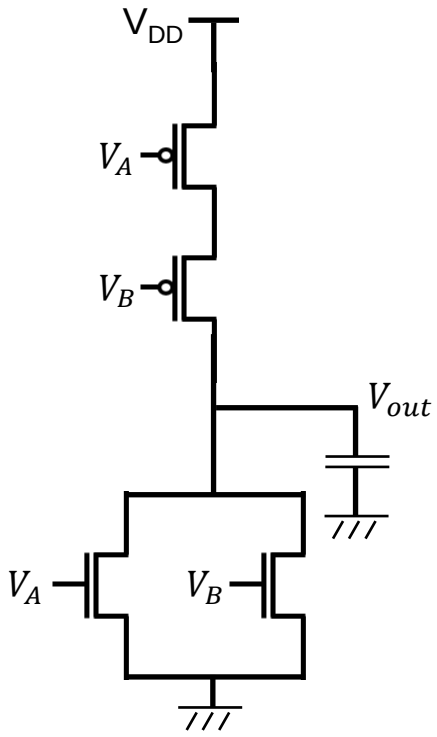
	V_A	V_B
(i)	$0 \rightarrow V_{DD}$	$0 \rightarrow V_{DD}$
(ii)	V_{DD}	$0 \rightarrow V_{DD}$
(iii)	$0 \rightarrow V_{DD}$	V_{DD}



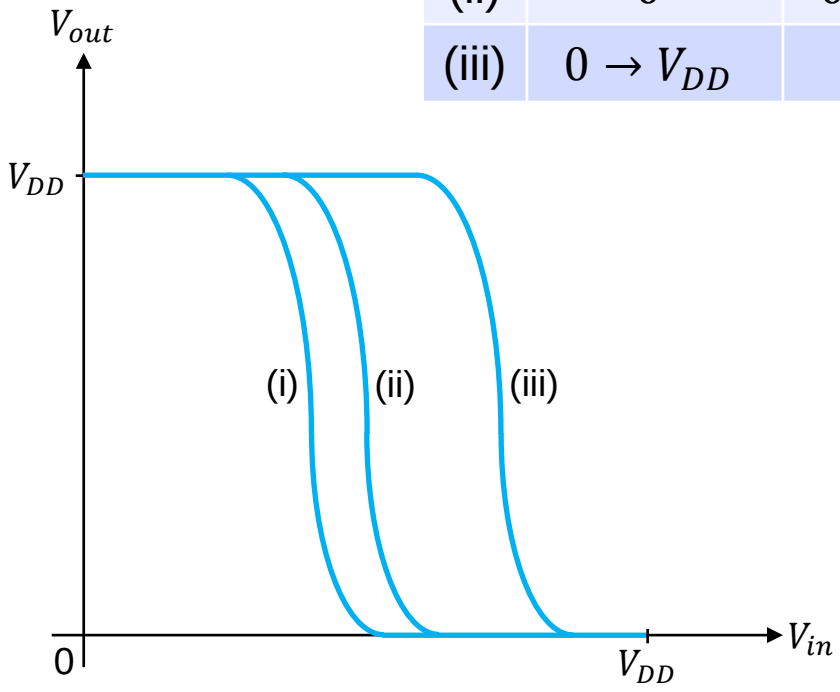
$$V_{tn} = V_{tn,0} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{2\phi_F})$$

CMOS NAND/NOR – DC Characteristics

- CMOS NOR



	V_A	V_B
(i)	$0 \rightarrow V_{DD}$	$0 \rightarrow V_{DD}$
(ii)	0	$0 \rightarrow V_{DD}$
(iii)	$0 \rightarrow V_{DD}$	0



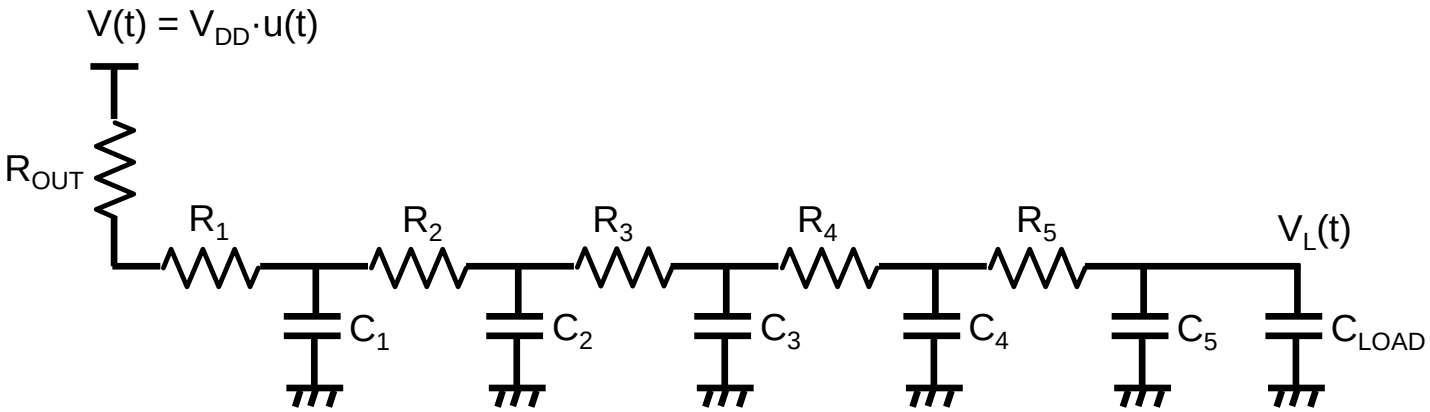
Elmore Delay

- Before we study the switching characteristics of the NAND and NOR gates, we need to know how to compute (approximate) delay of an RC tree.

- Elmore Delay
  - A very simple delay computation method.

Elmore Delay

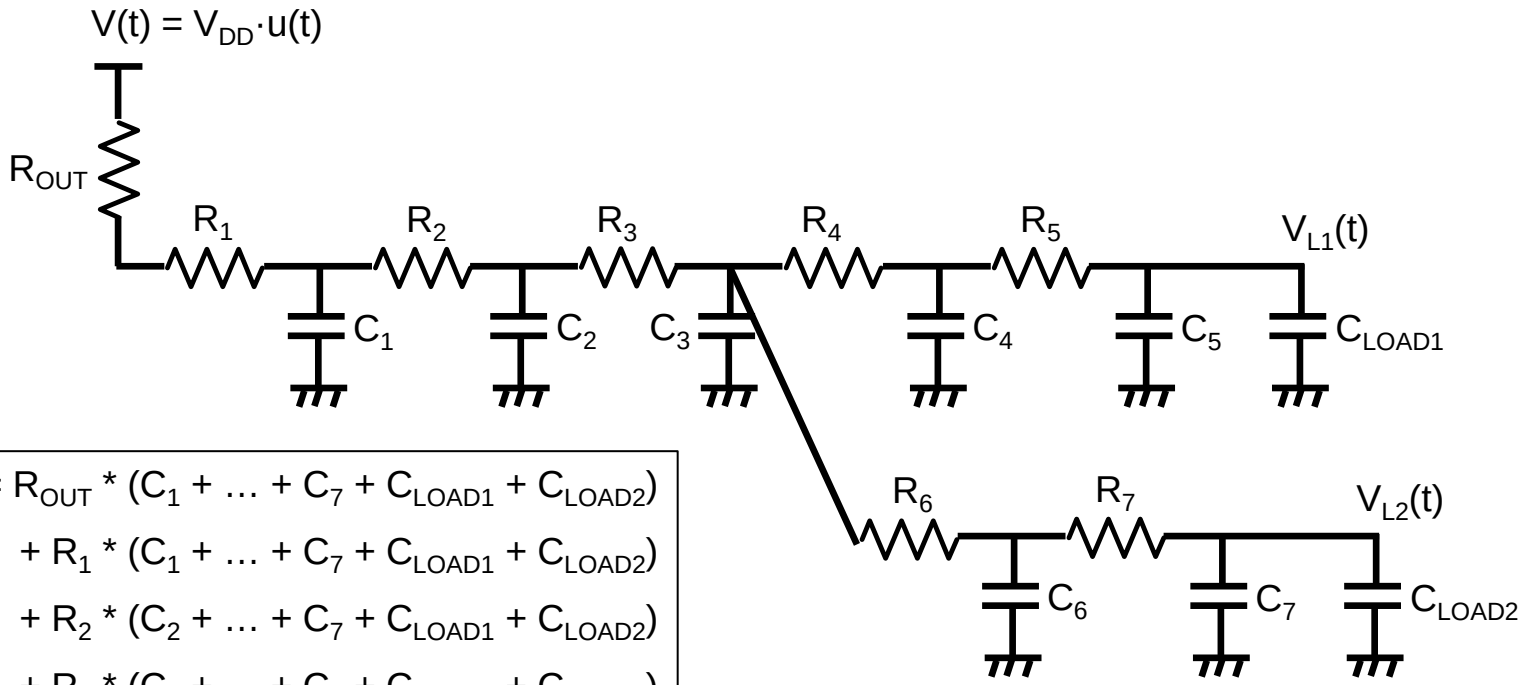
- For two-pin nets



$$\tau = R_{OUT} * (C_1 + \ldots + C_5 + C_{LOAD})$$
$$+ R_1 * (C_1 + \ldots + C_5 + C_{LOAD})$$
$$+ R_2 * (C_2 + \ldots + C_5 + C_{LOAD})$$
$$+ R_3 * (C_3 + \ldots + C_5 + C_{LOAD})$$
$$+ R_4 * (C_4 + C_5 + C_{LOAD})$$
$$+ R_5 * (C_5 + C_{LOAD})$$

Elmore Delay

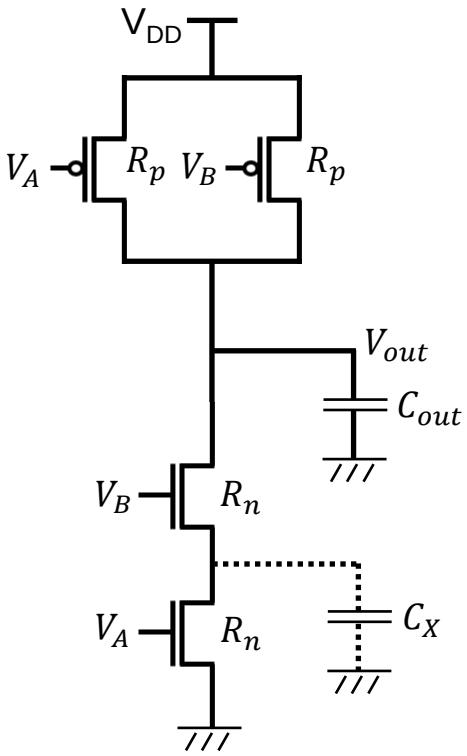
- For multi-pin nets



$$\tau_1 = R_{OUT} * (C_1 + \ldots + C_7 + C_{LOAD1} + C_{LOAD2})$$
$$+ R_1 * (C_1 + \ldots + C_7 + C_{LOAD1} + C_{LOAD2})$$
$$+ R_2 * (C_2 + \ldots + C_7 + C_{LOAD1} + C_{LOAD2})$$
$$+ R_3 * (C_3 + \ldots + C_7 + C_{LOAD1} + C_{LOAD2})$$
$$+ R_4 * (C_4 + C_5 + C_{LOAD1})$$
$$+ R_5 * (C_5 + C_{LOAD1})$$

CMOS NAND/NOR – Switching Characteristics

- CMOS NAND



Worst-case rise time: $t_r \approx 2.2\tau_p = 2.2(R_p(C_{out} + C_X))$

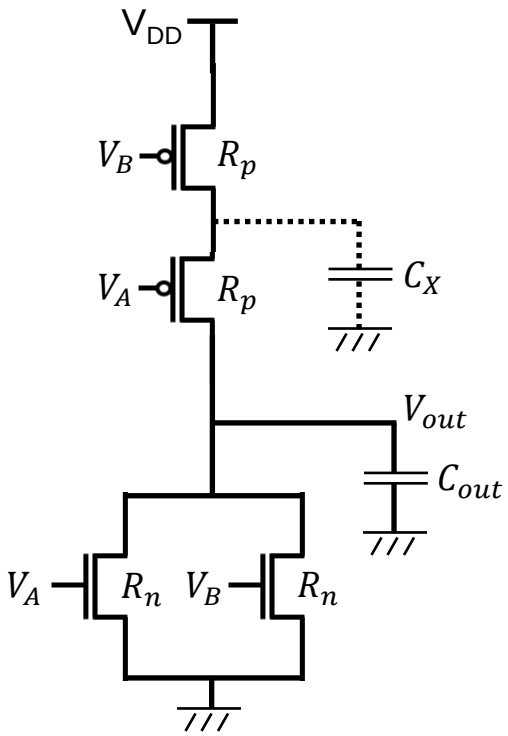
Best-case rise time: $t_r \approx 2.2\tau_p = 2.2(\frac{R_p}{2})C_{out}$

Worst-case fall time: $t_f \approx 2.2\tau_n = 2.2[(2R_n)C_{out} + R_nC_X]$

Best-case fall time: $t_f \approx 2.2\tau_n = 2.2(2R_n)C_{out}$

CMOS NAND/NOR – Switching Characteristics

- CMOS NOR



Worst-case rise time: $t_r \approx 2.2\tau_p = 2.2[R_p(C_X + C_{out}) + R_p C_{out}]$

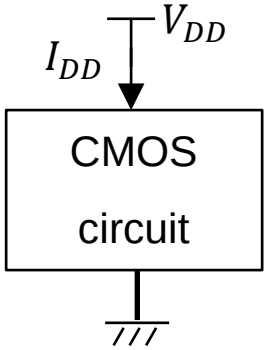
Best-case rise time: $t_r \approx 2.2\tau_p = 2.2(2R_p)C_{out}$

Worst-case fall time: $t_f \approx 2.2\tau_n = 2.2[R_n C_{out} + (R_n + R_p)C_X]$

Best-case fall time: $t_f \approx 2.2\tau_n = 2.2(\frac{R_n}{2})C_{out}$

CMOS Inverter – Power Dissipation

- $P = V_{DD} I_{DD}$
  $= P_{DC} + P_{dyn}$
  - $P_{DC} = V_{DD} I_{DDQ}$
    - I_{DDQ}: Quiescent leakage current
  - $P_{dyn} = \alpha \cdot f \cdot C_{out} {V_{DD}}^2$

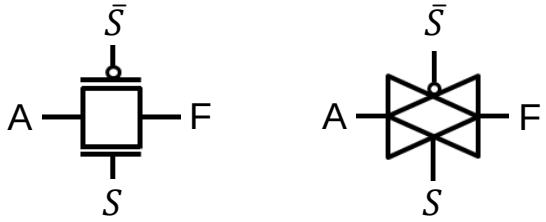


More CMOS Gates

- Combinational logic
- Transmission gates
- Multiplexors
- Tristate gates
- Sequential gates
  - Latches
  - Flip Flops

Transmission Gate

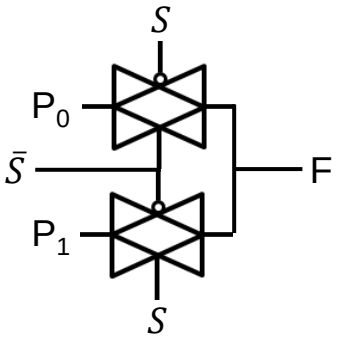
- Transmission gate



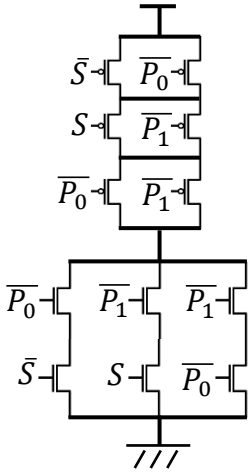
S \ A	0	1
0	Z	Z
1	0 (V_{SS}+δ)	1 (V_{DD}-δ)

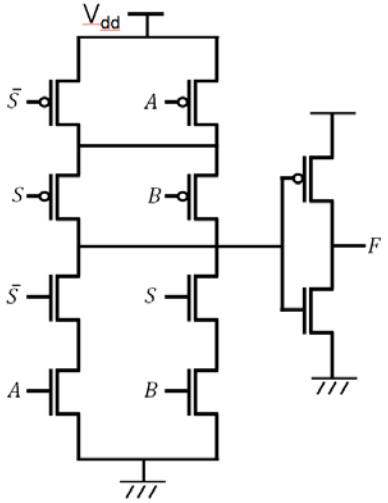
Multiplexor

- Multiplexor $F = \bar{S} \cdot P_0 + S \cdot P_1$ $F = \overline{\overline{\bar{S} \cdot P_0 + S \cdot P_1}} = \overline{(\bar{S} \cdot \overline{P_0} + S \cdot \overline{P_1} + \overline{P_0} \cdot \overline{P_1})}$



S	F
0	P_0
1	P_1

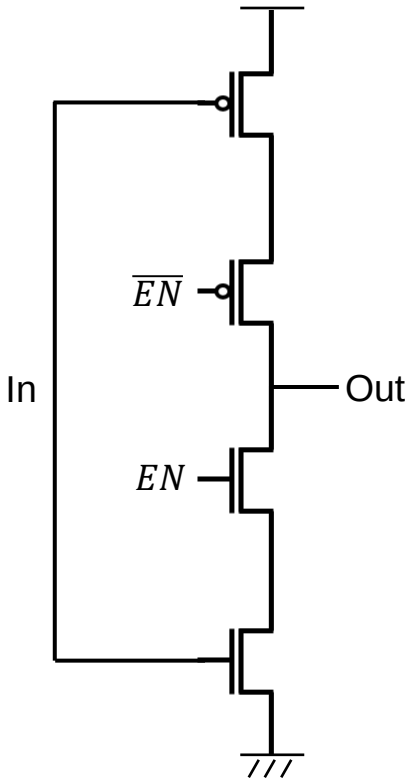




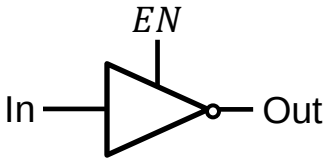
4 transistors vs. 12 (or 10) transistors

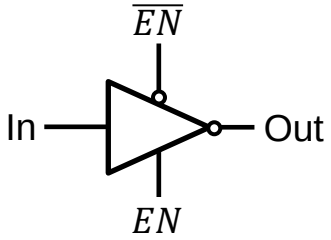
Tristate gate

- Tristate inverter



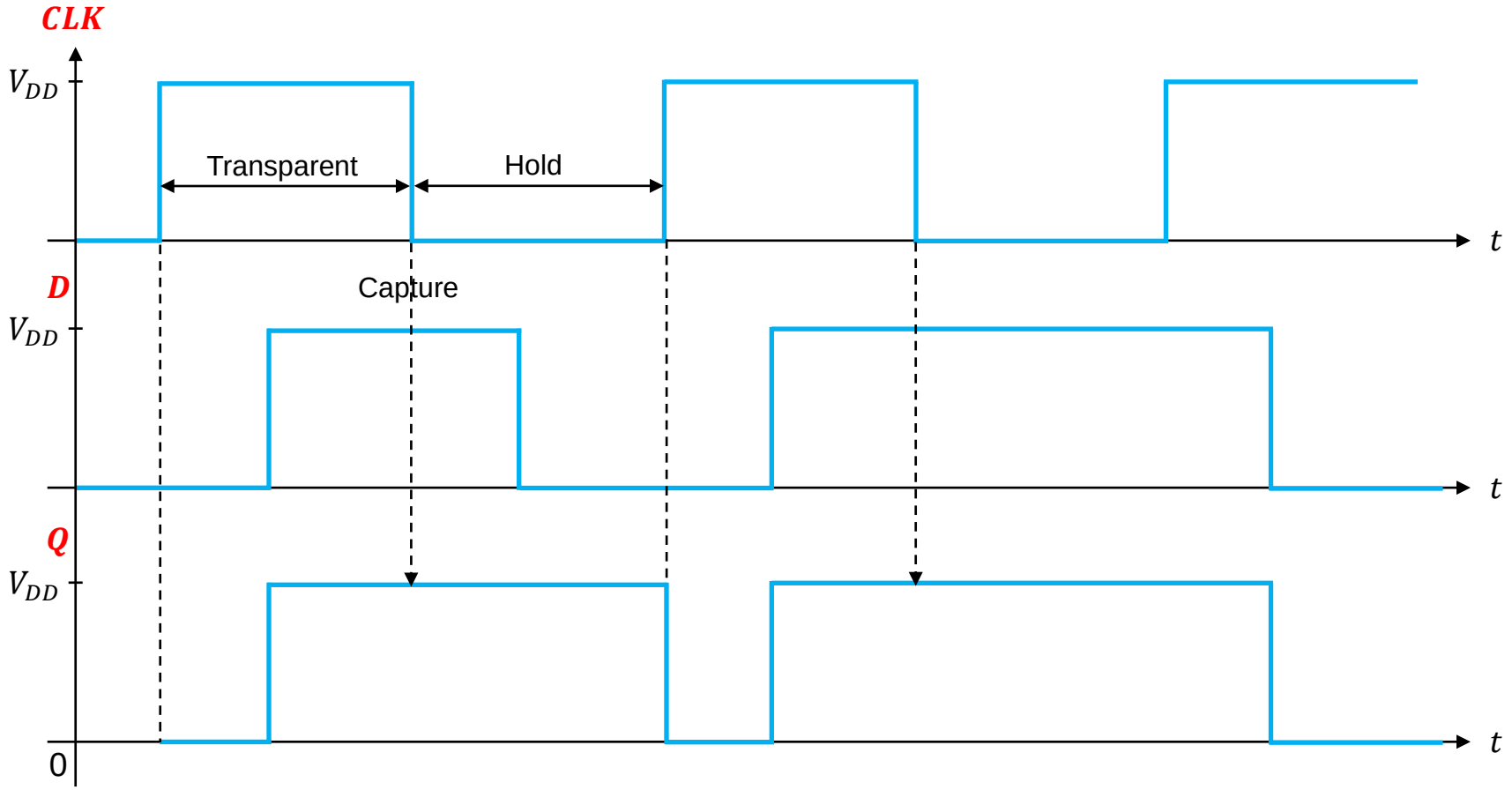
EN	Out
0	Z
1	$\overline{in}$





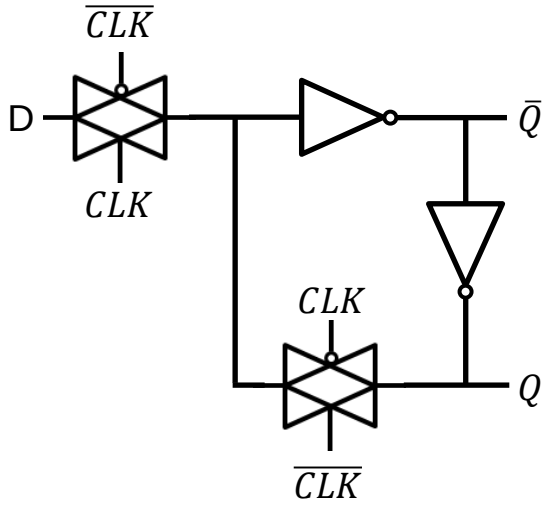
Static CMOS Sequential Gates

- D-latch



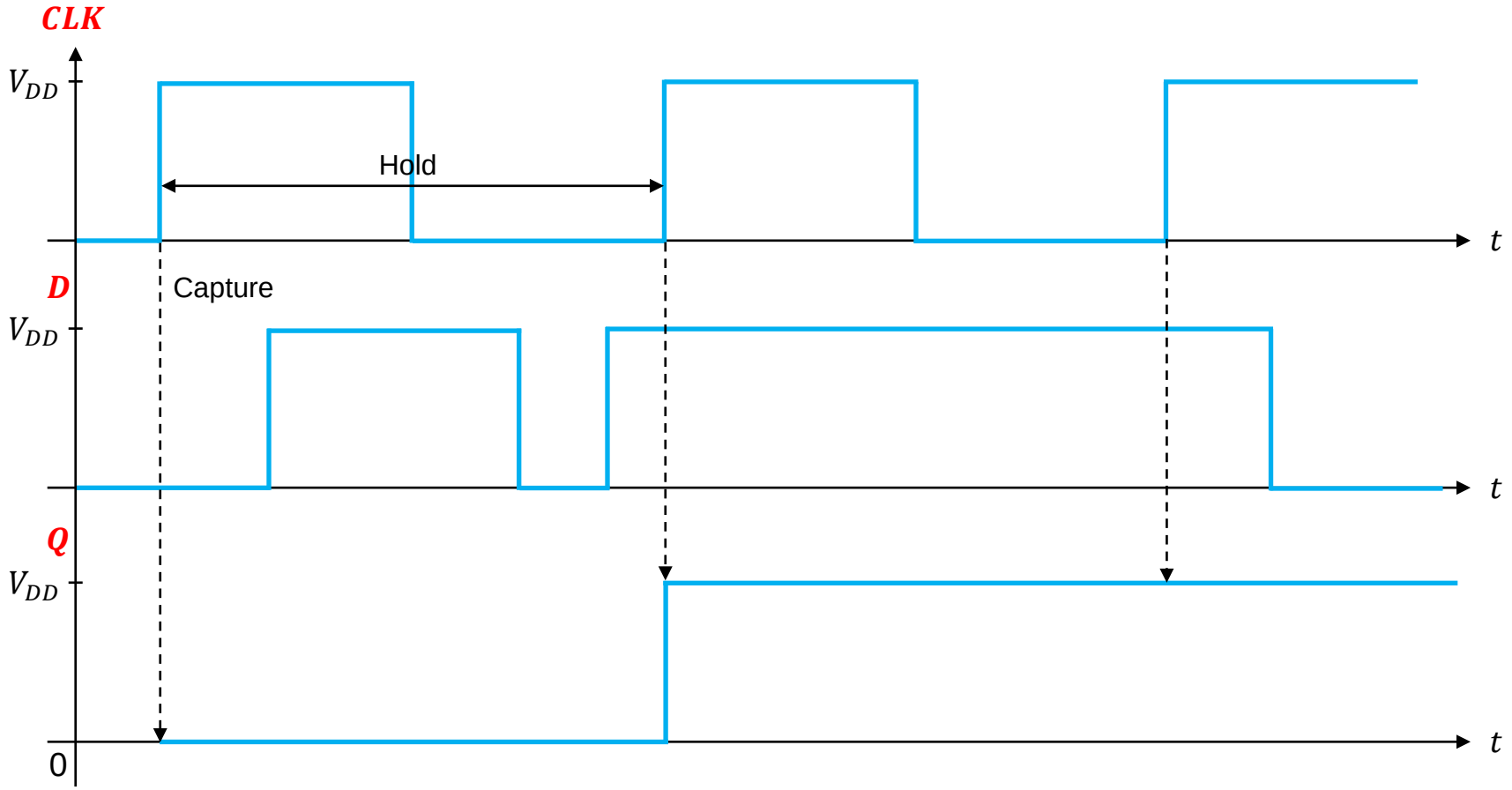
Static CMOS Sequential Gates

- D-latch



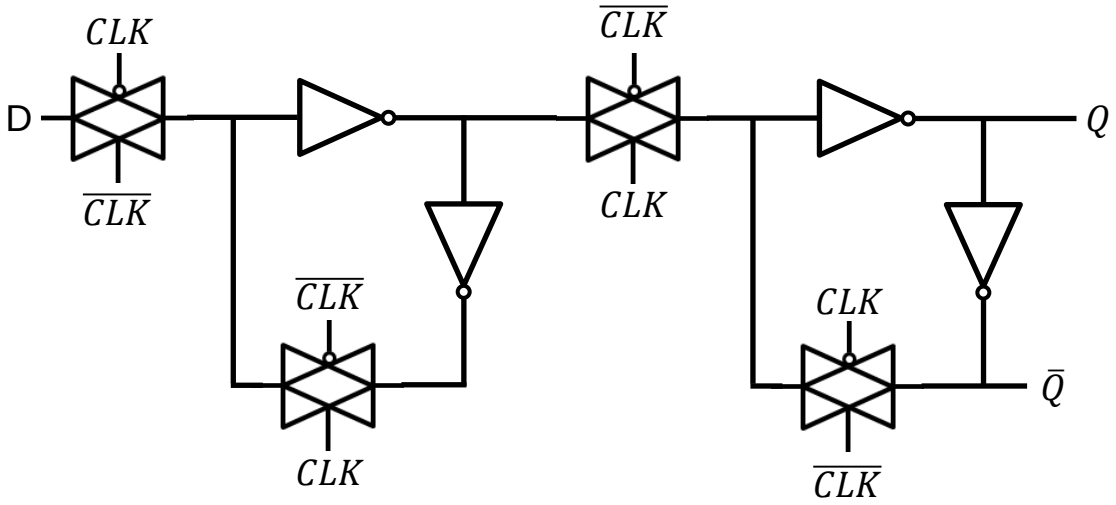
Static CMOS Sequential Gates

- Positive Edge-Triggered D Flip-Flop



Static CMOS Sequential Gates

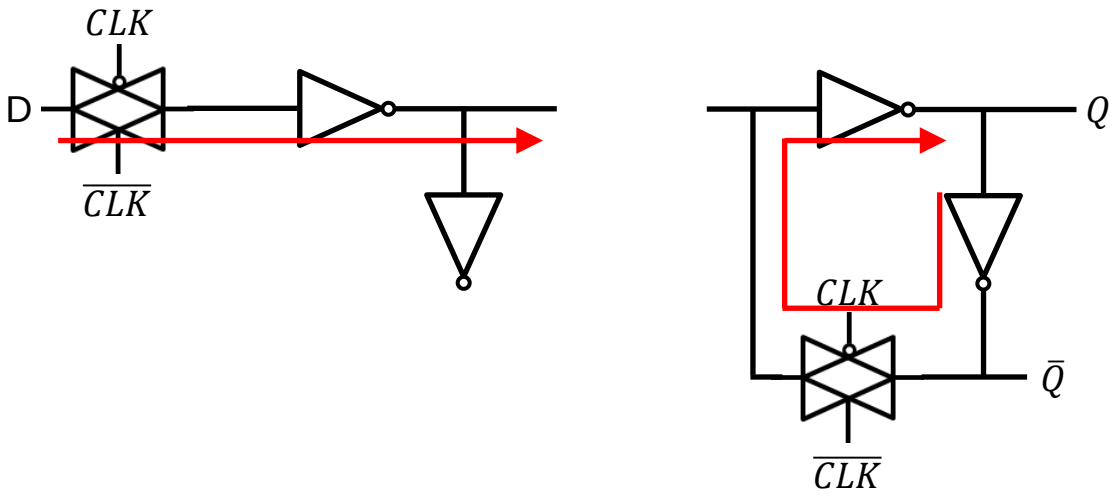
- Positive Edge-Triggered D Flip-Flop



Static CMOS Sequential Gates

- Positive Edge-Triggered D Flip-Flop

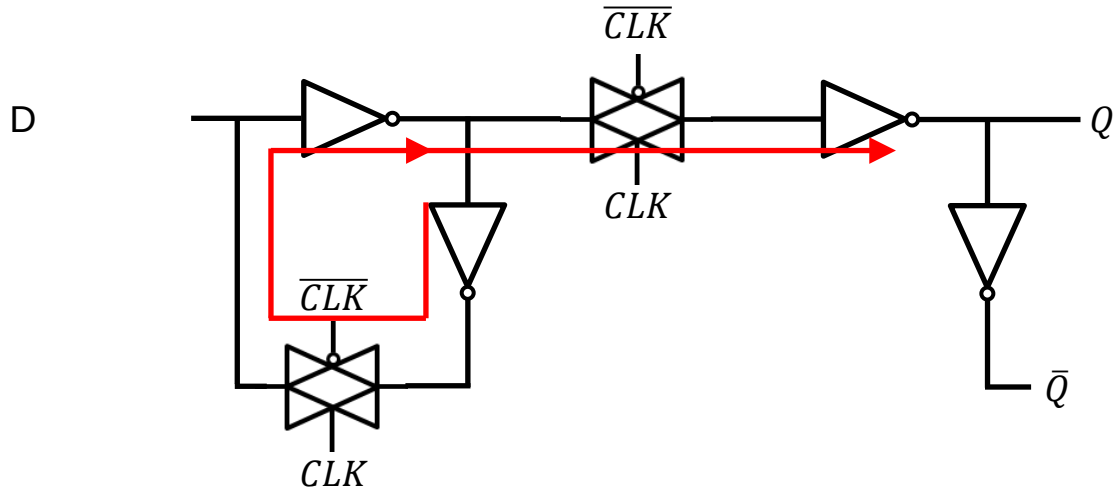
$\boldsymbol{CLK = 0}$



Static CMOS Sequential Gates

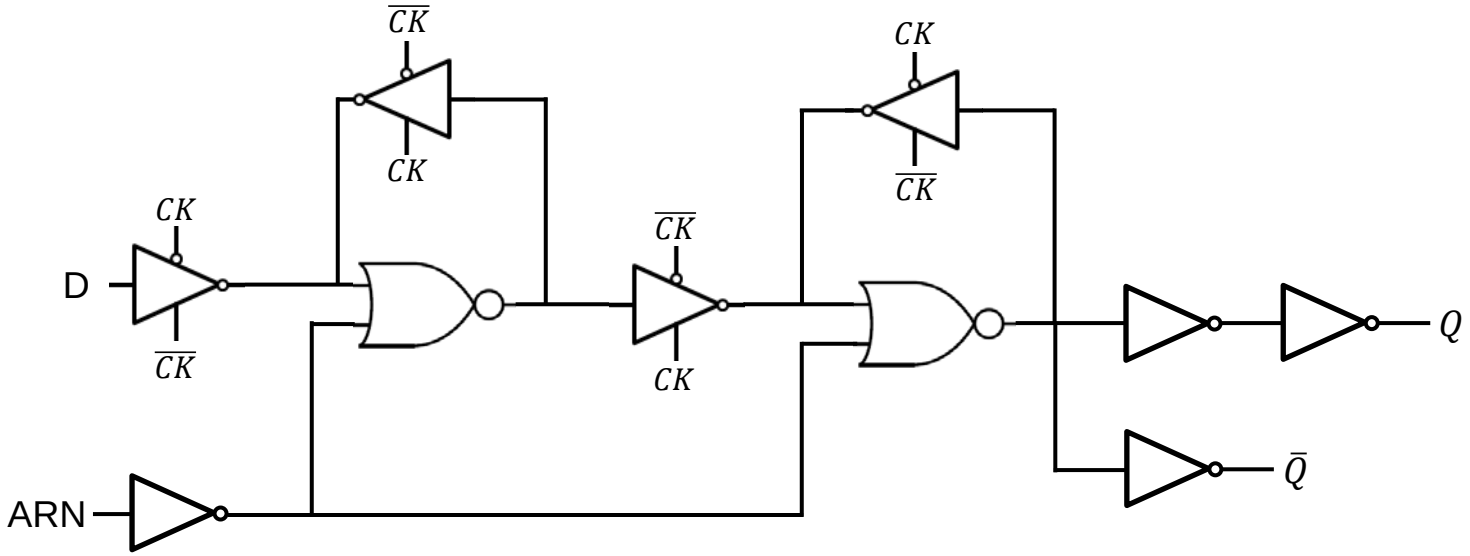
- Positive Edge-Triggered D Flip-Flop

$\boldsymbol{CLK = 1}$



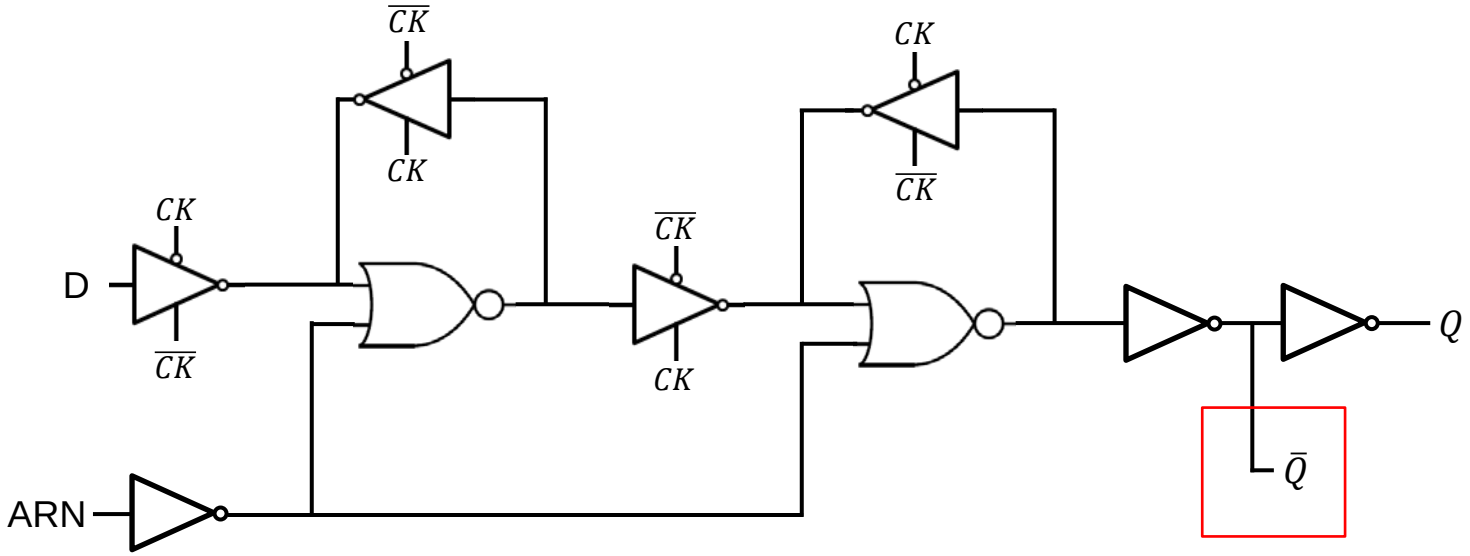
Static CMOS Sequential Gates

- Positive Edge-Triggered D Flip-Flop with ??



Static CMOS Sequential Gates

- Why not?



CMOS Properties

- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratio less
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors
- N fan-in gates need 2N transistors