EE434
ASIC & Digital Systems

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Lecture 4

More on CMOS Gates

Ref: Textbook chapter 2

Some of the slides are adopted from Digital Integrated Circuits by Jan M Rabaey

CMOS Properties

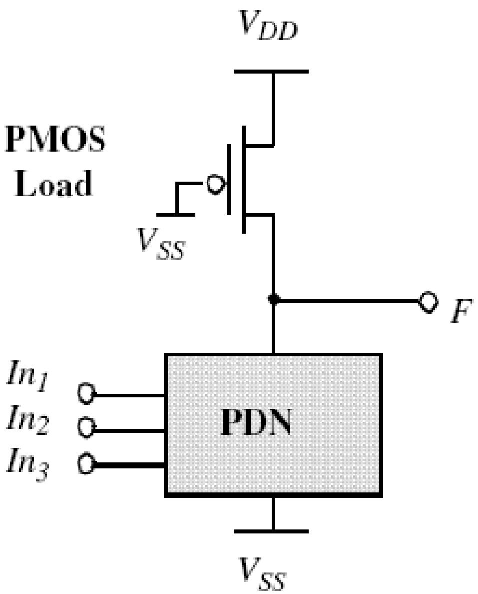
- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratio less
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors
- N fan-in gates need 2N transistors

Special CMOS Design Styles

- Ratioed Logic (Pseudo-nMOS)
- Dynamic CMOS
- Domino Logic
- Multiple-Output Domino Logic
- Dual-Rail Logic
- Pass Transistor Logic
- Transmissions Gate Logic

Ratioed Logic

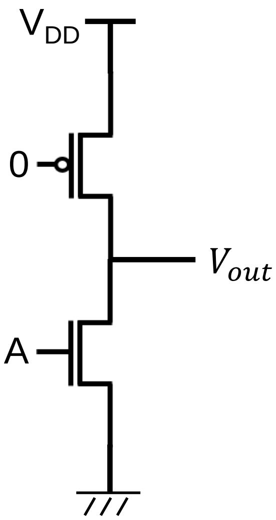
- Pseudo NMOS
  - Smaller area and load, but static power dissipation
  - Follow board notes



pseudo-NMOS

Pseudo-nMOS

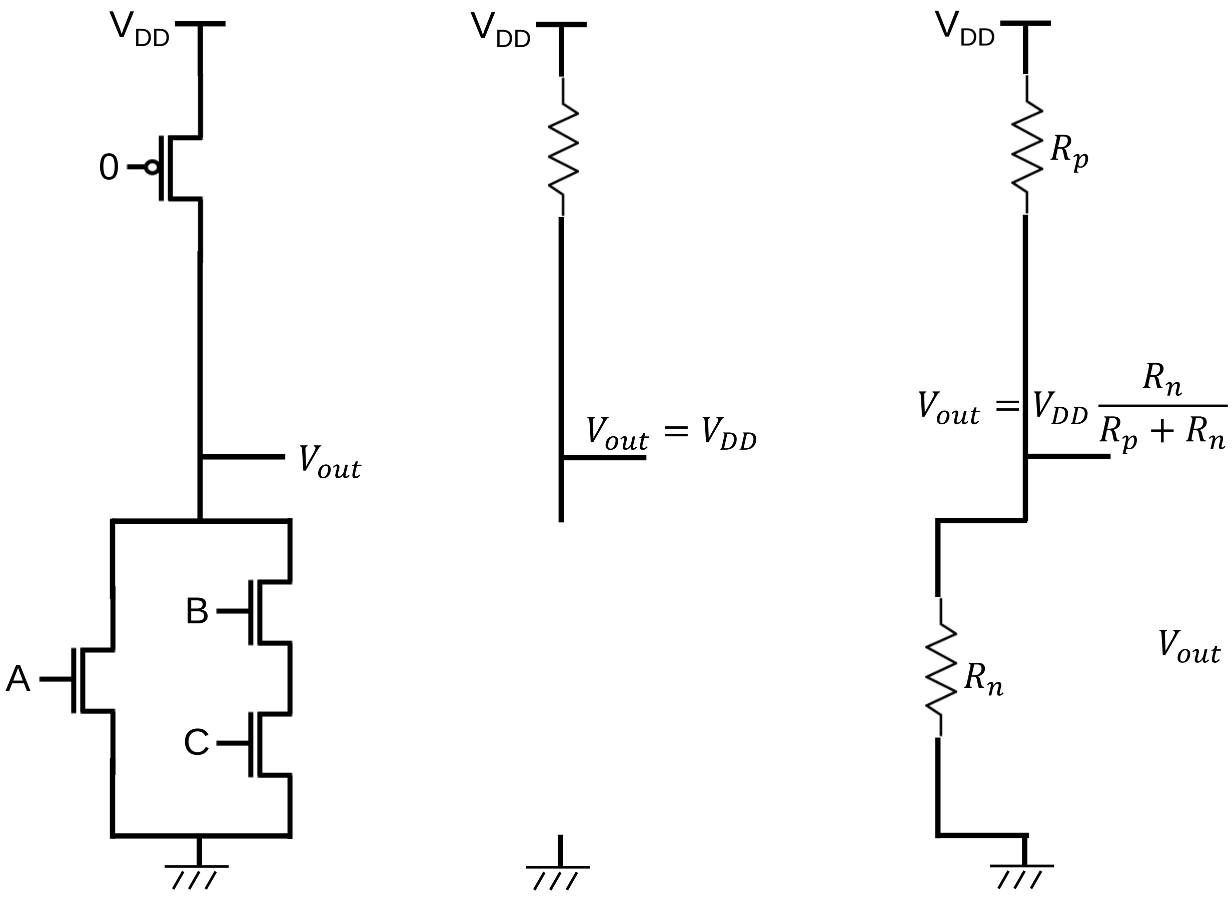
- More accurate computation
  - PMOS: Saturation
  - NMOS: Linear



$$\frac{\beta_n}{2}\left[2(V_{DD} - V_{tn})V_{OL} - {V_{OL}}^2\right] = \frac{\beta_p}{2}(V_{DD} - |V_{tp}|)^2$$

$$V_{OL} = (V_{DD} - V_{tn}) - \sqrt{(V_{DD} - V_{tn})^2 - \frac{\beta_p}{\beta_n}(V_{DD} - |V_{tp}|)^2}$$

Pseudo-nMOS



$$V_{out} = 0.1V_{DD} = V_{DD} \cdot \frac{R_n}{R_p + R_n}$$

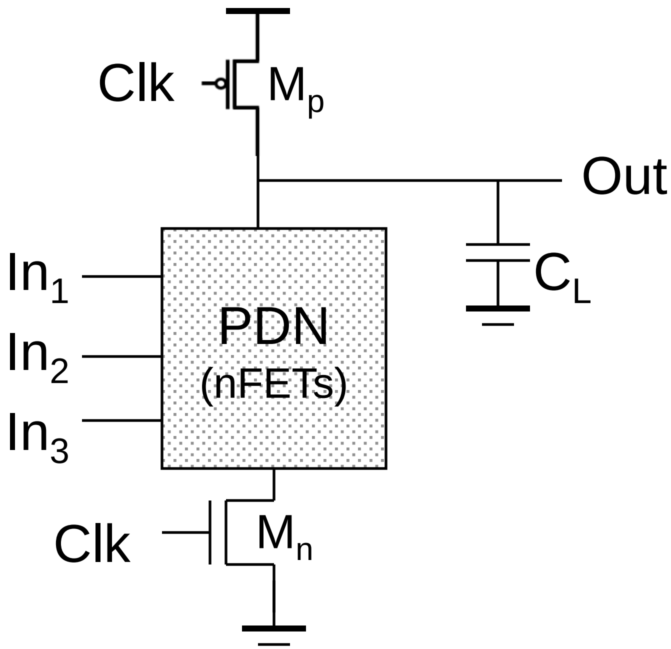
$$R_p = 9R_n$$

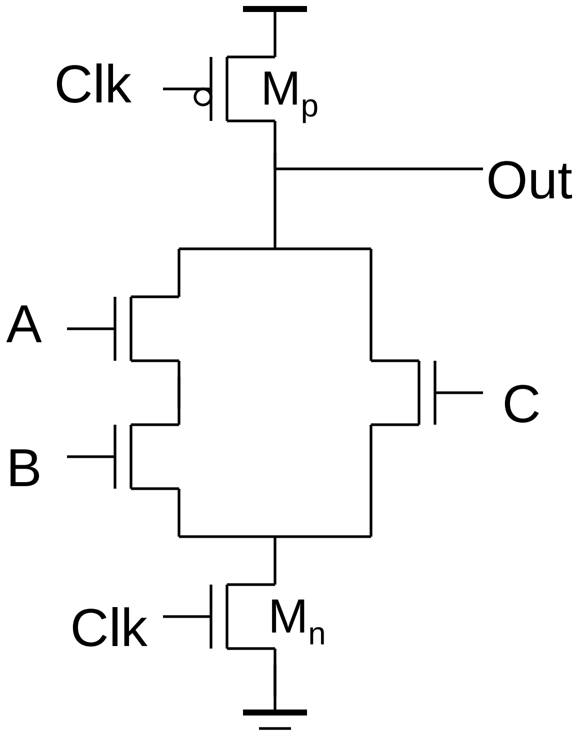
Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of n requires $2n$ (n N-type + n P-type) devices

- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on $n + 2$ (n+1 N-type + 1 P-type) transistors

Dynamic CMOS





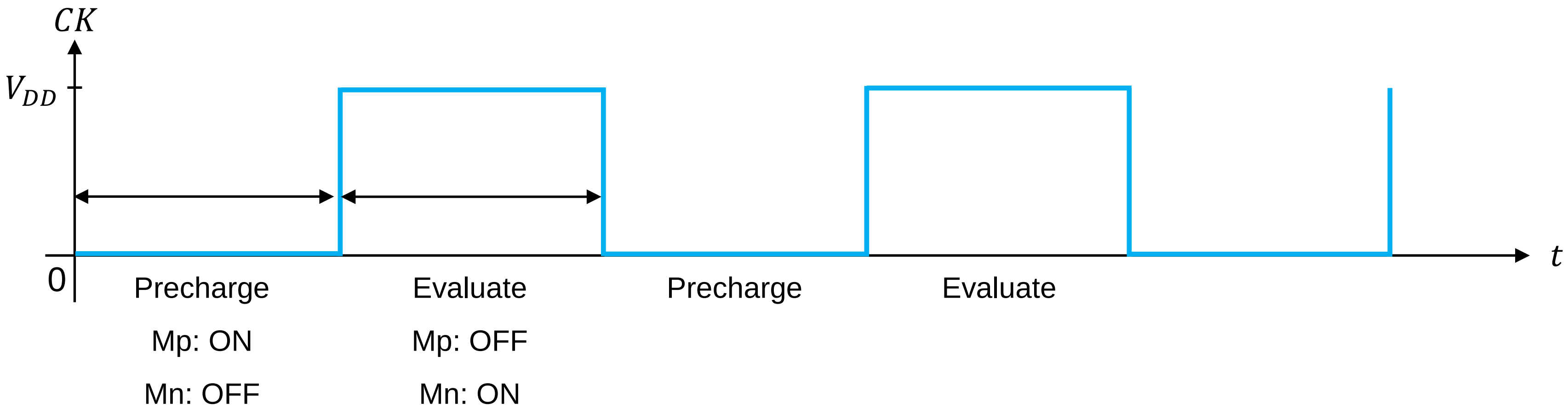
Two phase operation

Precharge (CLK = 0)

Evaluate (CLK = 1)

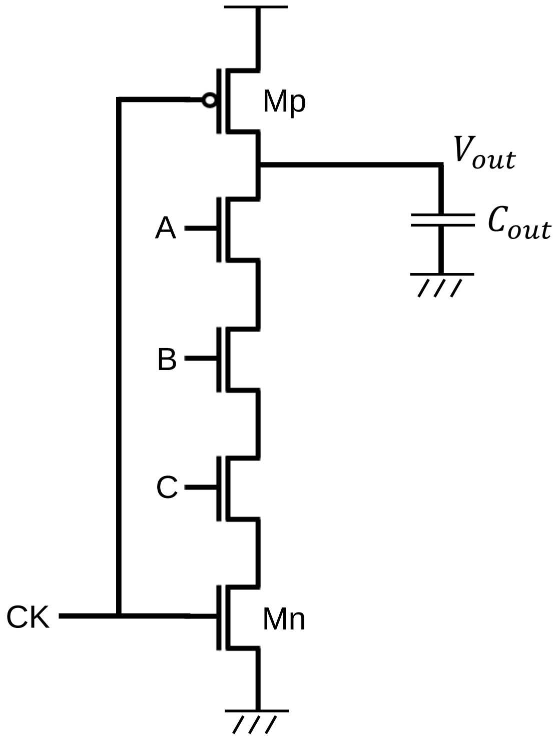
Dynamic CMOS

- Operation



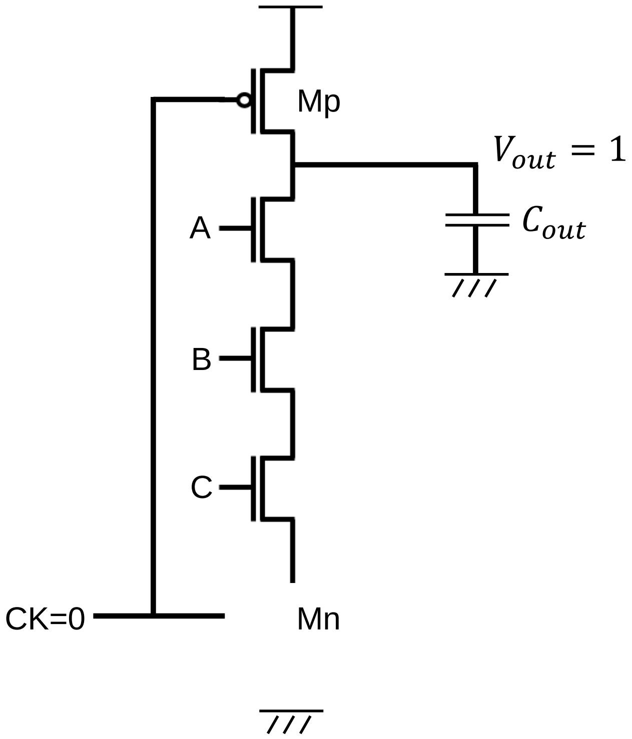
Dynamic CMOS

- $F = \overline{A \cdot B \cdot C}$



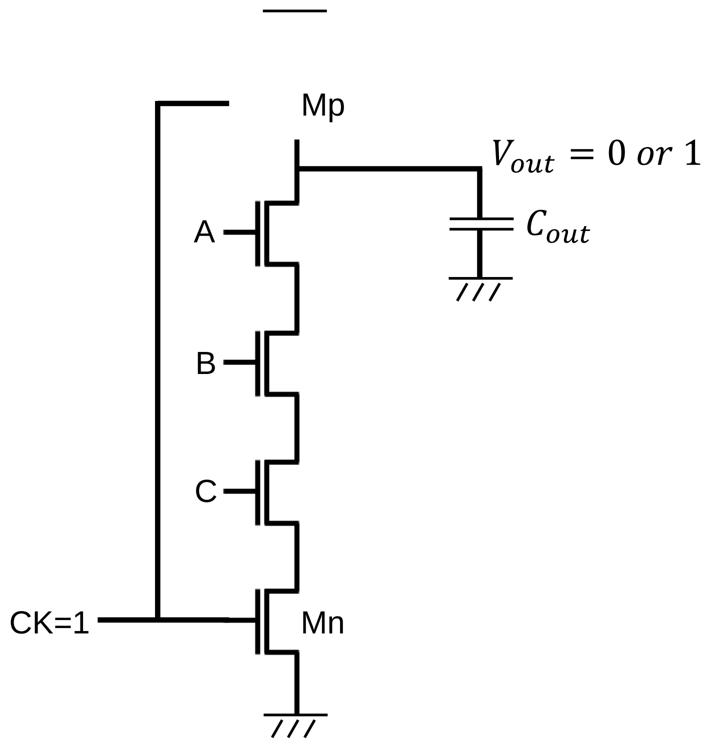
Dynamic CMOS

- Precharge



Dynamic CMOS

- Evaluation



Properties of Dynamic CMOS

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static CMOS gates)
- Full swing outputs
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (Cout)

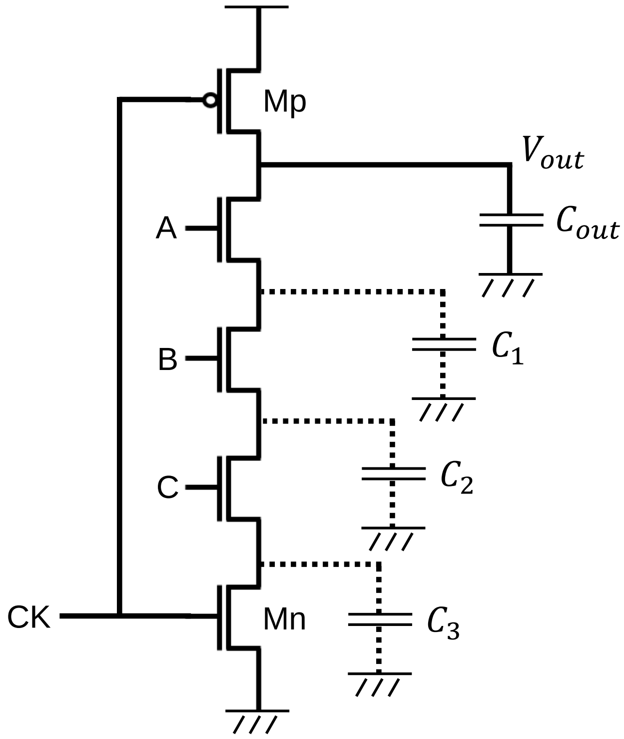
Properties of Dynamic CMOS

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND
  - no glitching
  - higher transition probabilities
  - extra load on Clk

- Needs a precharge/evaluate clock

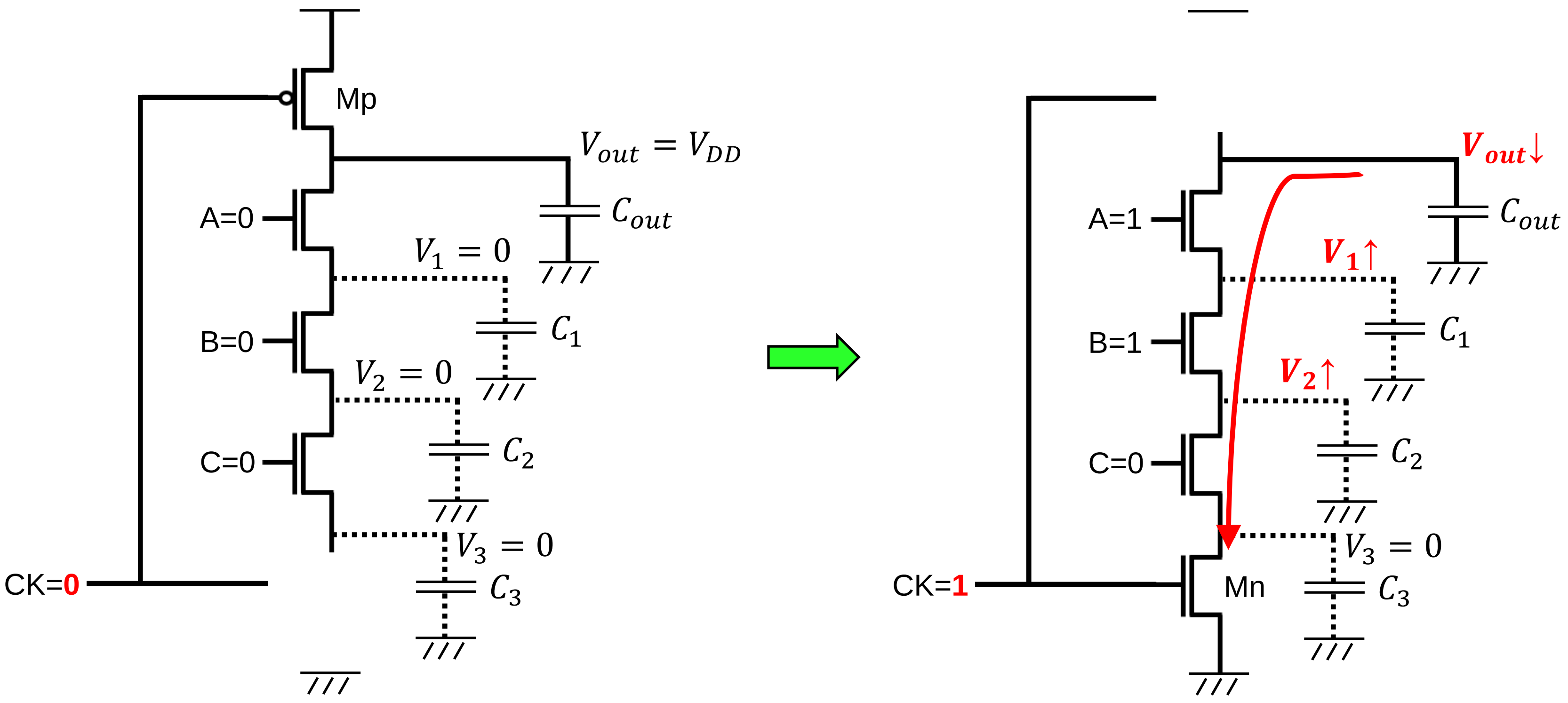
Dynamic CMOS

- Charge sharing



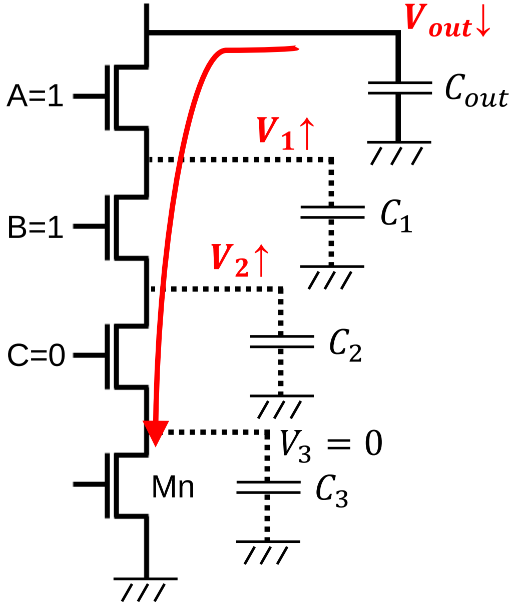
Dynamic CMOS

- Charge sharing



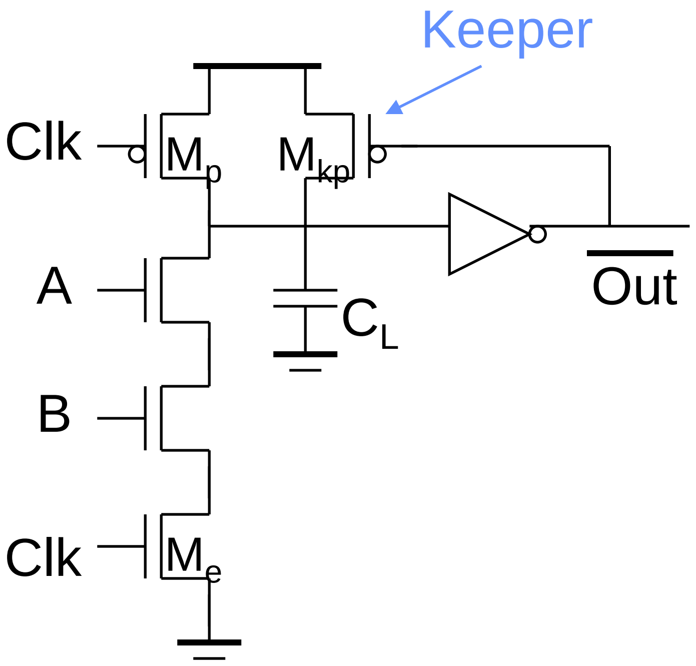
Dynamic CMOS

- Charge sharing
  - $V_{out} = V_1 = V_2$
  - $Q = C_{out}V_{DD} = C_{out}V_f + C_1V_f + C_2V_f = (C_{out} + C_1 + C_2)V_f$
  - $V_f = (\frac{C_{out}}{C_{out}+C_1+C_2})V_{DD}$



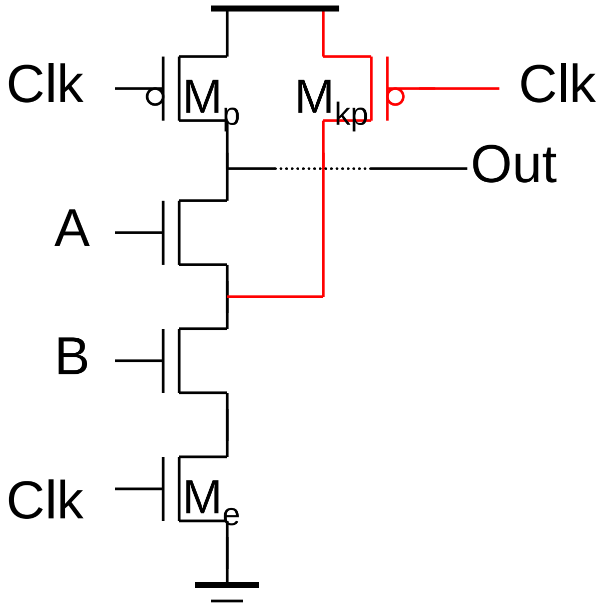
Dynamic CMOS

- How to solve the charge sharing problem
  - Constraint: $C_{out} \gg C_1 + C_2$
  - Keeper



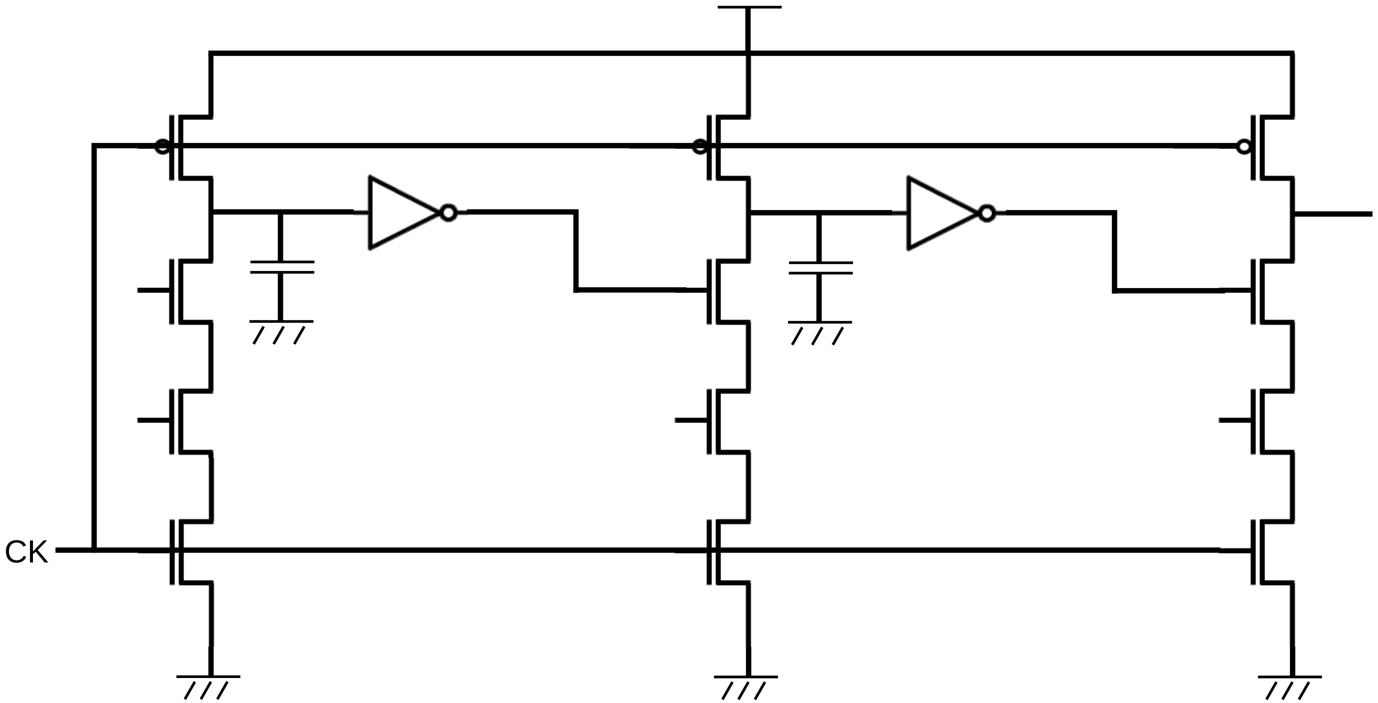
Dynamic CMOS

- How to solve the charge sharing problem

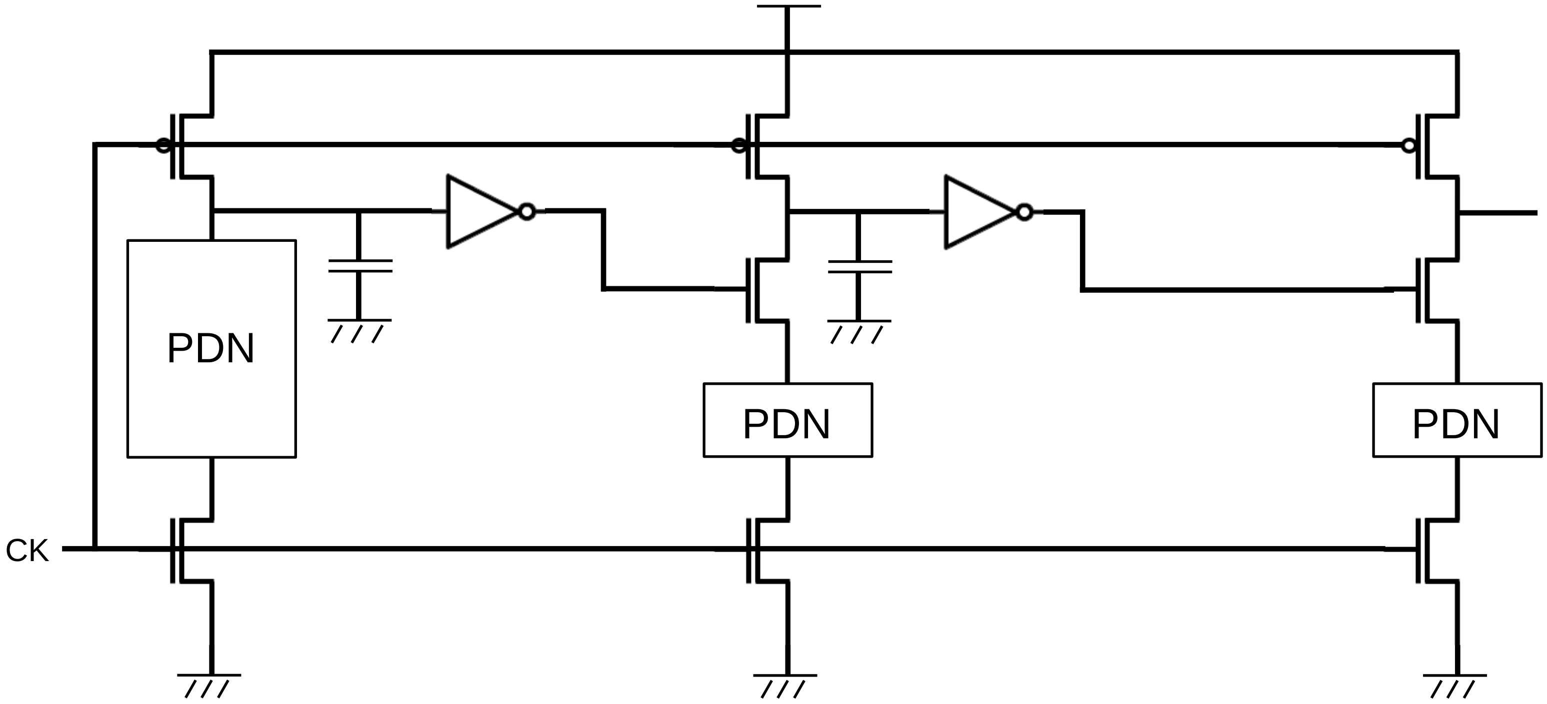


Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

Domino Logic

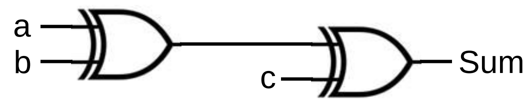


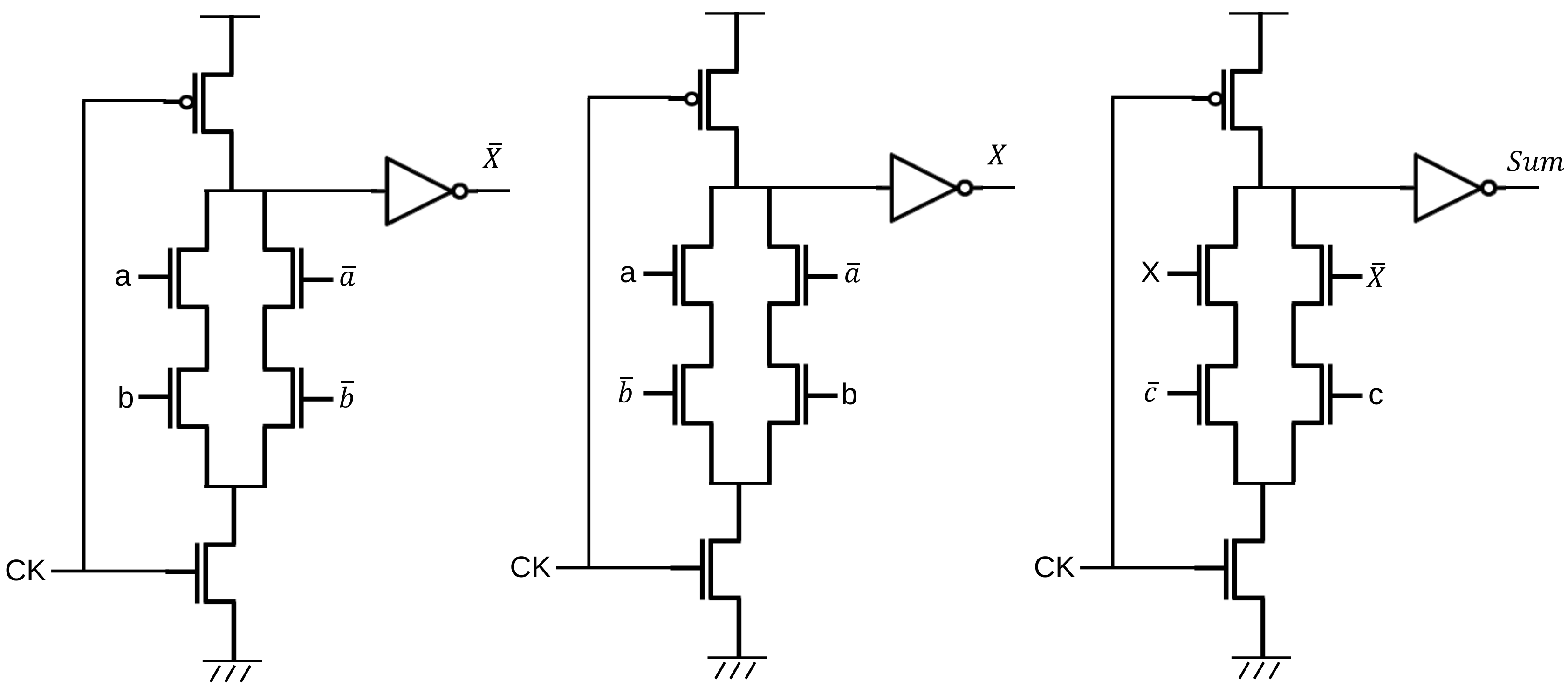
Domino Logic



Domino Logic

- Example
  - $Sum = a \oplus b \oplus c$



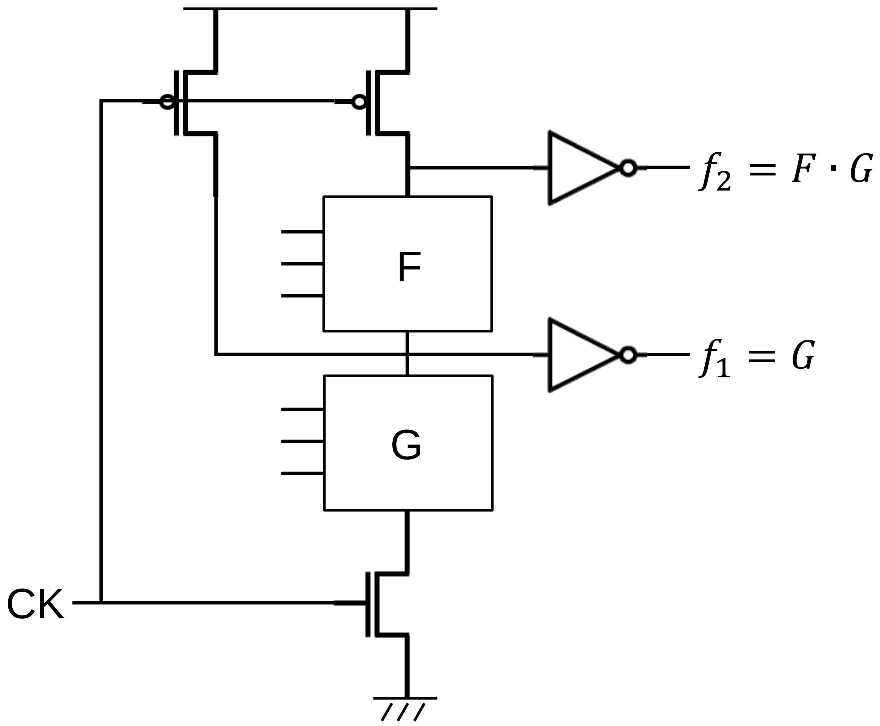


Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition
  - Input capacitance reduced

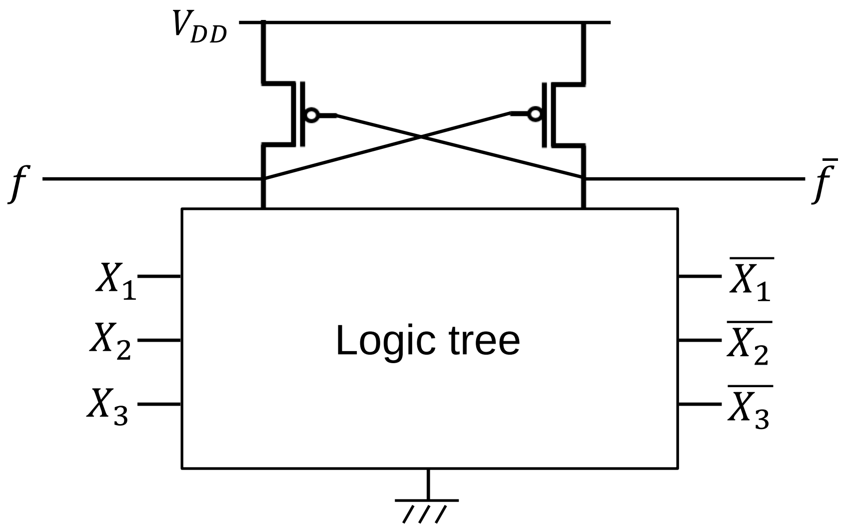
Multiple-Output Domino Logic (MODL)

- $f_1 = G$
- $f_2 = F \cdot G$



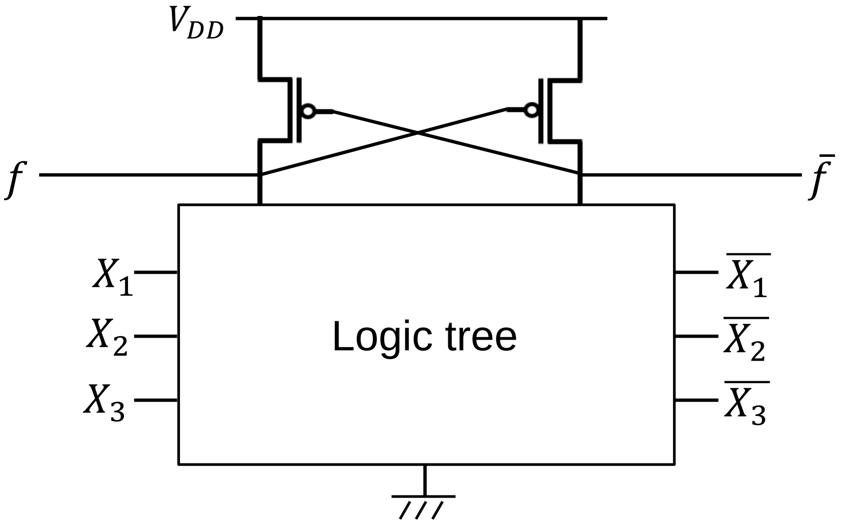
Dual-Rail Logic Network

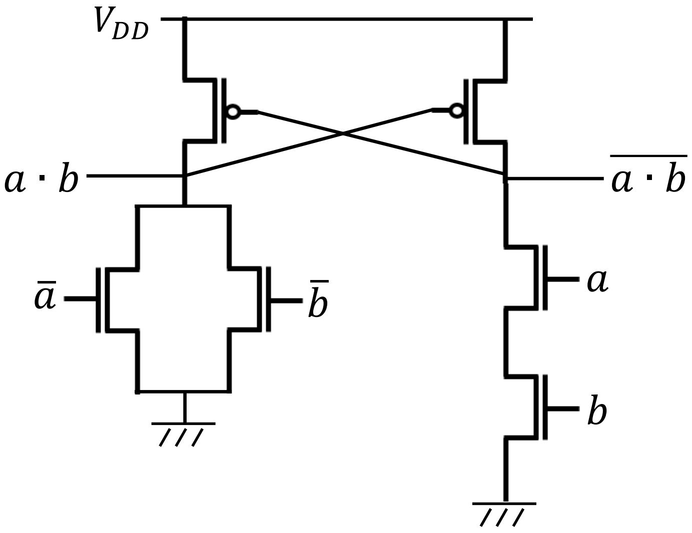
- Differential Cascode Voltage Switch Logic (DCVSL)



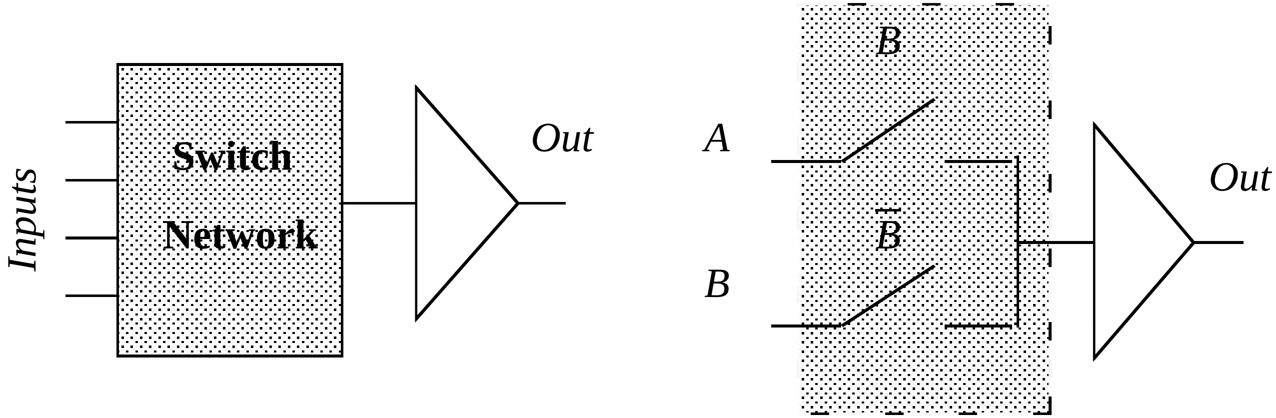
Dual-Rail Logic Network

- Differential Cascode Voltage Switch Logic (DCVSL)





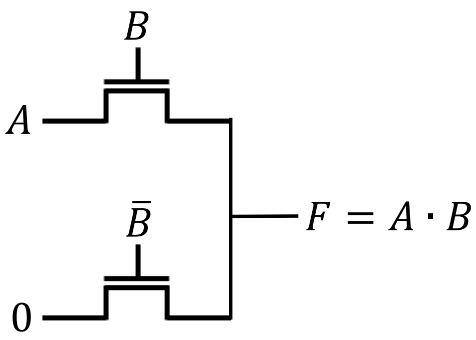
Pass Transistor Logic

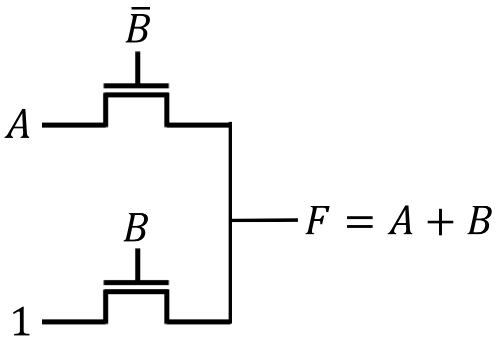


- **N transistors**
- **No static consumption**

Pass Transistor Logic

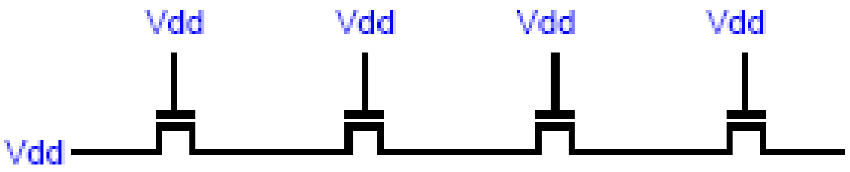
- Example

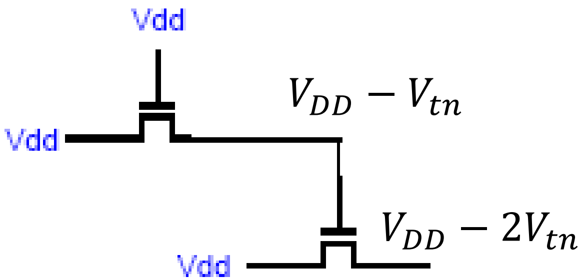




Issues with Pass Transistor Logic

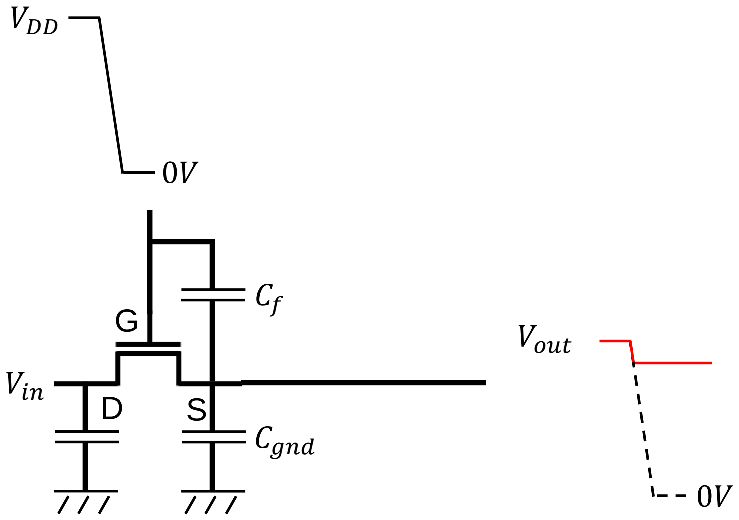
- Threshold drop
- Capacitive feed through
- Charge sharing
- Follow board notes



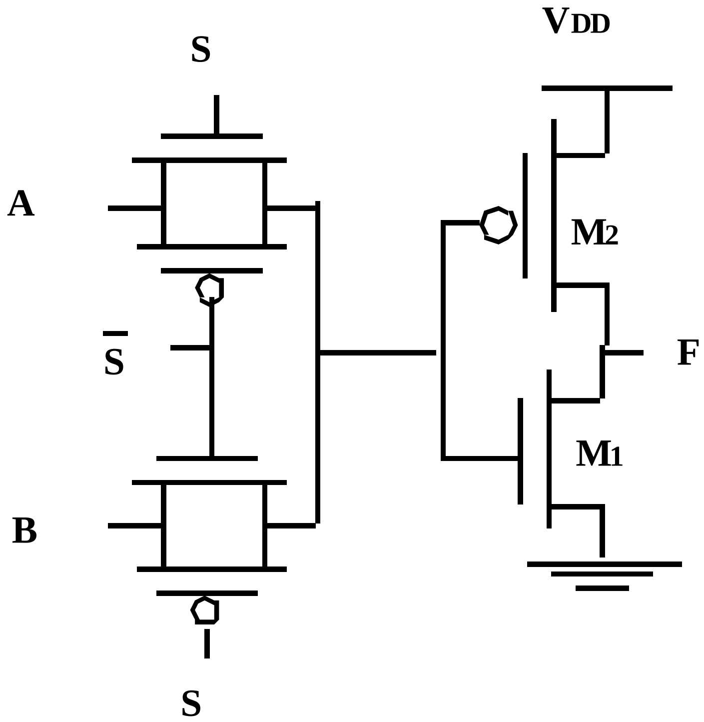


Pass Transistor Logic

- Capacitive Feedthrough



Transmission Gate Logic



• The control signal S turns the transfer gates on and off depending on its value.

• When s=1, the upper transfer gate is on and that allows A to follow to the output

• Implement the Multiplexer with static CMOS and compare with this

Transmission Gate Logic