EE434
ASIC & Digital Systems

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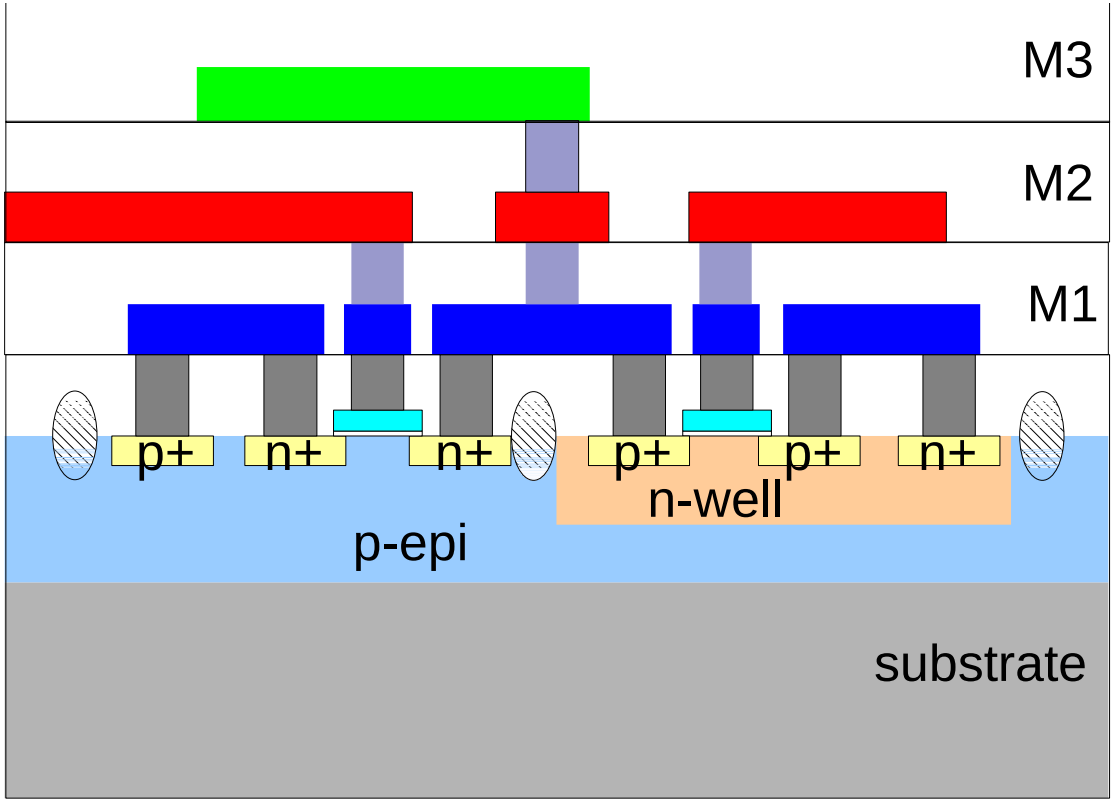
Lecture 5

Layout

Semiconductor Layers



Real Objects
Well (n, p)
Active (n+, p+)
Poly (gate)
Contact
Metal (m1, m2, …)
Via (v12, v23, …)

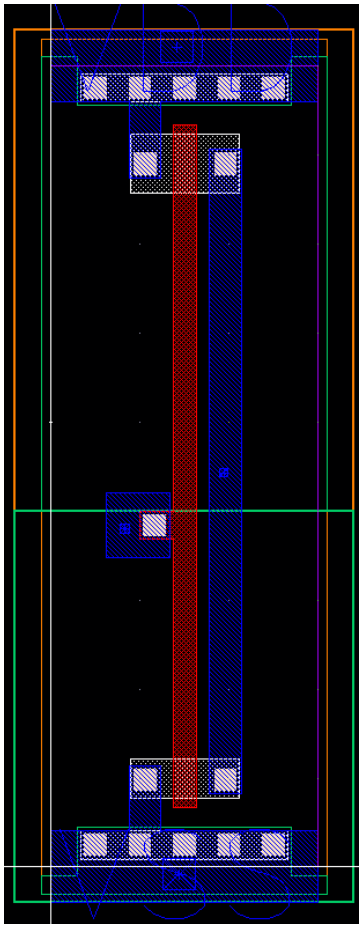
Virtual Objects
Cell boundary
Labels
Pins

Layout

- INV_X1

PMOS

NMOS

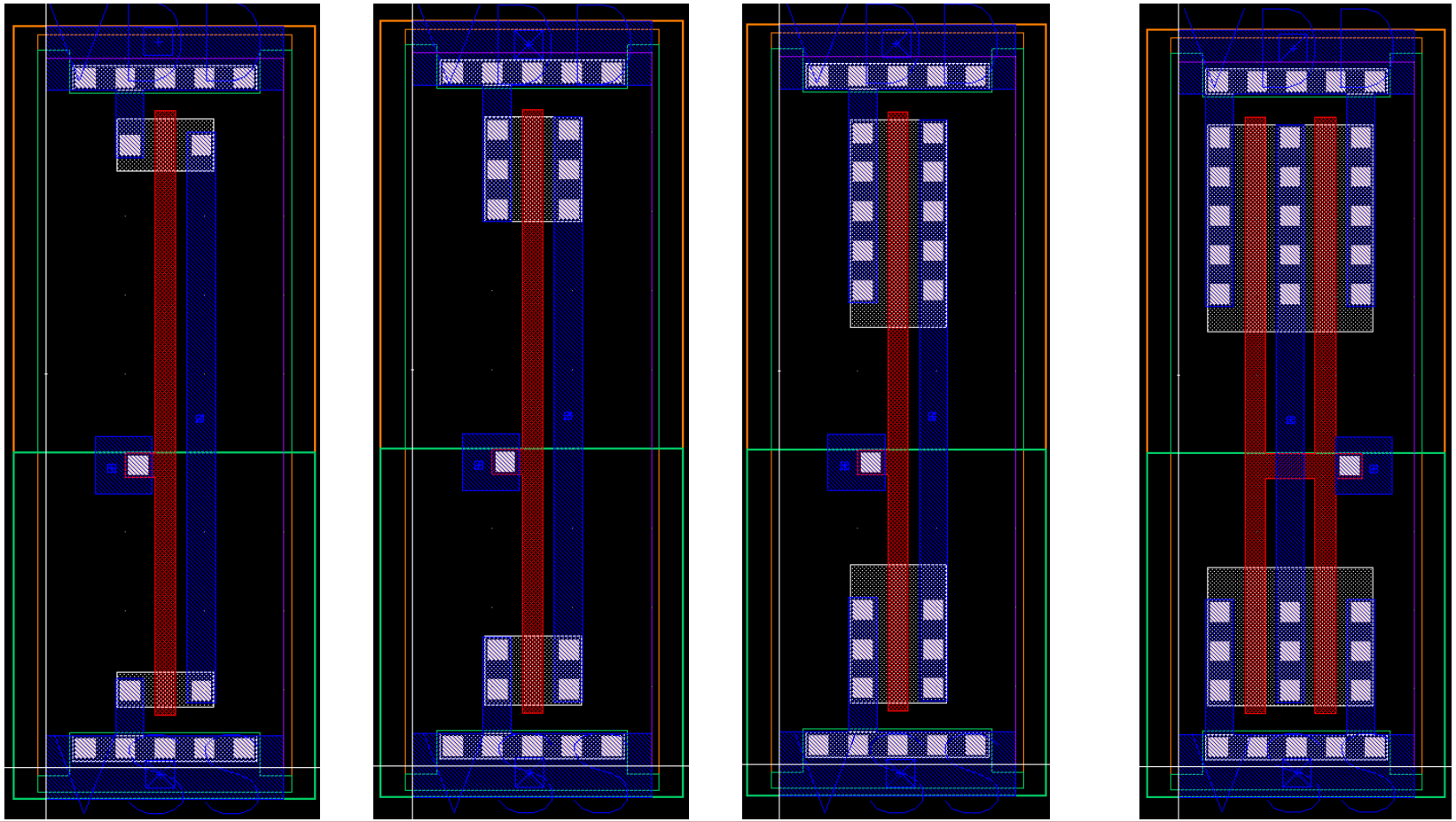


Real Objects	
Well (n, p)	
Active (n+, p+)	+ +
Poly (gate)	
Contact	
Metal (m1, m2, …)	Metal 1
Via (v12, v23, …)	

Virtual Objects	
Cell boundary	
Labels	VDD, VSS
Pins	

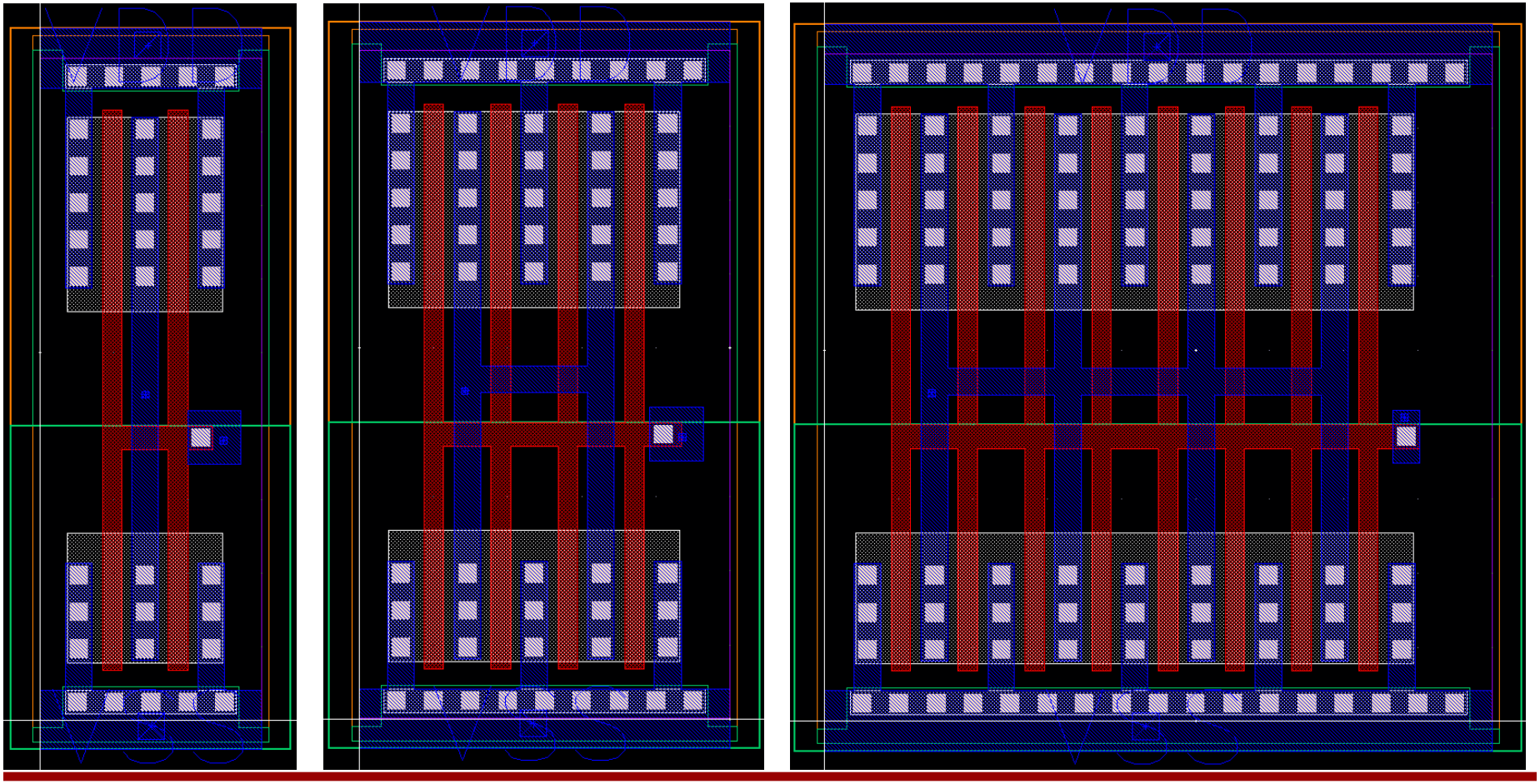
Layout

- INV_X1, INV_X2, INV_X4, INV_X8



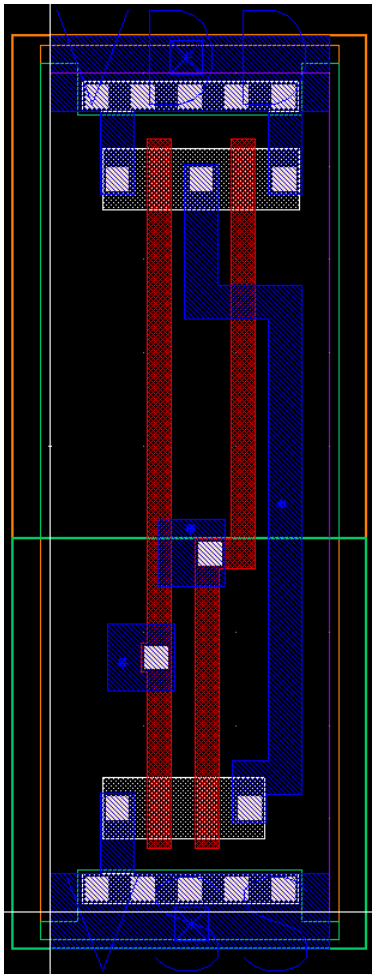
Layout

- INV_X8, INV_X16, INV_X32

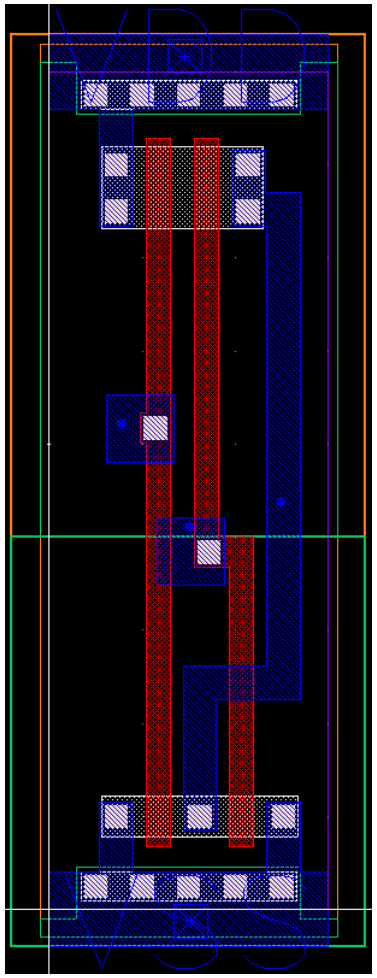


Layout

- NAND2_X1

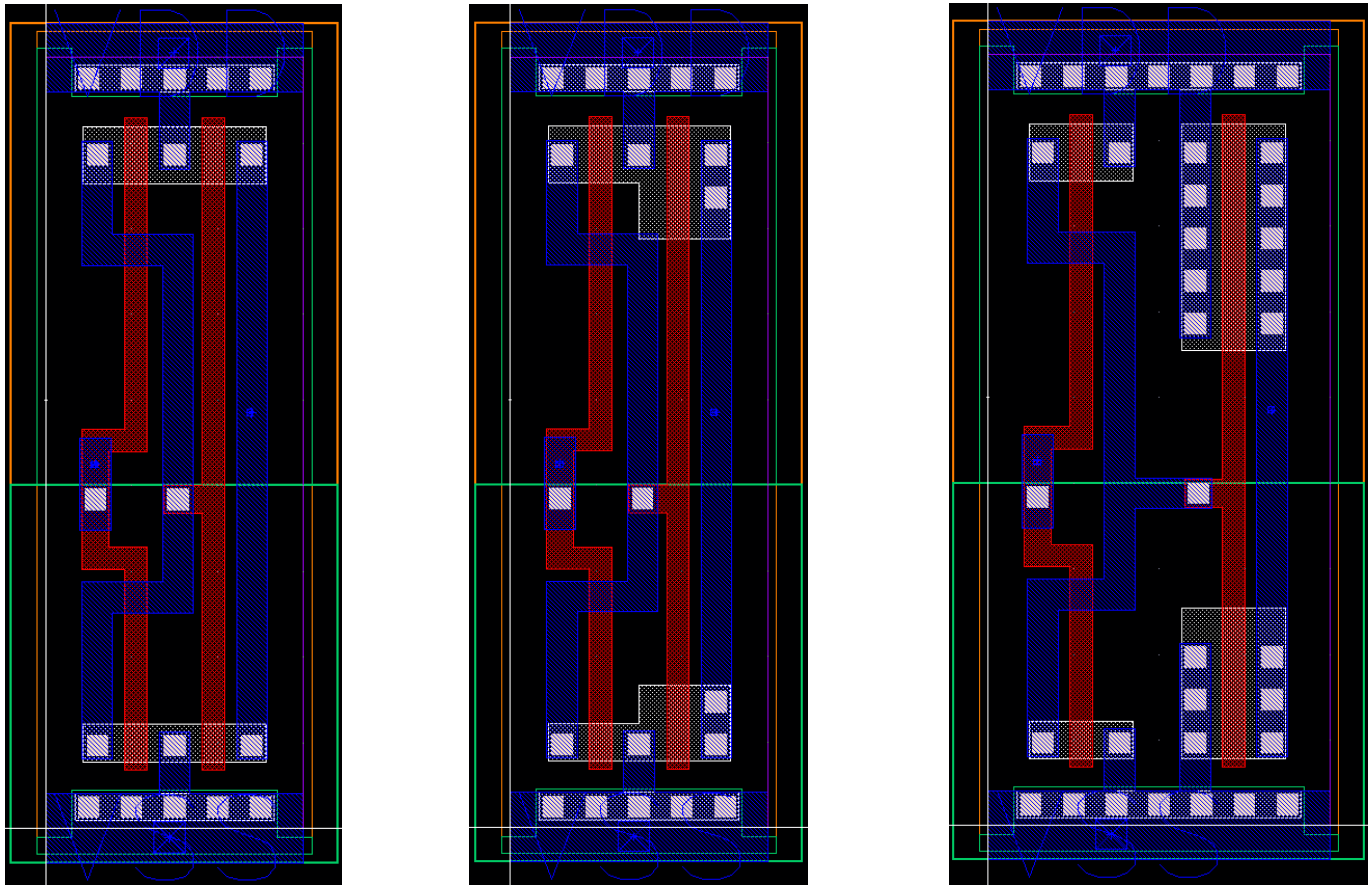


NOR2_X1



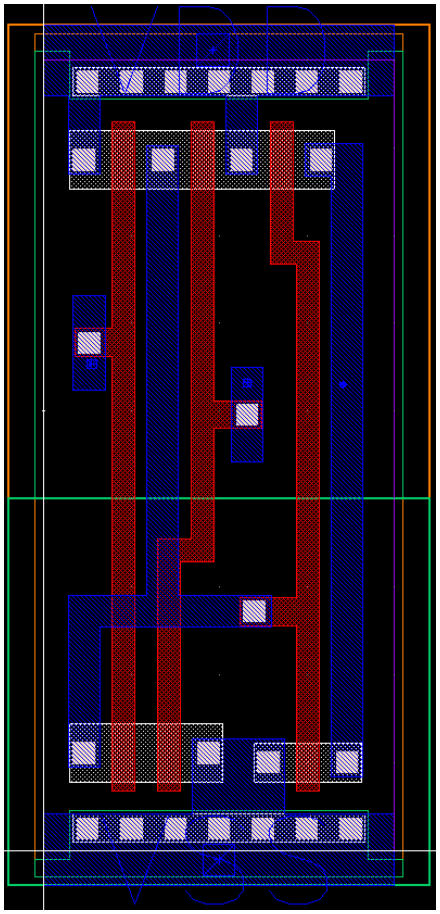
Layout

- BUF_X1, BUF_X2, BUF_X4

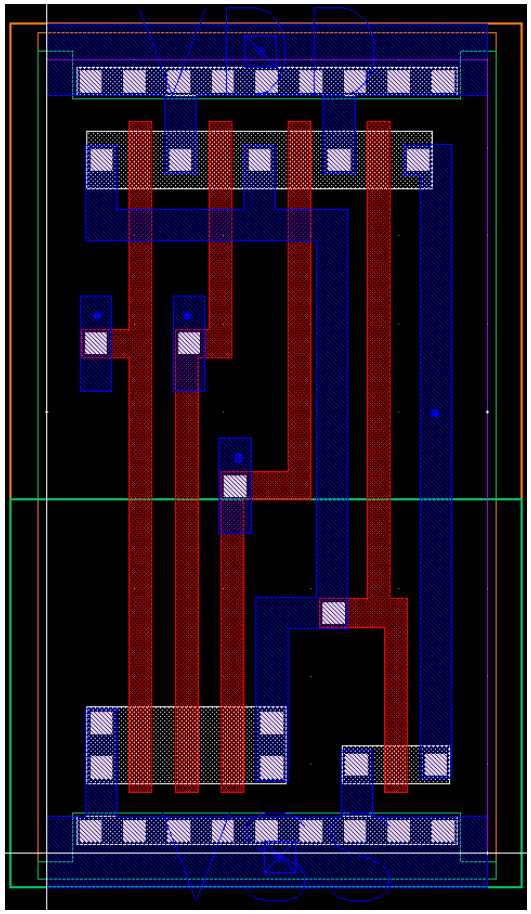


Layout

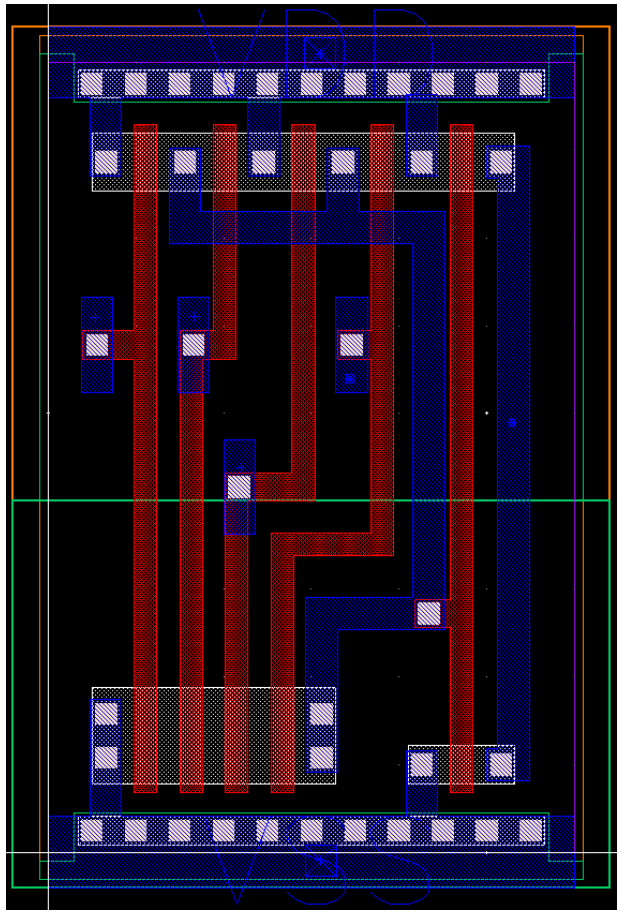
- AND2_X1



AND3_X1

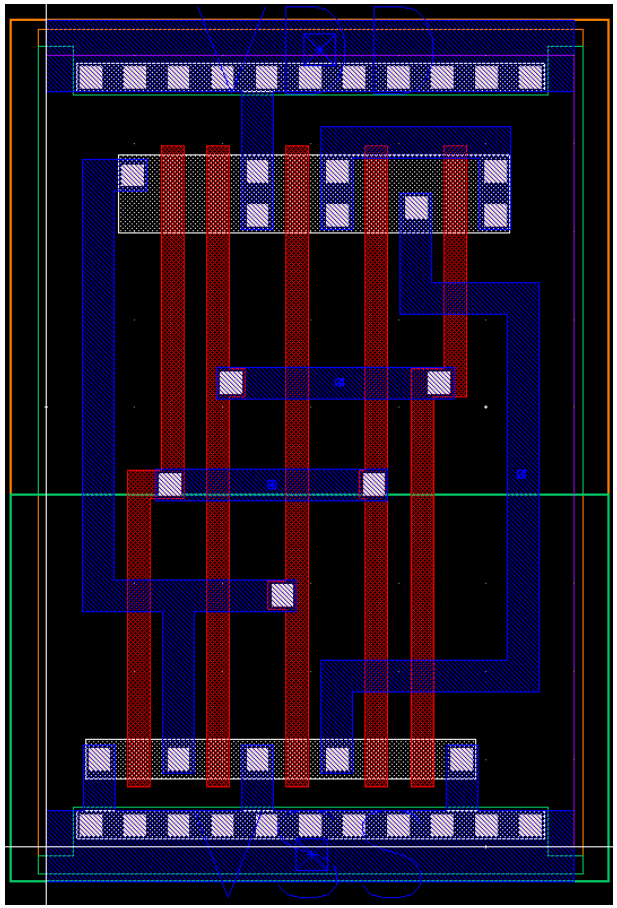


AND4_X1

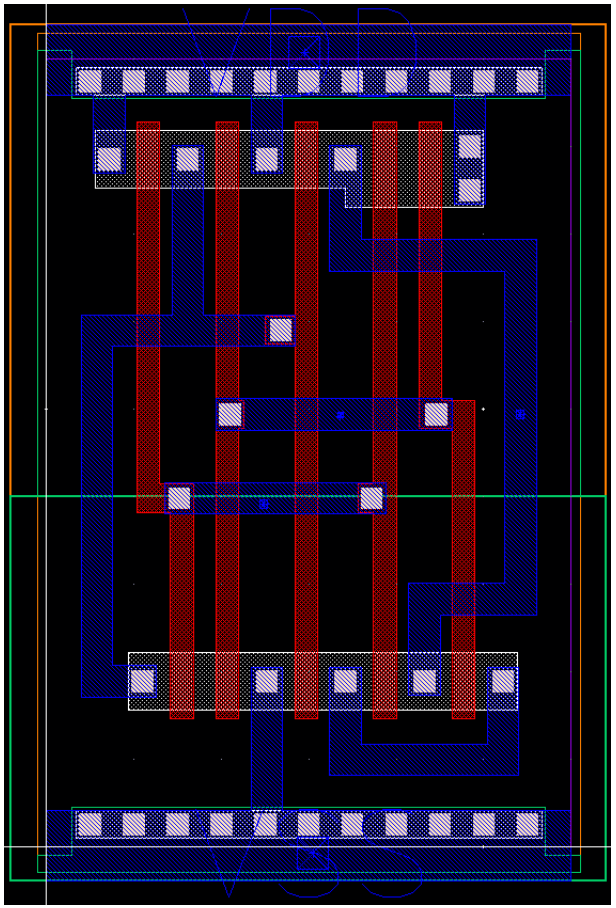


Layout

- XOR2_X1

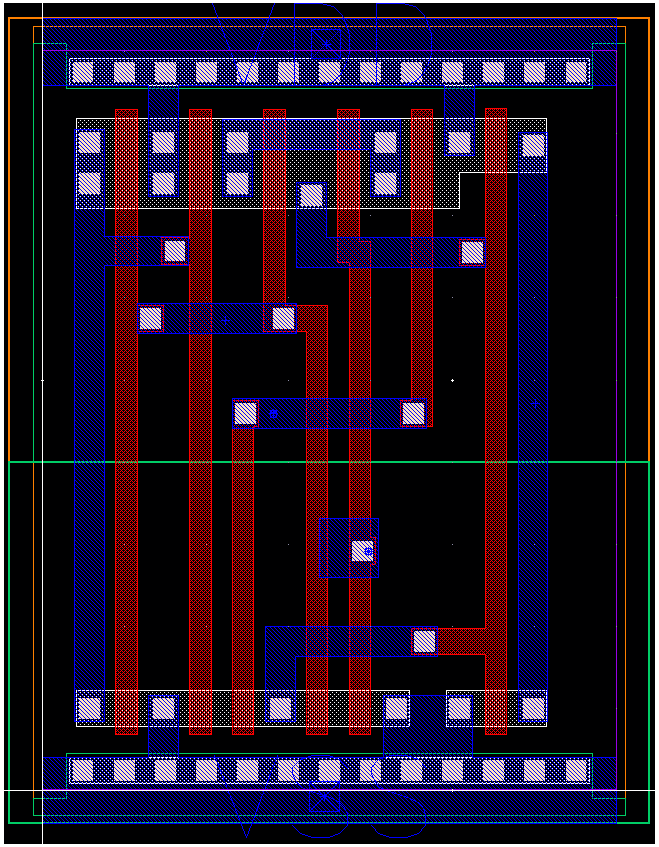


XNOR2_X1



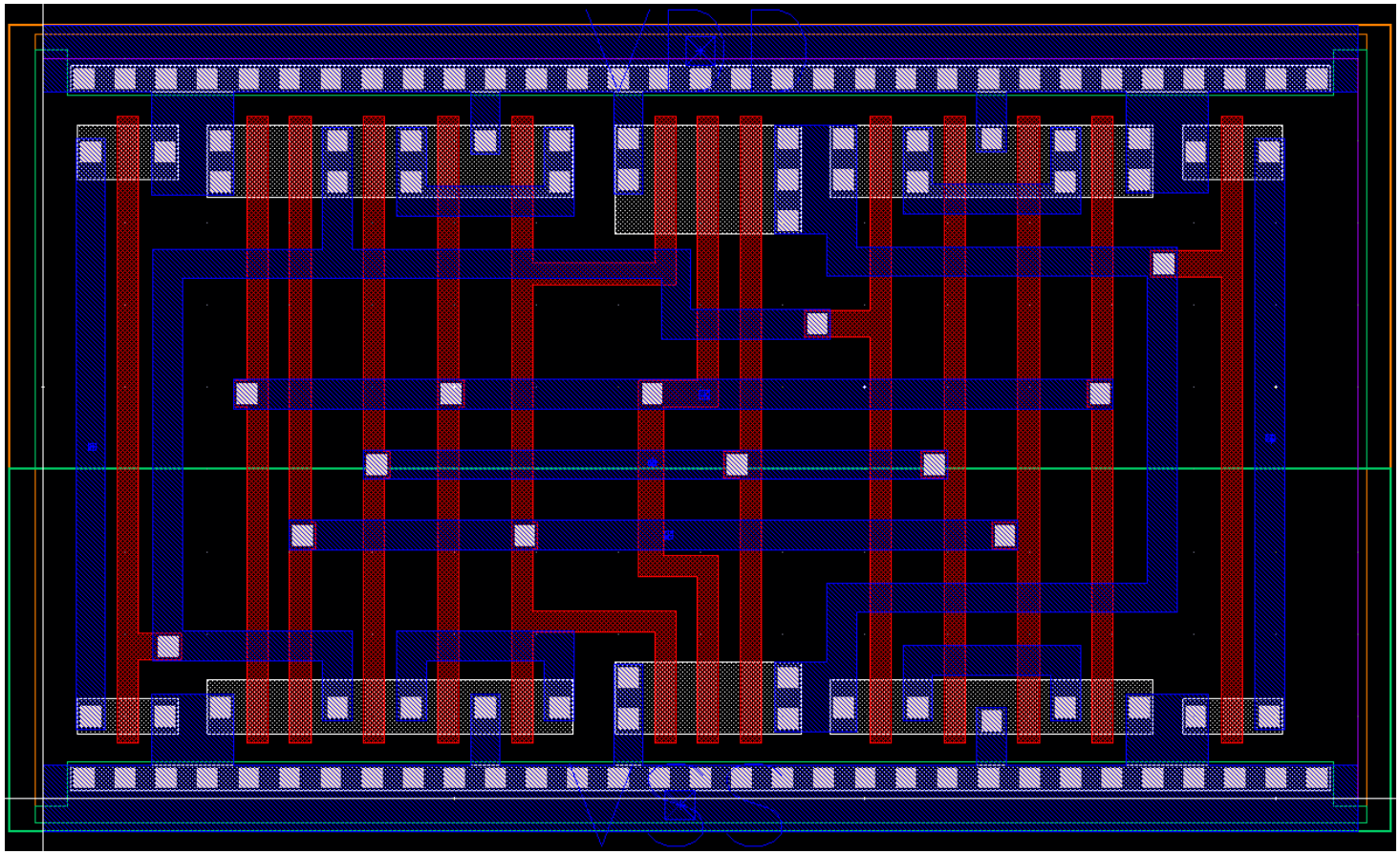
Layout

- MUX2_X1



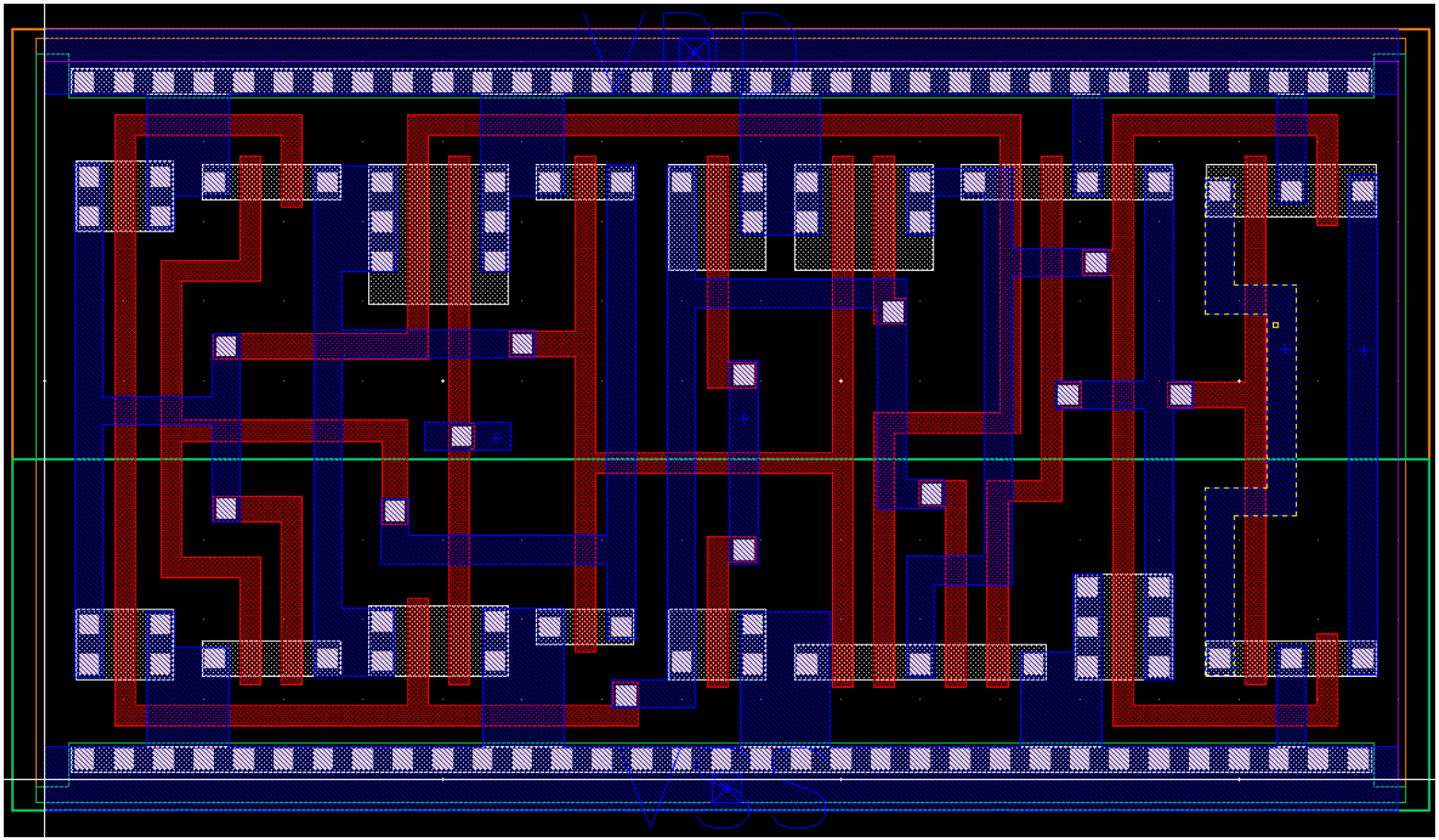
Layout

- FA_X1



Layout

- DFF_X1



Layout Generation

1. Draw a layout
   - Output: gdsii
2. Design rule check (DRC)
3. Layout vs. Schematic (LVS)
   1. Layout -> netlist 1
   2. Schematic -> netlist 2
   3. netlist 1 == netlist 2
4. Parasitic RC extraction (xRC)
   - Output: A SPICE netlist with parasitic RC
5. Simulation & Characterization