EE434
ASIC & Digital Systems

Memory

Spring 2015

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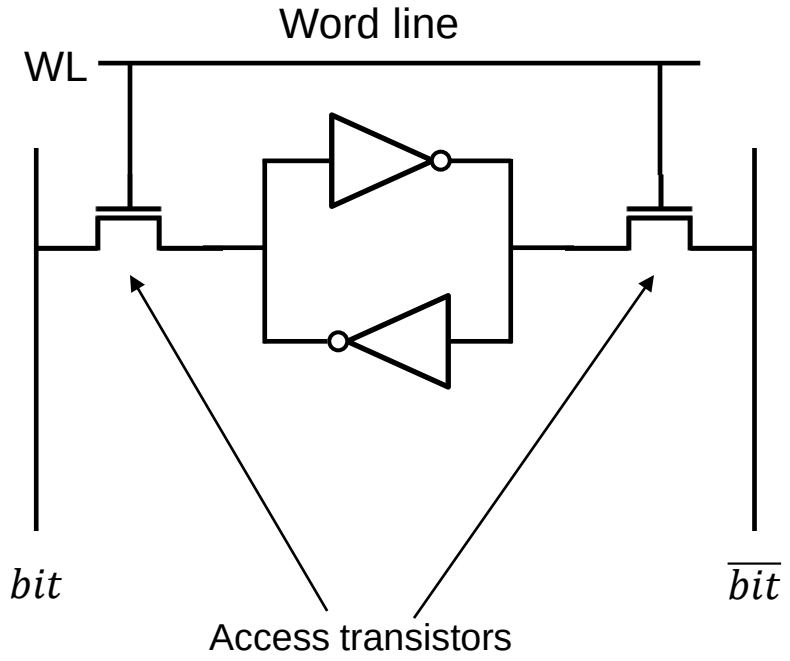
SRAM

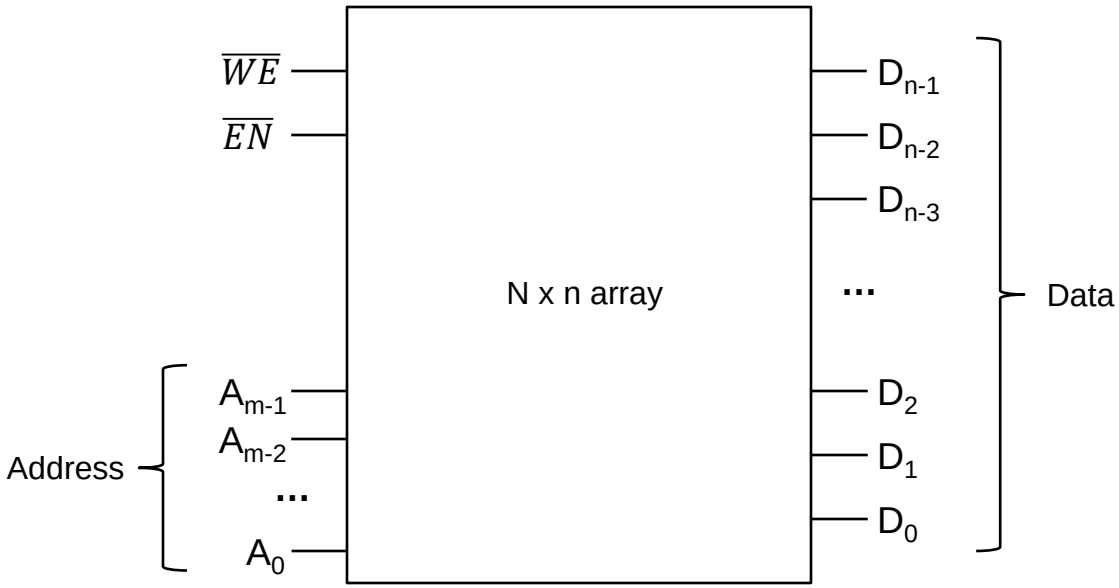
- Static Random Access Memory (SRAM)
- 6-TR SRAM cell



SRAM

- Design goal
  - Very high storage density
  - Short access time

SRAM

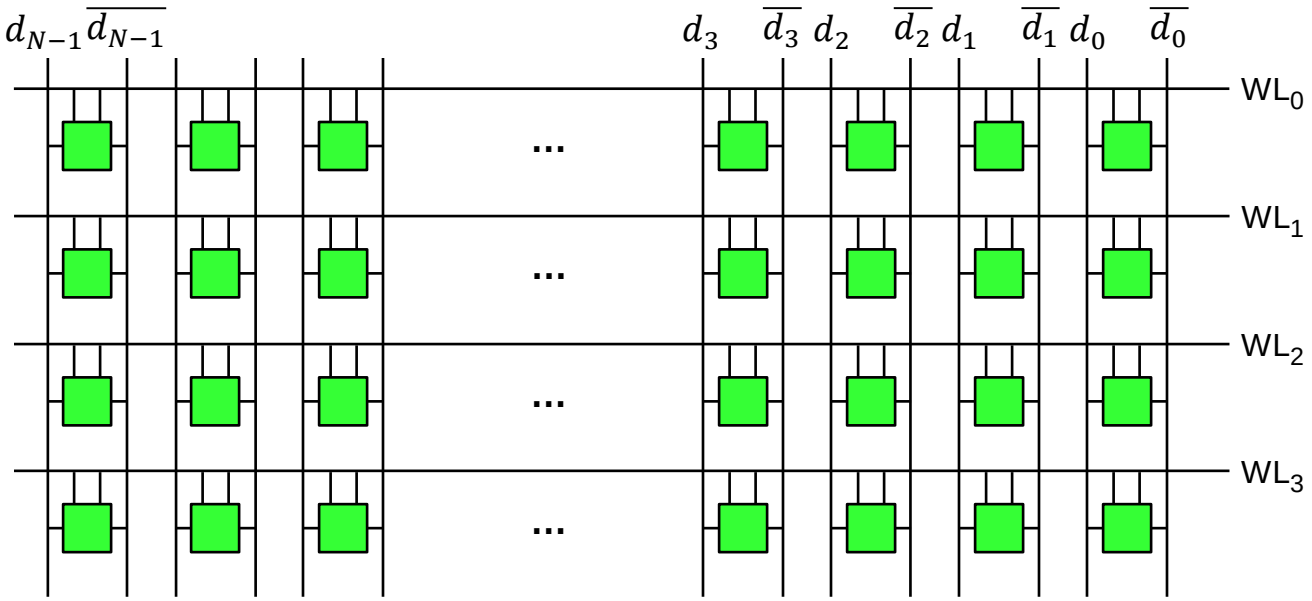

$\overline{WE}$
$\overline{EN}$
A_{m-1}
A_{m-2}
...
A_0
Address
N x n array
D_{n-1}
D_{n-2}
D_{n-3}
...
D_2
D_1
D_0
Data

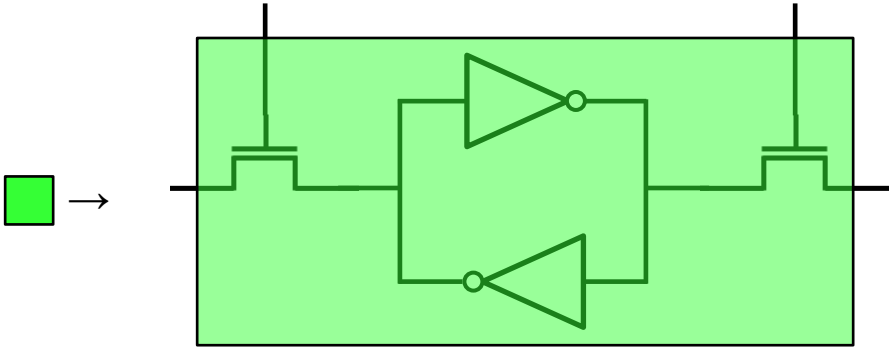
SRAM

- Example 1
  - Data: 16-bit (d-bit)
  - Address: 8-bit (a-bit)
  - Memory size = ($d*2^a$ bits) = 4096 bits = 4K bits = 512 Bytes

- Example 2
  - 512K x 8 SRAM chip = 512K 8-bit words
  - Memory size = 512K*8 bits = 4096K bits = 512K Bytes
  - Address: $2^a = 512K \rightarrow a = \log_2(512K) = 19$ bits

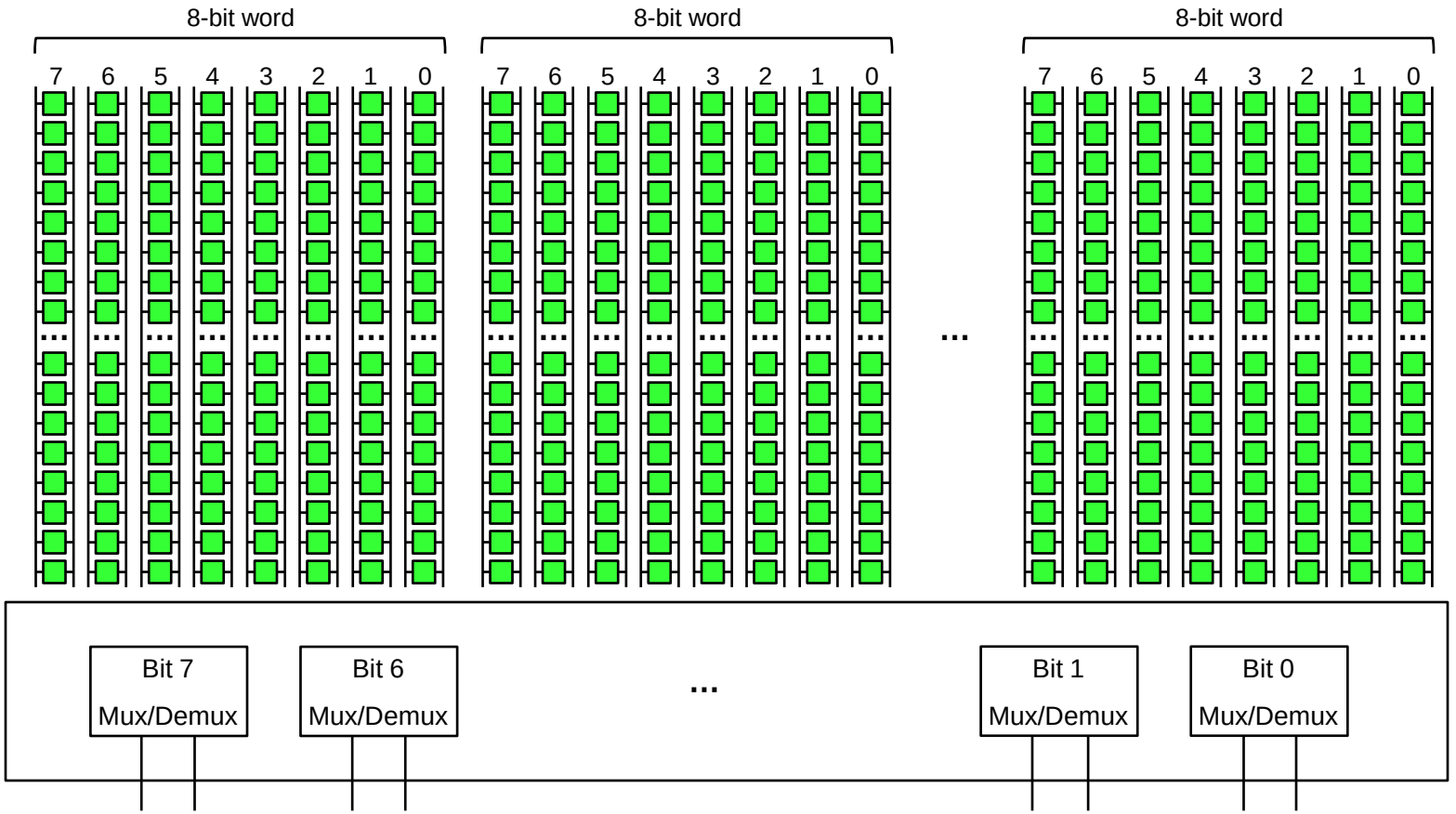
SRAM


d_{N-1} $\overline{d_{N-1}}$
d_3 $\overline{d_3}$ d_2 $\overline{d_2}$ d_1 $\overline{d_1}$ d_0 $\overline{d_0}$
WL0
WL1
WL2
WL3
...

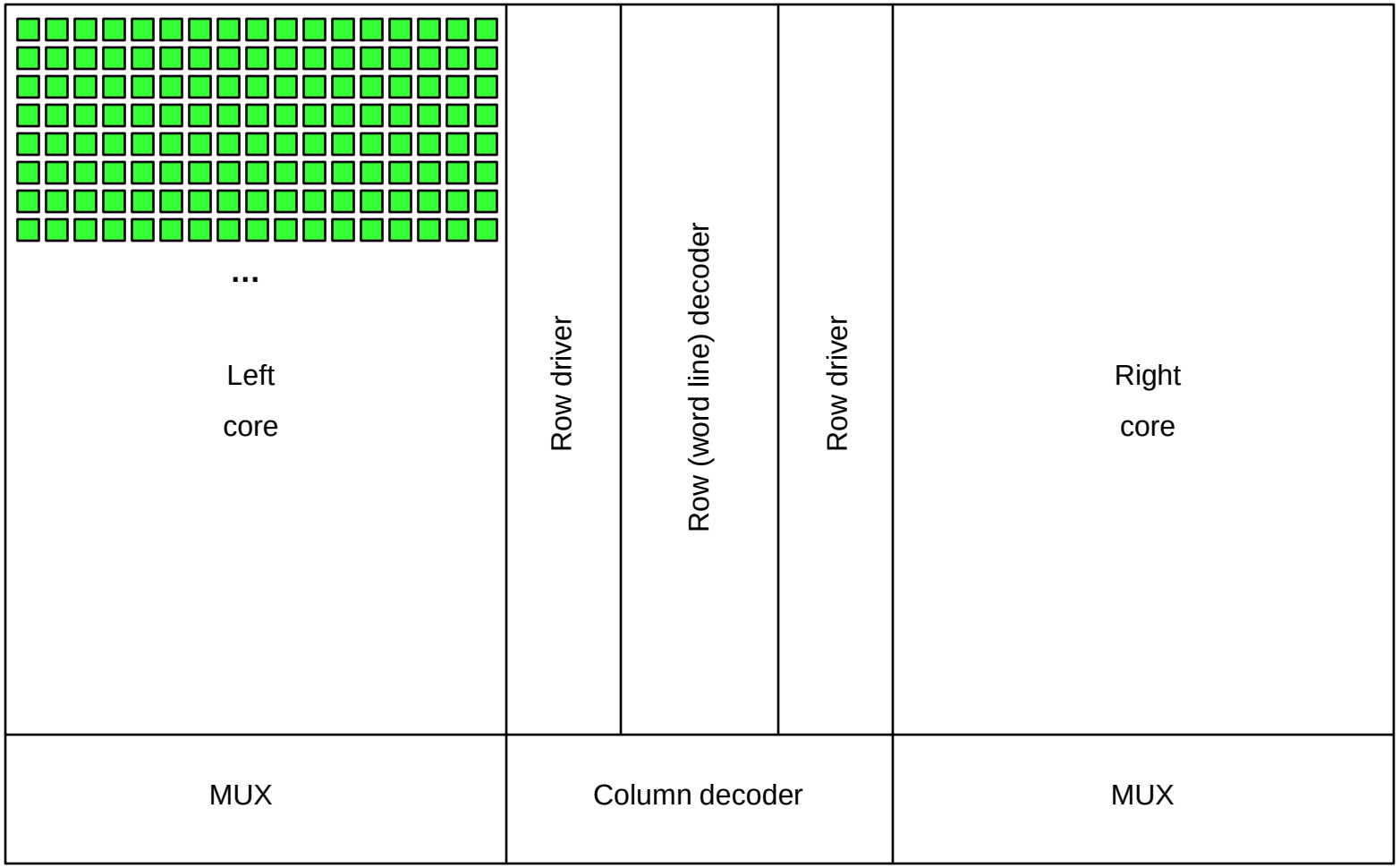


SRAM

- Column mux/demux

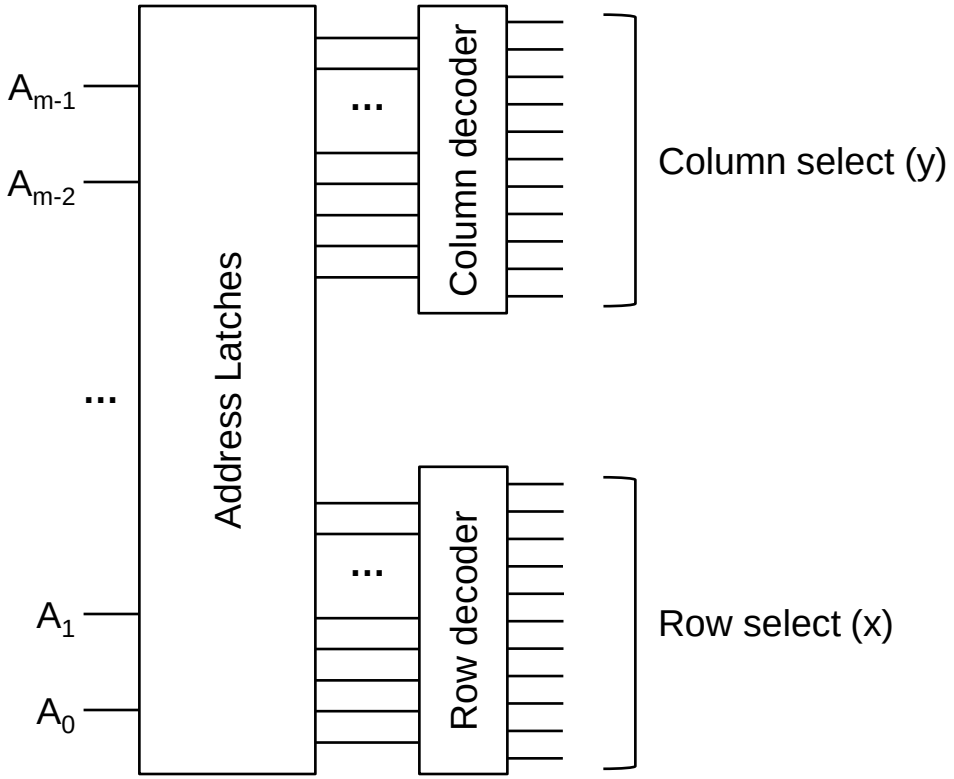


SRAM


...
Left
core
Row driver
Row (word line) decoder
Row driver
Right
core
MUX
Column decoder
MUX

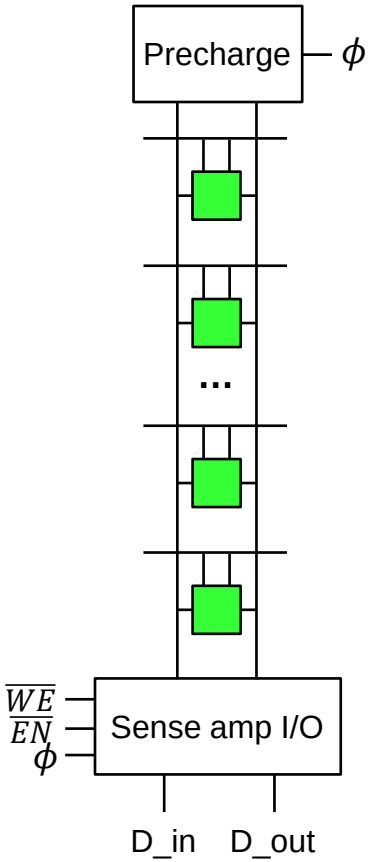
SRAM

- Addressing scheme



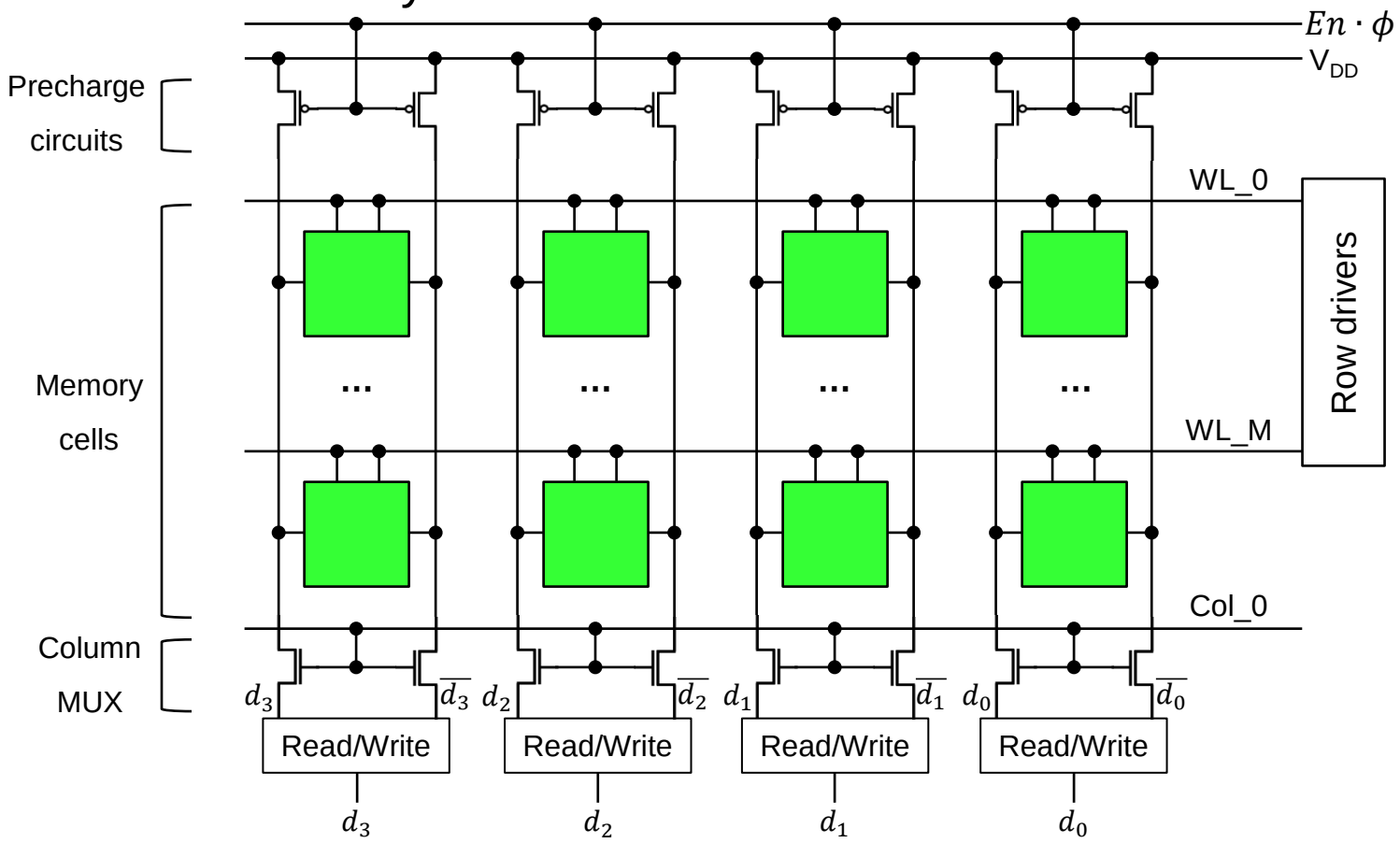
SRAM

- Precharge and I/O circuits for a single column



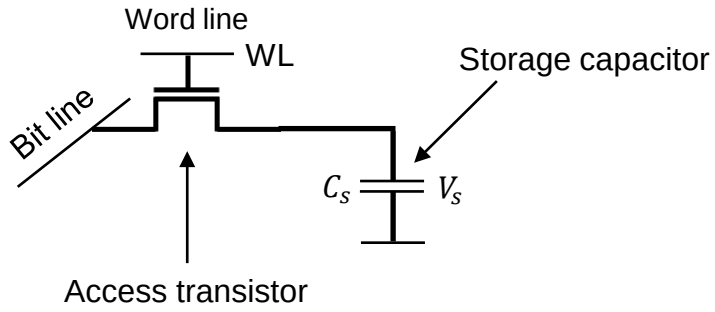
SRAM

- Column circuitry



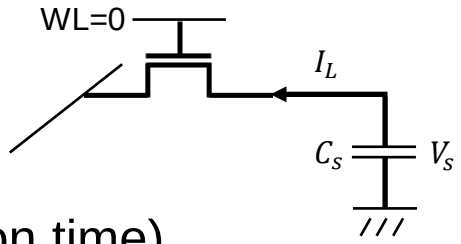
DRAM

- Dynamic RAM (DRAM)
- 1T DRAM cell



DRAM

- Charge leakage problem



- Hold time (= retention time)
  - The longest period of time that the cell can maintain a voltage large enough to be interpreted as a logic 1.
  - $t_h \approx \left(\frac{C_s}{I_L}\right)(\Delta V_s)$
  - Ex) $I_L = 1nA, C_s = 50fF, \Delta V_s = 1V \rightarrow t_h = 0.5\mu s$

- Need refresh.
  - $f_{refresh} \approx \frac{1}{2t_h}$

DRAM

- Refresh operation