Homework Assignment 1
(Due Jan. 29th at the beginning of the class)

***** Submission policy: Please zip your source code and waveform screenshots into a single file and send it to daehyun@eecs.wsu.edu. The file name should be *firstname_lastname*.zip (or .tar.gz or .tar …)

(1) **[VHDL, 10 points]** Make a VHDL code for a 4:1 mux and test it with the following spec.

- Input ports: i0, i1, i2, i3, s1, s0
- Output port: z
- Function: z=i0 when (s1s0=00), z=i1 when (s1s0=01), z=i2 when (s1s0=10), z=i3 when (s1s0=11)
- Test input vectors (i3,i2,i1,i0,s1,s0)
  - 000000 → 000100 → 000101 → 000110 → 000111 → 000100 → 000000 → 001000 → 001001 → 001010 → 001011 → 001000 → 000000 → 010000 → 010001 → 010010 → 010011 → 010000 → 000000 → 100000 → 100001 → 100010 → 100011 → 100000
- [**Submit**] Source code + test waveform (inputs + outputs)

(2) **[VHDL, 10 points]** Make a VHDL code for a D-latch and test it with the following spec.

- Input ports: D, Clk
- Output ports: Q, QN
- Function: If Clk=0, $Q=Q_{prev}$, $QN=QN_{prev}$. If Clk=1, Q=D, $QN=\overline{D}$.
- Test input vectors (D, Clk)
  - 00 → 01 → 00 → 10 → 00 → 01 → 11 → 01 → 11 → 10 → 00 → 10 → 00 → 01 → 00 → 10 → 00
- [**Submit**] Source code + test waveform (inputs + outputs)