Homework Assignment 2
(Due Feb. 1st at the beginning of the class)

***** Submission policy: Please zip your source code and waveform screenshots into a single file and send it to daehyun@eecs.wsu.edu. The file name should be *firstname_lastname*.zip (or .tar.gz or .tar …)

(1) **[VHDL, 10 points]** Design a positive-edge-triggered D-FF with synchronous reset and set. Use the following spec:

- Input ports: D, R, S, Clk
- Output port: Q
- Function:
  - Q = 0 if reset = 1 (regardless of D and set) when Clk ↑.
  - Q = 1 if reset = 0 and set = 1 (regardless of D) when Clk ↑.
  - Q = D if reset = 0 and set = 0 when Clk ↑.
- Create your own test input vectors to test all the following 16 combinations:
  - reset=0, set=0, D=0, Clk ↑ (when Q=0)
  - reset=0, set=0, D=0, Clk ↑ (when Q=1)
  - reset=0, set=0, D=1, Clk ↑ (when Q=0)
  - reset=0, set=0, D=1, Clk ↑ (when Q=1)
  - **…**
- [**Submit**] Source code + test waveform (inputs + outputs)

(2) **[VHDL, 10 points]** Design a positive-edge-triggered D-FF with asynchronous reset and set. Use the following spec:

- Input ports: D, R, S, Clk
- Output ports: Q
- Function:
  - Q = 0 if reset = 1 (regardless of D, set, and Clk).
  - Q = 1 if reset = 0 and set is 1 (regardless of D and Clk).
  - Q = D if reset = 0 and set is 0 when Clk ↑.
  - Test your design using the same input vectors you created above.
- [**Submit**] Source code + test waveform (inputs + outputs)