Homework Assignment 3
(Due Feb. 10th at the beginning of the class)

***** Submission policy: Please zip your source code and waveform screenshots into a single file and send it to daehyun@eecs.wsu.edu. The file name should be *firstname_lastname*.zip (or .tar.gz or .tar …)

(1) **[Synthesis, 10 points]** Click "Labs" in the course webpage and read "tut-dc.pdf". It explains how to run Design Compiler. Then, download the following file into your working directory.

- http://eecs.wsu.edu/~ee434/Homework/hw03.zip
- Unzip it.
  - > unzip hw03.zip
- You will see the following files.
  - dlatch.vhd (VHDL code for D-latches)
  - dlatch_tb.vhd (VHDL code to test D-latches)
  - add8.vhd (VHDL code for 8-bit adders)
  - add8_tb.vhd (VHDL code to test 8-bit adders)
- Synthesize the d-latch code (use the same std. cell library file).
- Save the synthesized netlist into dlatch_syn.v.
- Open dlatch_syn.v in a text editor and see the netlist. It will have a single D-latch cell.
- Run ModelSim, create a new project, and add the following files to the project:
  - dlatch_tb.vhd
  - dlatch_syn.v
  - NangateOpenCellLibrary.v
- Compile them and simulate it (until 12ns). Does the synthesized netlist work well?
- [**Submit**] The synthesized netlist (dlatch_syn.v) and a snapshot of your test waveform.

(2) **[Synthesis, 10 points]** Synthesize the 8-bit adder (add8.vhd) and save the netlist into add8_syn.v. Run ModelSim, create a new project (or you can just open an existing project), and add (add8_syn.v, add8_tb.vhd, NangateOpenCellLibrary.v) to the project. Simulate test_myADD8 until 5ns. Verify the output result against the expected output values in add8_tb.vhd.

- [**Submit**] The synthesized netlist (add8_syn.v) and a snapshot of your test waveform.