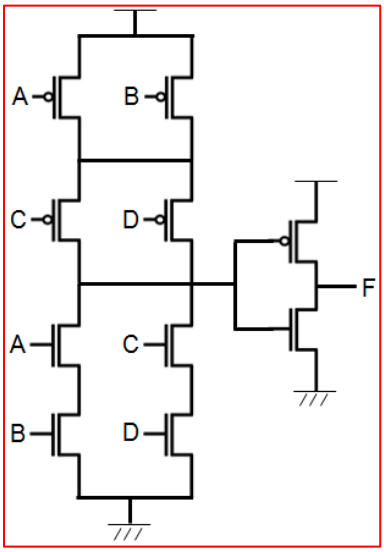
Homework Assignment 4
(Due Feb. 22nd at the beginning of the class)

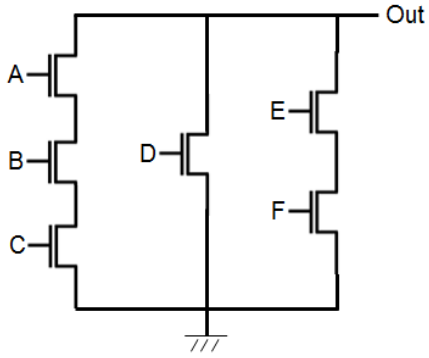
(1) **[Static CMOS Gates, 5 points]** Draw a transistor-level schematic for the following function. Use (6 NMOS and 6 PMOS transistors) or (5 NMOS and 5 PMOS transistors).

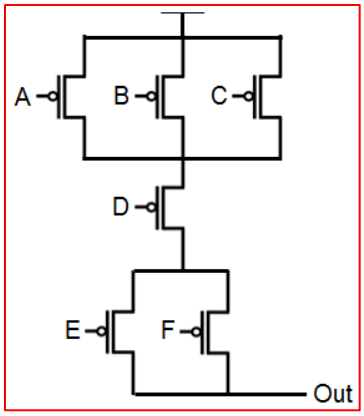
$$F = A \cdot B + C \cdot D$$



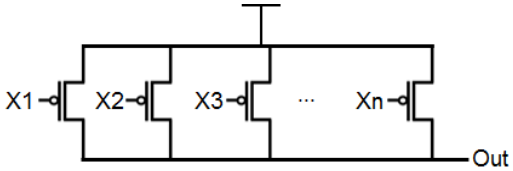
(or $F = \overline{\overline{A \cdot B} + \overline{C \cdot D}} = \overline{A \cdot B \cdot C \cdot D}$, so you can use three two-input NAND gates (6 NMOS + 6 PMOS transistors))

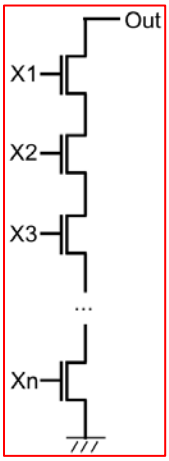
(2) **[Static CMOS Gates, 5 points]** A pull-down network of a Boolean function is shown below. Draw its pull-up network to complete the function.





(3) **[Static CMOS Gates, 5 points]** A pull-up network of a Boolean function is shown below. Draw its pull-down network to complete the function.

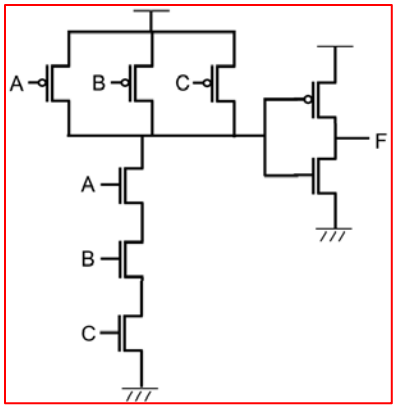




(4) **[Static CMOS Gates, 5 points]** Draw a transistor-level schematic for the following function. Try to minimize # transistors. Inverted inputs are not provided.

$$\boldsymbol{F = \overline{\overline{A} + \overline{B} + \overline{C}}}$$

$$\boldsymbol{F = A \cdot B \cdot C}$$


A
B
C
F
A
B
C