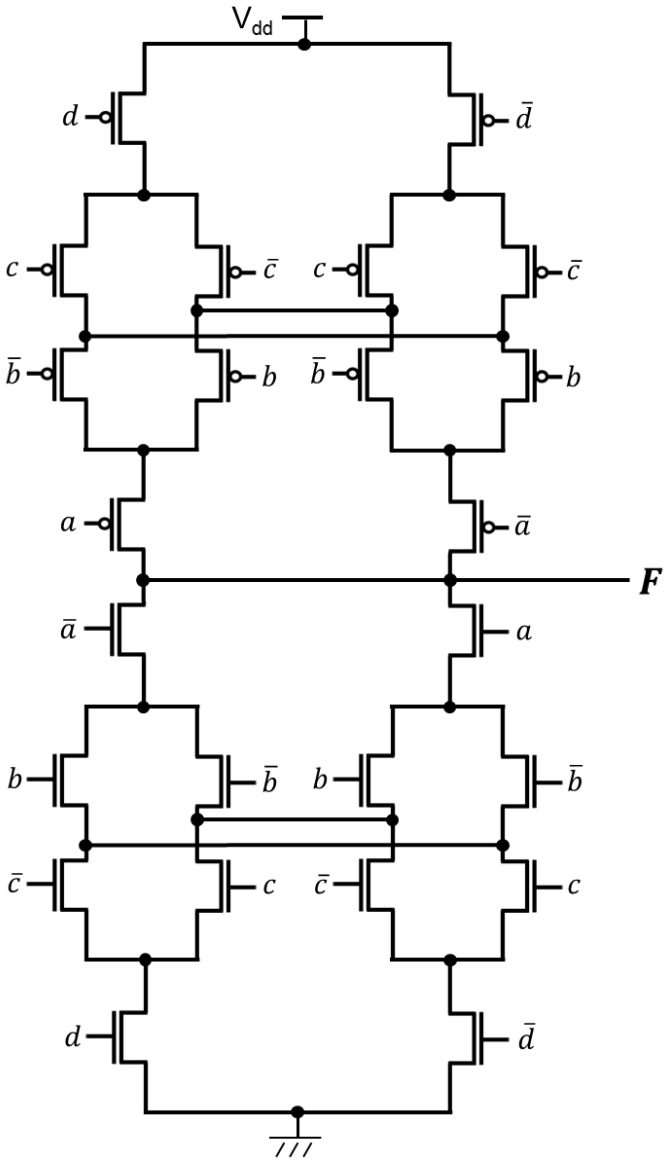
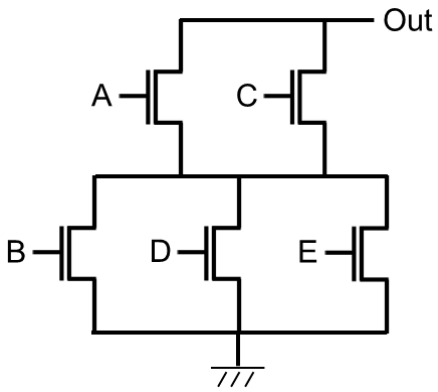
Homework Assignment 6
(Due Mar. 4th at the beginning of the class)

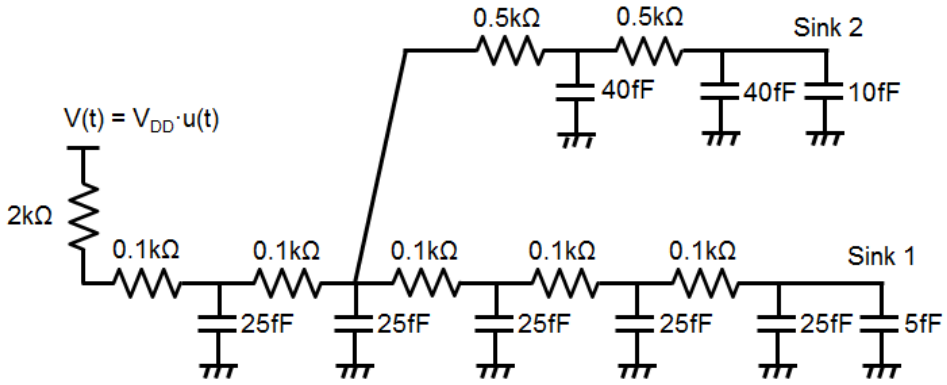
(1) **[Transistor Sizing, 5 points]** $\mu_n = 2\mu_p$. R is the resistance of a 1X NMOS transistors. The target time constant is RC where C is the load capacitance. Size the transistors in the following figure to satisfy the target time constant (try not to over-optimize them).



(2) **[Transistor Sizing, 5 points]** R is the resistance of a 1X NMOS transistors. The target time constant is RC where C is the load capacitance. Size the transistors in the following pull-down network to satisfy the time constant. However, **<u>minimize</u>** the total width of the transistors.



(3) **[Elmore Delay, 5 points]** Compute Elmore delay at Sink 1 and Sink 2 in the following figure.



(4) **[Switching Characteristics, 5 points]** Compute the rise time at the output node in the following figure. C_1 and C_2 are parasitic capacitances at the internal nodes. The input switches from (A, B, C, D, E, F) = (1, 0, 0, 0 0, 0) to (0, 0, 0, 1, 0, 1). Use R_X (where X=A, B, C, D, E, F) for the resistance of transistor X.