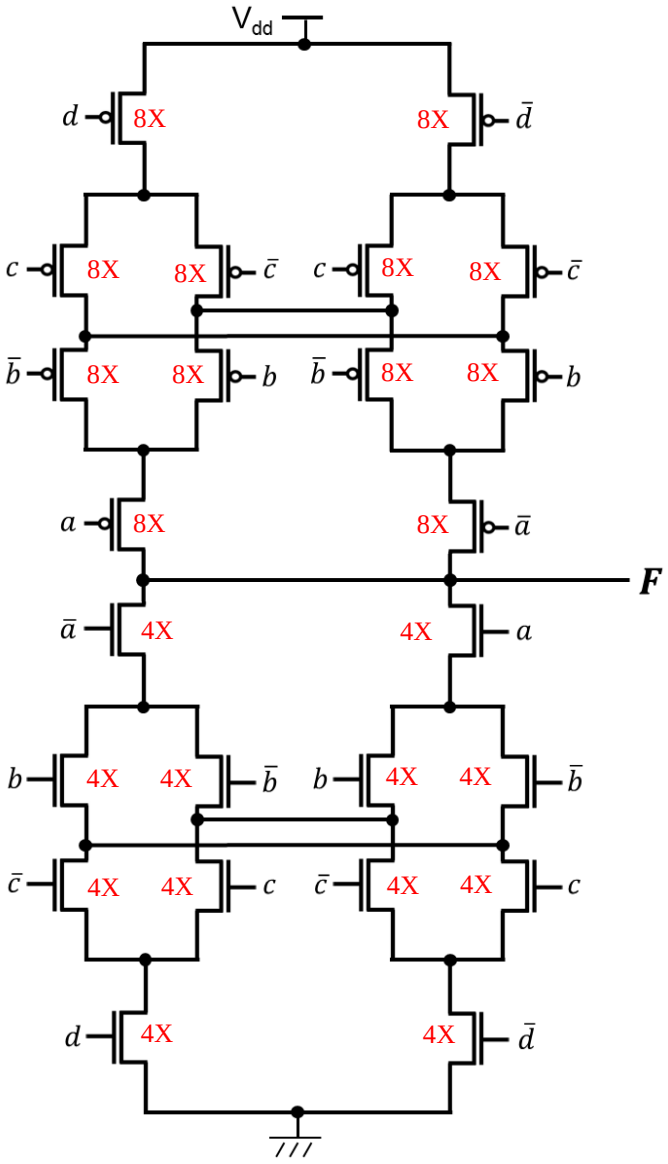
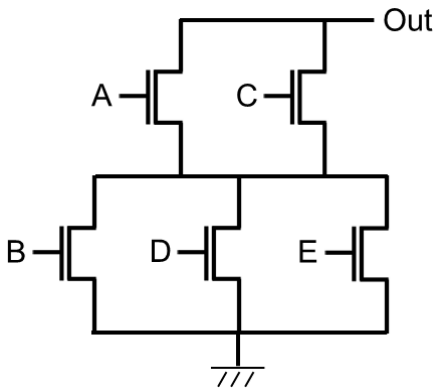
Homework Assignment 6
(Due Mar. 4th at the beginning of the class)

(1) **[Transistor Sizing, 5 points]** $\mu_n = 2\mu_p$. R is the resistance of a 1X NMOS transistors. The target time constant is RC where C is the load capacitance. Size the transistors in the following figure to satisfy the target time constant (try not to over-optimize them).



Each path goes through four TRs, so the size of each NMOS is 4X and the size of each PMOS is 8X.

(2) **[Transistor Sizing, 5 points]** R is the resistance of a 1X NMOS transistor. The target time constant is RC where C is the load capacitance. Size the transistors in the following pull-down network to satisfy the time constant. However, **<u>minimize</u>** the total width of the transistors.

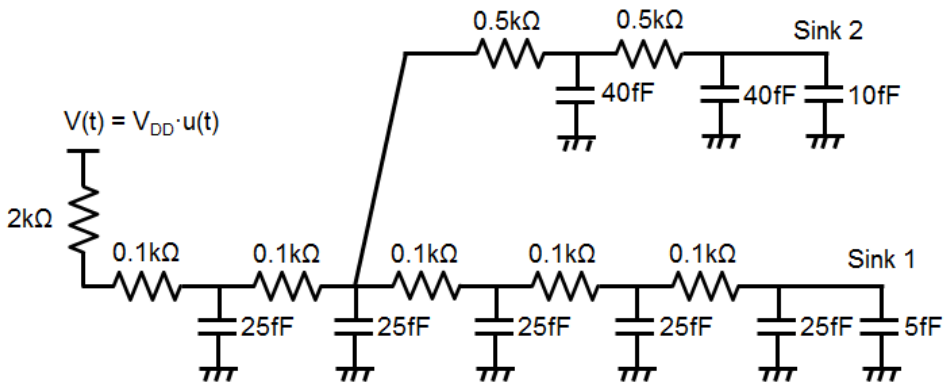


A and C are connected in parallel, so let's upsize them to aX. B, D, and E are connected in parallel, so let's upsize them to bX. Then the total width is $W = 2a + 3b$. Constraint:

$\frac{R}{a} + \frac{R}{b} = R \Rightarrow b = \frac{a}{a-1} \Rightarrow W = 2a + \frac{3a}{a-1} \Rightarrow W' = 2 + \frac{3(a-1)-3a}{(a-1)^2} = \frac{2(a-1)^2-3}{(a-1)^2} = 0$

$2a^2 - 4a - 1 = 0 \Rightarrow a = 1 + \frac{\sqrt{6}}{2},\ b = \frac{\sqrt{6}}{3}$

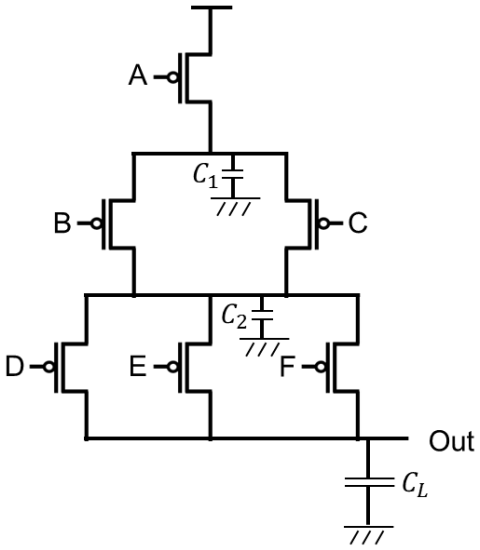
(3) **[Elmore Delay, 5 points]** Compute Elmore delay at Sink 1 and Sink 2 in the following figure.



Sink 1: $\tau = 0.1k * (25f + 5f) + 0.1k * (25f + 25f + 5f) + 0.1k * (25f + 25f + 25f + 5f) + 0.1k * (25f + 25f + 25f + 25f + 5f + 40f + 40f + 10f) + 0.1k * (the\ whole\ downstream\ cap = 220f) + 2k * 220f = 3ps + 5.5ps + 8ps + 19.5ps + 22ps + 440ps = 498ps$

Sink 2: $\tau = 0.5k * (40f + 10f) + 0.5k * (40f + 40f + 10f) + 0.1k * (25f + 25f + 25f + 25f + 5f + 40f + 40f + 10f) + 0.1k * 220f + 2k * 220f = 25ps + 45ps + 19.5ps + 22ps + 440ps = 551.5ps$

(4) **[Switching Characteristics, 5 points]** Compute the rise time at the output node in the following figure. C_1 and C_2 are parasitic capacitances at the internal nodes. The input switches from (A, B, C, D, E, F) = (1, 0, 0, 0 0, 0) to (0, 0, 0, 1, 0, 1). Use R_X (where X=A, B, C, D, E, F) for the resistance of transistor X.



When (A, B, C, D, E, F)=(1, 0, 0, 0, 0, 0), C_1 and C_2 (and C_L) are fully discharged. When (A, B, C, D, E, F) switch to (0, 0, 0, 1, 0, 1), only A, B, C, and E are turned on. Thus,

$$\tau = R_E \cdot C_L + \frac{R_B \cdot R_C}{R_B + R_C} \cdot (C_2 + C_L) + R_A \cdot (C_1 + C_2 + C_L)$$

delay=2.2τ