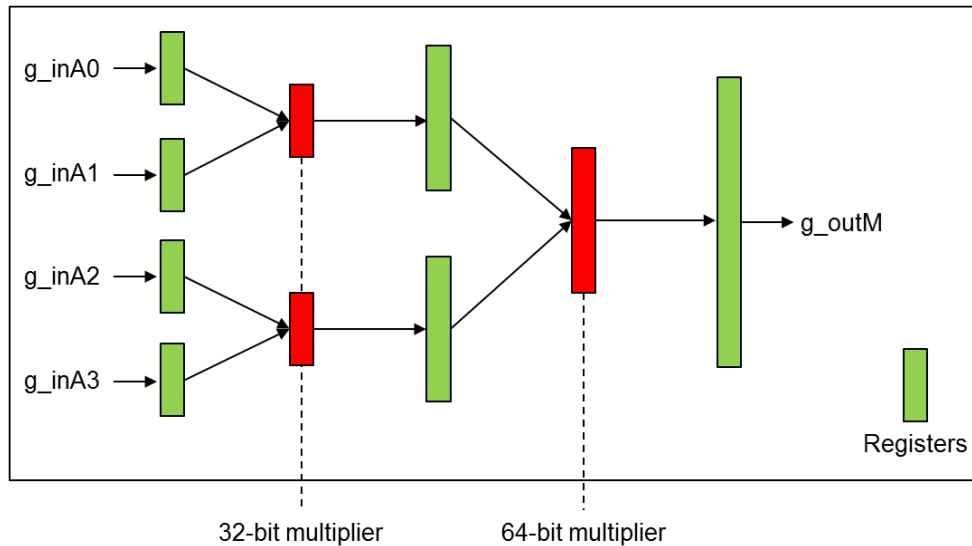


## Lab 3

**(Due Apr. 17<sup>th</sup> at the beginning of the class)**

Design a four-input 32-bit pipelined multiplier. The following shows a block diagram for the multiplier:



The following file also contains all the files required for lab3.

- <http://eecs.wsu.edu/~ee434/Labs/lab3.tar.gz>
- pmul32\_4\_fm.globals, .view, .v, .sdc, .ctstch (use metalfill.cmd for metal fill insertion)

### Spec

- Initial core utilization: 0.5

### Submit

- Layout snapshots at each stage
  - After P/G network design
  - After placement (turn off the visibility of all metal layers)
  - After routing (turn off the visibility of all metal layers)
  - After routing (turn on the visibility of all metal layers)
  - After fill insertion (turn on the visibility of all metal layers)
- A snapshot of the clock tree after CTS

- Timing report (use “timeDesign”) at each stage
  - After placement
  - After pre-CTS optimization
  - After CTS
  - After post-CTS optimization
  - After routing
  - After post-routing optimization
  - After fill insertion