EE434
ASIC & Digital Systems

Design Compiler

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Overview

- Synthesis is converting given HDL source codes into a netlist.

- Synthesis software
  - Synopsys Design Compiler
  - Cadence RTL Compiler

How to Run Synopsys Design Compiler (DC)

- Run the following command:

  > source /net/ictools/sh/synopsys.sh

- Run DC:

  > design_vision

Library Files

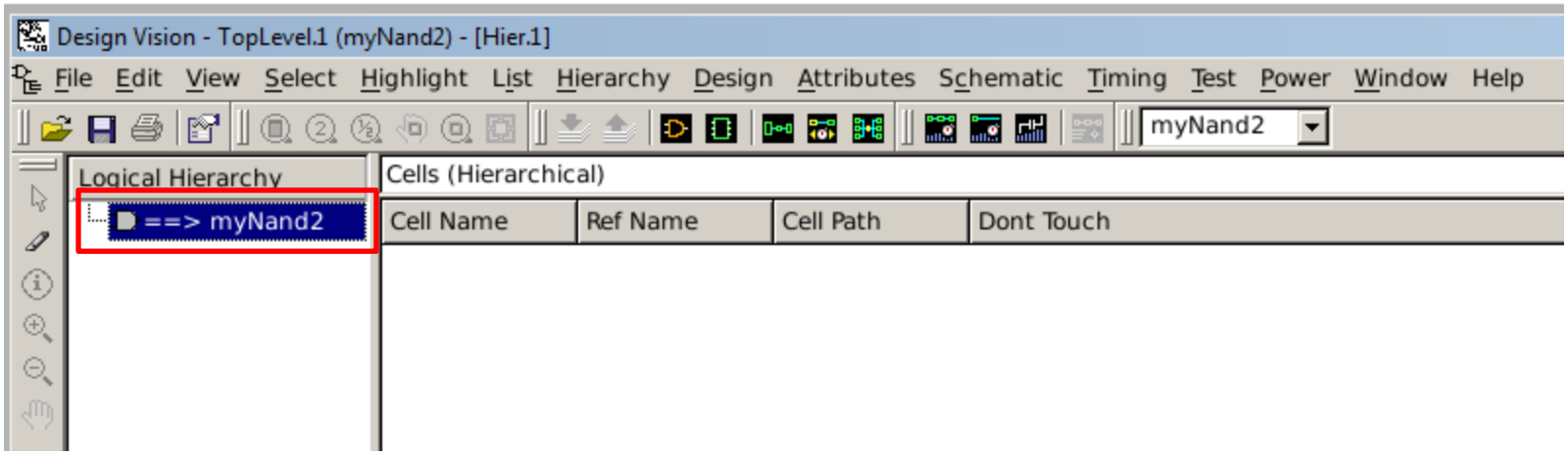
- Download the following file into your working directory:
  - http://eecs.wsu.edu/~ee434/Labs/tut-dc.zip
- Unzip it
  - unzip tut-dc.zip
- You will see the following files:
  - NangateOpenCellLibrary_typical.db
    - Standard cell library for synthesis
  - NangateOpenCellLibrary.v
    - Verilog source code for standard cells
  - and some more files

Run DC

- Run DC.
  > design_vision
- Set libraries.
  > set link_library {NangateOpenCellLibrary_typical.db}
  > set target_library {NangateOpenCellLibrary_typical.db}
- Read source files.
  > read_file –format vhdl {nand2.vhd}
  – (Make sure that there is no error)
- Set the top-level module you want to synthesize.
  > current_design myNand2
- Compile.
  > compile –exact_map –map_effort high

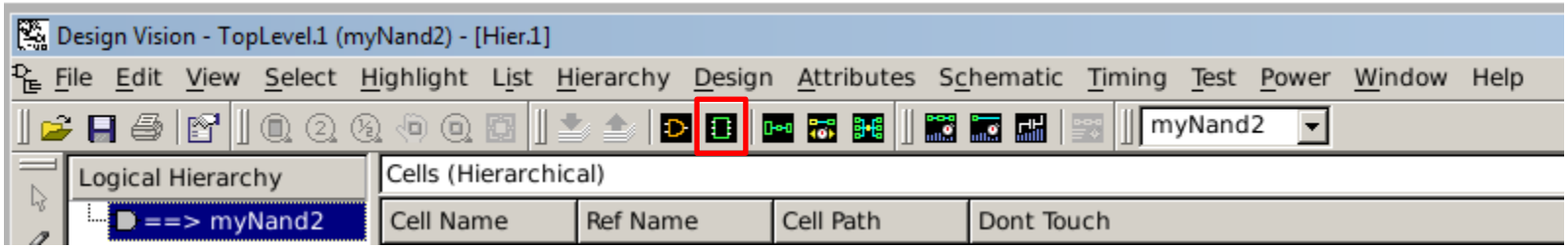
Compile

- “Compile” actually synthesizes a given circuit and generates a netlist.
- It also optimizes your netlist during synthesis.
- Once it’s done, let’s visualize the netlist in DC.
- Click myNand2 in the “Logical Hierarchy” window.



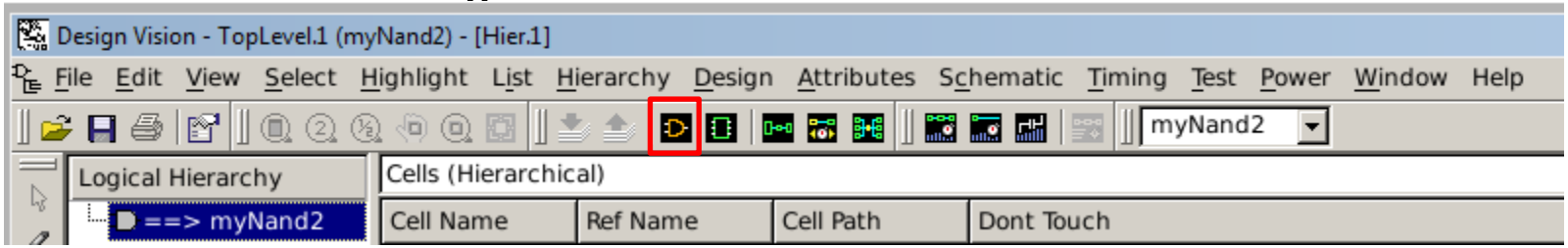
Schematic Viewer

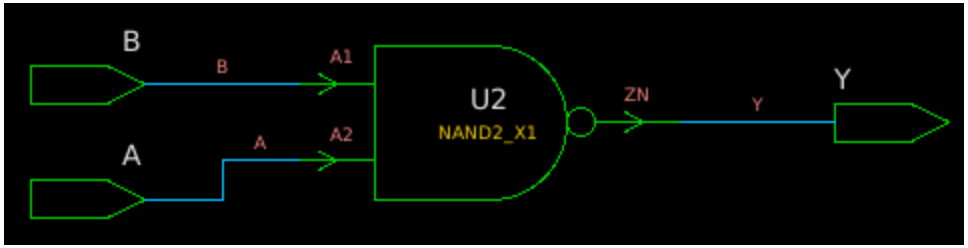
- You can see the I/O ports or the schematic (netlist) of the module.
- Click the following button to see the I/O ports of the module (symbol view).



Schematic Viewer

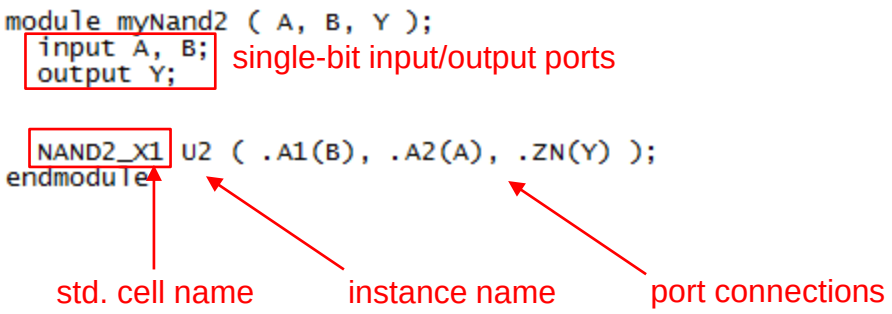
- Close the symbol view.
- Click the following button to see the schematic of the module.





Save

- Save the synthesized netlist.
  > write –format verilog -output nand2_syn.v
  – (Notice that we are using Verilog for the synthesized netlist.)
- Open the synthesized netlist in a text editor and see how it looks like.

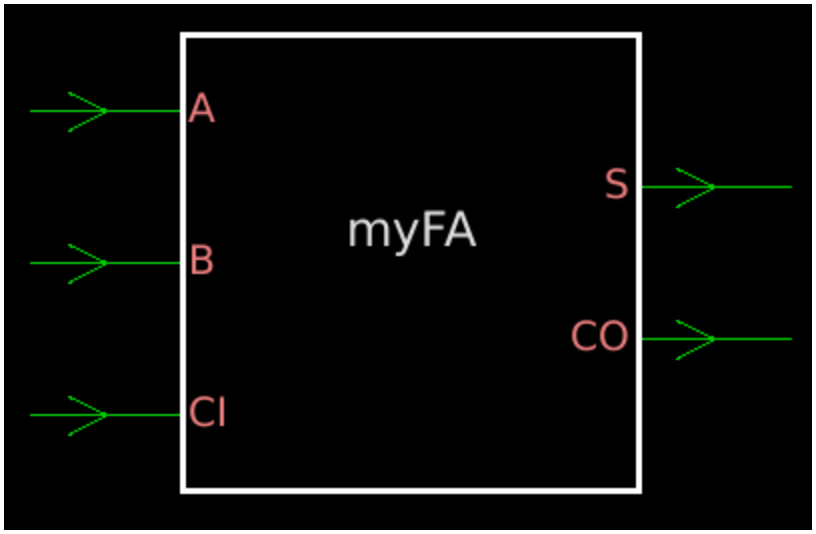


- Exit
  > exit (or quit)

Example

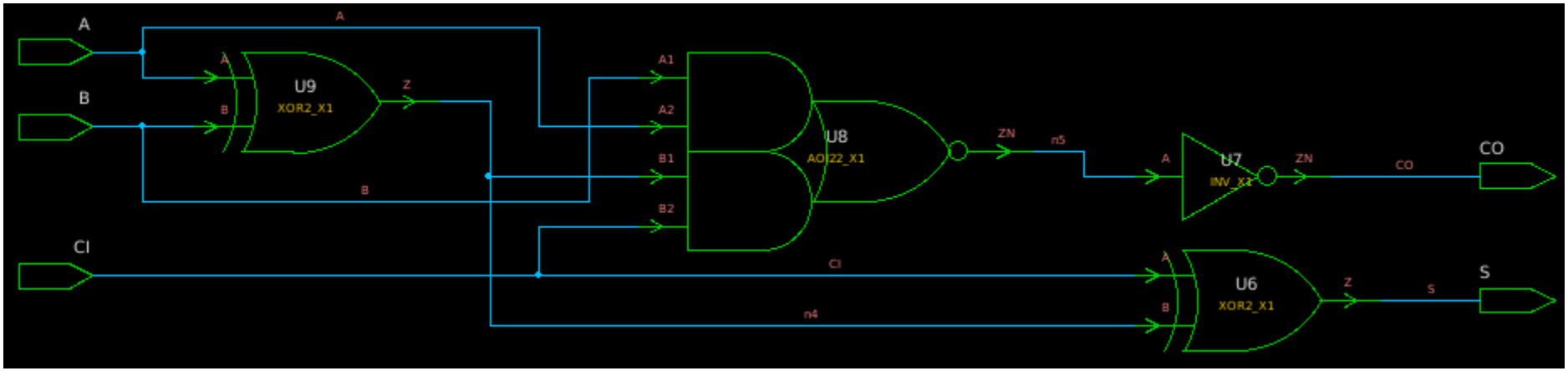
- Repeat the same synthesis procedure to synthesize a full adder.
- Use “fa.vhd”.
- The top-level module name is “myFA”.
- Use “compile –exact_map -map_effort low”

- Symbol



Example

- Schematic



Simulation

- Save the synthesized netlist.

  > write –format verilog –output fa_syn.v

- Exit.

- Now, we will simulate the synthesized full adder using ModelSim.

Simulation

- Run ModelSim (you need to source /net/ictools/sh/mentor-modelsim.sh).
- Create a new project and add existing files.
  - NangateOpenCellLibrary.v
  - fa_syn.v
  - fa_sim.vhd
- Compile all of them.
- Run until 12ns.

Simulation

- Results