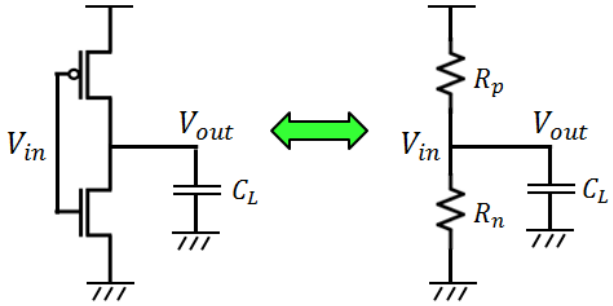
Homework Assignment 2

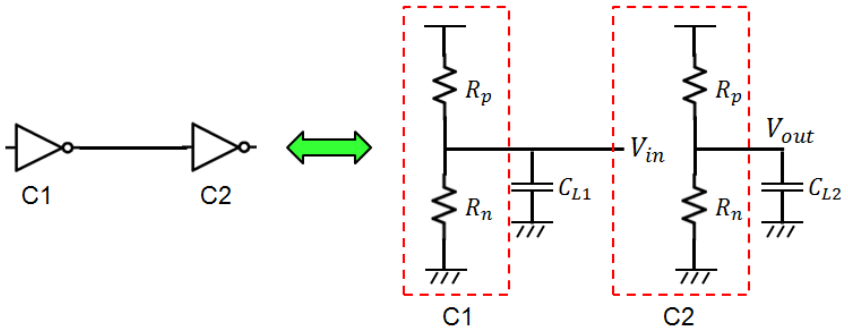
(Due Feb. 13th at the beginning of the class)

1. [Modeling, **10 points**] We can model an inverter by a simple RC circuit as follows. ($R_{OFF,p} = \infty, R_{OFF,n} = \infty, R_{ON,p} = 1k\Omega, R_{ON,n} = 1k\Omega, C_L = 20fF$) When $V_{in} = 0$ and V_{DD}, $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_{ON,p} \cdot C_L}}\right)$ and $V_{DD} \cdot e^{-\frac{t}{R_{ON,n} \cdot C_L}}$, respectively. Find t satisfying $V_{out}(t) = 0.1V_{DD}, 0.2V_{DD}, \dots, 0.9V_{DD}$ when $V_{in} = 0$. Find t satisfying $V_{out}(t) = 0.9V_{DD}, 0.8V_{DD}, \dots, 0.1V_{DD}$ when $V_{in} = V_{DD}$. Sketch $V_{out}(t)$ for $V_{in} = 0$ and V_{DD} by interpolating and extrapolating the points.



2. [Modeling, **10 points**] We upsize the NMOS and PMOS transistors in Problem 1 by 4x. Upsizing them increases the widths of the transistors, so their resistances go down. Now, $R_{ON,p} = 0.25k\Omega, R_{ON,n} = 0.25k\Omega$. Repeat Problem 1 with these new resistances. Do you see the impact of upsizing?

3. [Modeling, **10 points**] If you upsize a gate, the gate becomes faster (i.e., stronger). However, there are two side effects. First, it occupies more silicon area. Second, its input capacitance goes up, which has negative impact on the gate driving this gate. For example, in the following figure, upsizing C2 increases C_{L1}, so C1 needs more time to charge C_{L1}. This problem simulates the side effect of transistor sizing. Repeat Problem 1 using the following parameters. ($R_{OFF,p} = \infty, R_{OFF,n} = \infty, R_{ON,p} = 1k\Omega, R_{ON,n} = 1k\Omega, C_L = 40fF$)



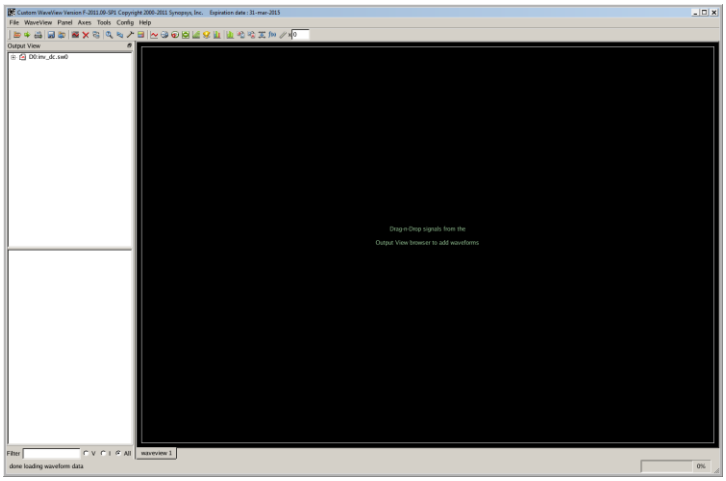
4. [Static CMOS Circuit, **5 points**] Draw a transistor-level schematic for the following function. (Primary inputs are A, B, and C). Simplify the logic before you draw the schematic so that you can use NAND2 and NOR2 gates.

$$\boldsymbol{F = A \cdot B \cdot \overline{C}}$$

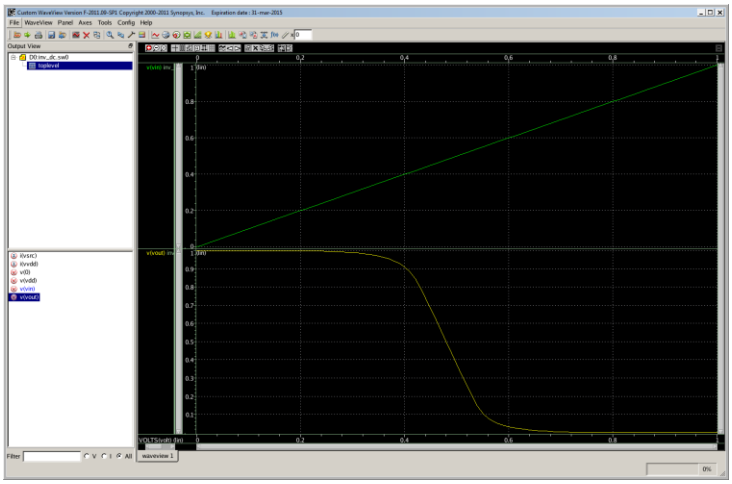
5. [Transistor Sizing, **5 points**] We are supposed to design the following function. $\mu_n = 2\mu_p$, C_L is the output load, and R_n is the resistance of a 1x NMOS. Design the gate and size the transistors so that both the NMOS and PMOS time constants become $R_n C_L$.

$$\boldsymbol{F = \overline{A \cdot B + C \cdot D \cdot E}}$$

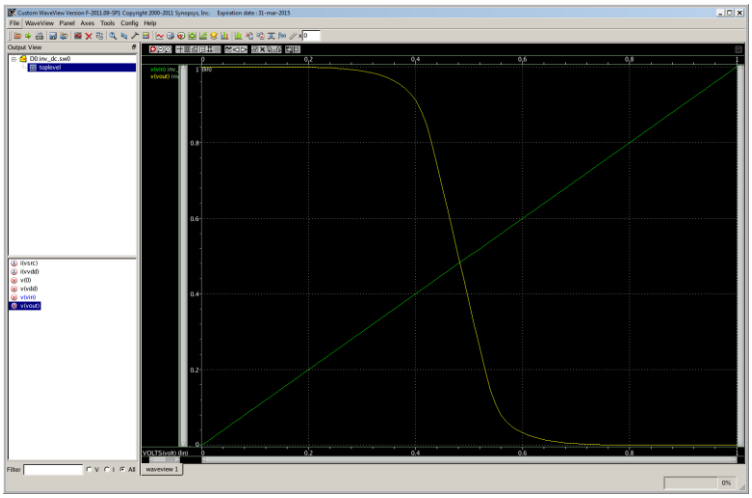
6. [DC Analysis, **10 points**]
    1) Create a work directory.
        - mkdir ee434_hw02
        - cd ee434_hw02
    2) Download the following file into your directory.
        - wget http://www.eecs.wsu.edu/~ee434/Homework/hw02.tar.gz
    3) Unzip it.
        - tar xvzf hw02.tar.gz
    4) Source the .sh file (Note: You should source this file. Not the .sh file in hw01)
        - source synopsys.sh
    5) Open inv_dc.sp and read the comments. This file is for DC analysis of a CMOS inverter.
    6) Run HSpice to simulate the given netlist.
        - hspice inv_dc.sp
    7) Run WaveView to visualize the output.
        - wv inv_dc.sw0
    8) You will see the following window.



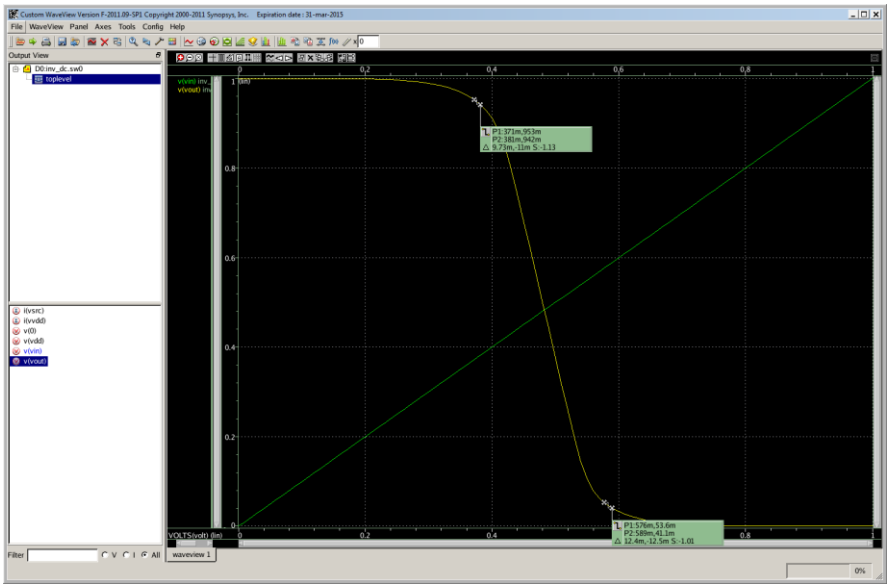
9) Expand “D0:inv_dc.sw0” and click “toplevel”. In the voltage and current list, double click “v(vin)” and “v(vout)”. You will see the following window.



10) Merge them into a single plot by clicking/dragging/merging “v(vout)” into “v(vin)”. Now you will see the following DC plot.



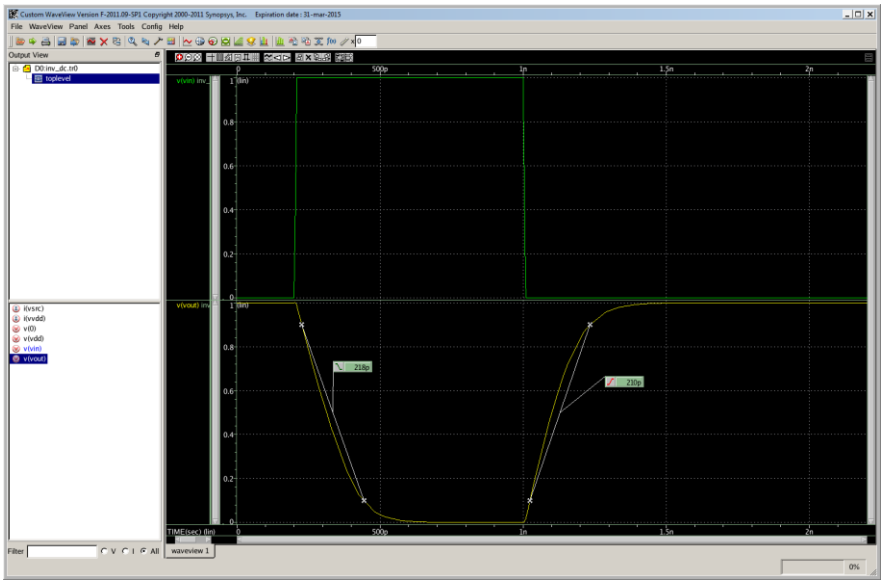
11) Click the "measurement tool" icon (the ruler in the icon list). Choose "Difference" and click "OK". Select the measurement box created in the main window, drag, and release it at the first point you want to measure. Then, drag the box again and release it at the second point. Then, the box will show the slope between the two points. Find the two points at which the slope becomes -1.



12) In my window, $V_{IL} = 375mV, V_{IH} = 580mV, V_{OL} = 45mV, and\ V_{OH} = 950mV$.
13) $NM_L = 375mV - 45mV = 330mV, NM_H = 950mV - 580mV = 370mV$.
14) [**Submit**] Use ($W_n = 90nm, W_p = 70nm$) and run DC sweep analysis again. Compute NM_L and NM_H.
15) [**Submit**] Use ($W_n = 45nm, W_p = 140nm$) and run DC sweep analysis again. Compute NM_L and NM_H.
16) [**Submit**] Use ($W_n = 90nm, W_p = 140nm$) and run DC sweep analysis again. Compute NM_L and NM_H.

7. [Switching Characteristics, **10 points**]
   1) Use ($W_n = 45nm, W_p = 70nm$). Run HSpice.
   2) Run WaveView to visualize the transient output.
      - wv inv_dc.tr0
   3) Double click "v(vin)" and "v(vout)" to visualize the input and the output. Do not merge them.
   4) Click the measurement tool and choose "Rise/Fall Time". Make sure the "Rise/Fall Margin Threshold" is set to 90.00% and 10.00%. Move the measurement box to the bottom plot so that you can measure the fall time.

Measure the rise time in the same way. In my simulation, I got fall time=218ps and rise time=210p.



5) [**Submit**]Use ($W_n = 90nm, W_p = 140nm$) and run HSpice again. Obtain t_f and t_r.
6) [**Submit**]Use ($W_n = 135nm, W_p = 210nm$) and run HSpice again. Obtain t_f and t_r.
7) [**Submit**]Use ($W_n = 180nm, W_p = 280nm$) and run HSpice again. Obtain t_f and t_r.
8) [**Submit**]Use ($W_n = 450nm, W_p = 700nm$) and run HSpice again. Obtain t_f and t_r.