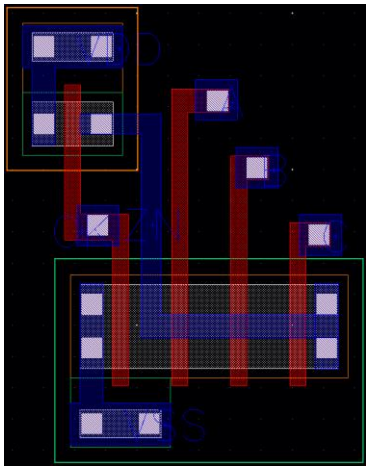
Homework Assignment 4

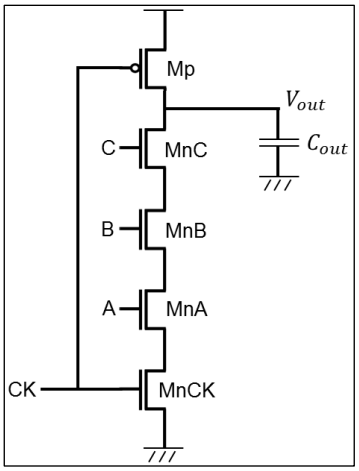
(Due Mar. 4th at the beginning of the class)

0. Preparation for homework 4
    - Download the following file into your working directory.
        - wget http://www.eecs.wsu.edu/~ee434/Homework/hw04.tar.gz
    - Unzip it.
        - tar xvzf hw04.tar.gz
    - Source synopsys.sh
        - source synopsys.sh

1. [Pseudo-nMOS, **20 points**]
    - Design a pseudo-nMOS inverter for the following design spec:
        - Simulate the inverter with the following load cap and input signal
            - Load cap: 10fF
            - The fall & rise transition time of the input signal: 10ps
        - Spec
            - Rise time < 100ps
            - Fall time < 100ps
            - V_{OL} < 100mV
            - V_{OH} > 900mV
            - NM_L > 150mV
            - NM_H > 300mV
    - [**Submit**]
        - The size of the NMOS and PMOS transistors
        - Rise time, fall time
        - V_{IH}, V_{IL}, V_{OH}, V_{OL}, NM_L, NM_H
        - Average power for falling and rising transitions

2. [Dynamic CMOS, **20 points**]
    - We design a three-input NAND gate using the dynamic CMOS design style.
    - Open myNAND3_pex.cdl and see the netlist of the NAND gate. I drew a layout for the NAND gate and extracted parasitic RC. myNAND3_pex.cdl includes all the parasitic RC.
    - Open myNAND3_simul.sp and see the netlist. It is used to simulate the NAND gate.
    - The followings show the layout and schematic of the NAND gate.





- Add four signal waveforms (CK, A, B, C) to simulate charge sharing.
    - Load cap: 10fF
    - CK: $V_{DD} \rightarrow 0 \rightarrow V_{DD}$
    - When CK is V_{DD} (before it goes down to 0), set A, B, and C to V_{DD} so that it can fully discharge the output capacitor and all the parasitic capacitors.
    - Then, set A, B, and C to 0 before CK goes to 0.
    - Then, CK goes to 0 and the gate will charge the output capacitor.
    - Then, CK goes to V_{DD}.
    - Then, set C to V_{DD} so that charge sharing can happen between the output capacitor and the parasitic capacitor between MnC and MnB.
    - Perform the same simulation, but set both B and C to V_{DD} so that charge sharing can happen among the output capacitor, the parasitic capacitors between MnC and MnB and between MnB and MnA.
- [**Submit**]
    - Vout when only C is set to V_{DD} for C_{out} =10fF, 9fF, …, 1fF.
- [**Submit**]
    - Vout when both C and B are set to V_{DD} for C_{out} =10fF, 9fF, …, 1fF.

3. [Synthesis, **20 points**]
    - In this problem, we will synthesize a netlist for a few gates.
    - Make sure you have the following files in your working directory.
        - NangateOpenCellLibrary_typical_ecsm.db
        - nand8.v
    - Source synopsys.sh.
    - Run Design Compiler (DC).
        - design_vision –no_gui
    - In DC, run the following commands.
        - set link_library {NangateOpenCellLibrary_typical_ecsm.db}

    - set target_library {NangateOpenCellLibrary_typical_ecsm.db}
    - read_file -format verilog {nand8.v}
    - compile -exact_map
    - write -format verilog -output nand8_mapped.v
    - exit
- The two “set” statements set up target libraries.
- “read_file” reads HDL source codes.
- “compile” compiles (synthesizes) the source codes.
- “write” writes the synthesized code into the file specified after “-output”.
- Open “nand8.v” and see the function of the module.
- Open “nand8_mapped.v” and see the function of the module. Are they equal?
- [**Submit**] Draw a schematic for the netlist of “nand8_mapped.v”.
- Implement a 20-input nand gate by modifying “nand8.v” and synthesize it.
- [**Submit**] Draw a schematic for the netlist of the synthesized 20-input nand gate.
- Implement a full adder and synthesize it.
    - Primary inputs: A, B, CI
    - Primary outputs: S, CO
    - Use ^, &&, and || for XOR, logical AND, and logical OR operations in Verilog.
    - Use parentheses to prioritize the operations.
    - Use two assignments, one for S and the other for CO.
- [**Submit**] Draw a schematic for the netlist of the synthesized full adder.