Lab 1
(Due Mar. 23rd at the beginning of the class)

Draw a layout for a full adder (primary inputs: A, B, CI, primary outputs: S, CO, do not use M2~M10). Run DRC, LVS, and xRC. Run HSpice and compare the two netlists (with and without parasitic RC). You need to create proper input waveforms to test the worst-case rising and falling times.

Tips

- Draw a schematic first and properly size the transistors.
- Refer to the full-adder layout shown in the class slide.

Submit

- Layout snapshot
- Transistor-level schematic (with the size of each transistor)
- DRC report (Do not print out on paper. Copy and paste it in your report and send it to me by email).
- LVS report
- xRC report
- Input and output waveforms (use WaveView).
- The worst-case rising and falling times.