EE 434
ASIC & Digital Systems

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Course Website

- http://eecs.wsu.edu/~ee434

Themes

- Study how to design, analyze, and test a complex application-specific integrated circuit (ASIC).

- At the end of this semester, you will be able to
  - Understand how a VLSI chip works.
  - Design complex digital VLSI circuits and systems both manually and automatically.
  - Understand basic theories behind VLSI.
  - Analyze VLSI circuits and systems.
  - Test VLSI circuits and systems.

Course Materials

- We will use both bottom-up and top-down approaches.
- We will not discuss much about device physics.
- We will learn more about transistor-, gate-, circuit-, and system-level issues.
- We will study
  - Transistor characteristics (logical, physical, DC, AC, power, etc.)
  - Standard cell design, analysis, and optimization
  - Interconnects (resistance, capacitance, delay, power, etc.)
  - Timing analysis
  - HDL (Verilog/VHDL)
  - Memory
  - Full-custom layout, computer-aided design (CAD)
  - Test

Schedule

- Week 1 (1/9, 11, 13): Introduction to VLSI, CMOS transistors
- Week 2 (1/20): CMOS transistors, gates
- Week 3 (1/23, 25, 27): CMOS inverter, combinational logic
- Week 4 (1/30, 2/1, 3): CMOS sequential logic, design styles
- Week 5 (2/6, 8, 10): Characterization and performance estimation
- Week 6 (2/13, 15, 17): Characterization and performance estimation
- Week 7 (2/22, 24): Midterm 1, layout, simulation, optimization
- Week 8 (2/27, 3/1, 3): Interconnects, timing analysis
- Week 9 (3/6, 8, 10): HDL
- Week 10 (3/13 – 17): Spring break
- Week 11 (3/20, 22, 24): HDL, Memory
- Week 12 (3/27, 29, 31): Synthesis, physical design, arithmetic units
- Week 13 (4/3, 5, 7): Midterm 2, test
- Week 14 (4/10, 12, 14): Test
- Week 15 (4/17, 19, 21): Test
- Week 16 (4/24, 26, 28): Test
- Final: May 4 (8am – 10am)

References

- FPGA-BASED System Design by Wayne Wolf, Prentice Hall, 2004, ISBN 0-13-142461-0
- Analysis and Design of Digital Integrated Circuits by Hodges, Jackson, and Saleh, 3/E, 2003, McGraw Hill, ISBN 0072283653
- CMOS VLSI Design: A Circuits and Systems Perspective by Weste and Harris, 4/E, 2010, Addison-Wesley, ISBN 0321547748
- Digital Integrated Circuits by Rabaey, Chandrakasan, and Nikolic, 2E, 2003, Prentice Hall, ISBN 0130909963
- Introduction to VLSI Circuits and Systems by Uyemura, 1E, 2001, Wiley, ISBN 0471127043
- CMOS Logic Circuit Design by Uyemura, 1999, Springer, ISBN 0387781641
- Application-Specific Integrated Circuits by Smith, 1997, Addison-Wesley, ISBN 0201500221
- Digital Systems Testing and Testable Design, 1990, IEEE Press, ISBN 0-7803-1062-4
- Extra reading materials will be supplied in the class.

Assignments

- Homework
  - Due dates will be mentioned when handed out.
  - Late submission penalty
    - -5% per day
    - -80% max.

- Lab and HW are very important parts of this course.
  - Lab assignments will involve HDL coding.
    - No worries! You will learn HDL step by step.
  - You will be supposed to use several commercial design&analysis tools.
    - No worries! Detailed tutorials will be provided.
  - EME 205 is the lab for this course.
  - You will be allowed to work anytime in the lab.
  - TA will be available only in his fixed office hours.

Labs

- HDL coding and simulation
- Std. cell layout, DRC, LVS, PEX, and simulation
- VLSI design and analysis
- SPICE simulation, analysis, and optimization

ASIC

- **A**pplication **S**pecific **I**ntegrated **C**ircuits

- Integrated circuits
  - All components are integrated on a single semiconductor substrate.

- Metrics and design specification
  - Area
  - Speed
  - Power (dynamic, leakage)

VLSI

- **V**ery-**L**arge-**S**cale **I**ntegration

- What does it integrate?
  - Transistors
  - Interconnects

- History

Name	Signification	Year	# Transistors
SSI	Small-Scale Integration	1964	1 – 10
MSI	Medium-Scale Integration	1968	10 – 500
LSI	Large-Scale Integration	1971	500 – 20K
VLSI	Very-Large-Scale Integration	1980	20K – 1M
ULSI	Ultra-Large-Scale Integration	1984	> 1M

Source: https://en.wikipedia.org/wiki/Integrated_circuit#SSI.2C_MSI_and_LSI

ASIC Design Process

System specifications

64-bit integer multiplier
Freq (1GHz) / Area (0.1mm^2) / Power (1mW)

High-level model

Hardware description language (HDL)
such as VHDL and Verilog

```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  reg [63:0] int_stage1;
  reg [63:0] int_stage2;

  always @ (posedge clk)
  begin
    ...
  end

endmodule
```

Verification

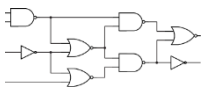
Logic synthesis

Output: netlist

```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  NAND2_X1 ( .A(in_1[0]), .B(in_2[0]), .Z(n1) );
  FA_X1 ( .A(in_1[0]), .B(in_2[0]), .CI(1'b0), .S(n2), .CO(n3) );
  ...

endmodule
```



Verification

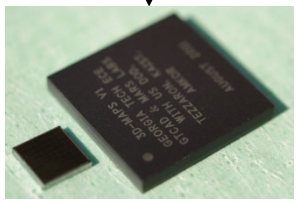
Circuit design

Verification

Physical design

Verification

Manufacturing



Testing

Working chip

VLSI Design Styles

	Full-Custom Design	Fully-Automated
Design	Manual	Automatic
Transistors	Manually drawn	Standard-cell-based
Placement & Routing (P&R)	Manual	Automatic
Development time	Several months	A few days – weeks