

# Physical Structure of CMOS Integrated Circuits

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# References

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- John P. Uyemura, “Introduction to VLSI Circuits and Systems,” 2002.
  - Chapter 3

# Goal

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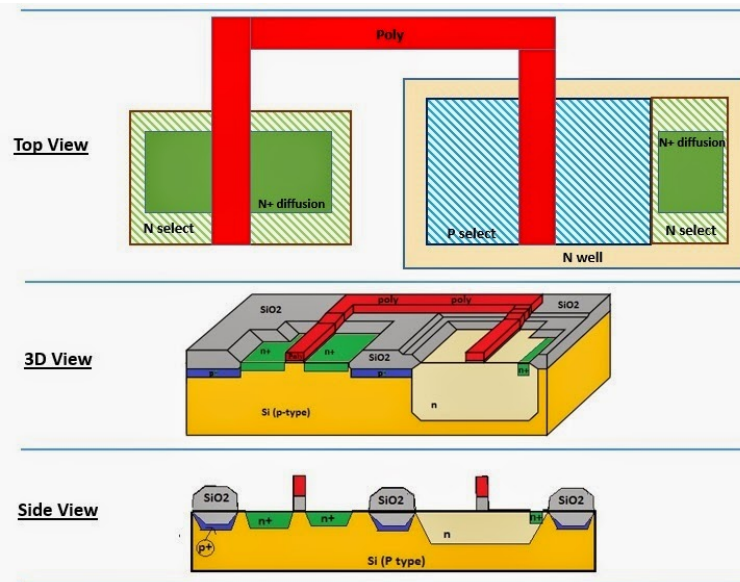
- Understand the physical structure of CMOS integrated circuits (ICs)

# Logical vs. Physical

- Logical structure



- Physical structure



Source: <http://www.vlsi-expert.com/2014/11/cmos-layout-design.html>

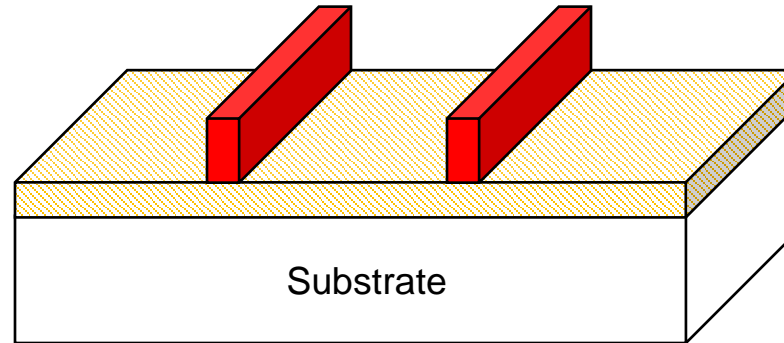
# Integrated Circuit Layers

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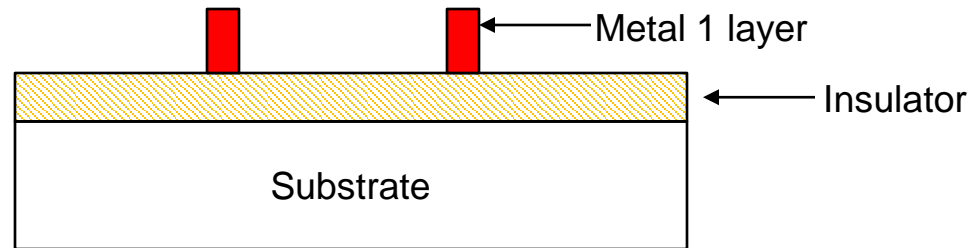
- Semiconductor
  - Transistors (active elements)
- Conductor
  - Metal (interconnect)
    - Wire
    - Via
- Insulator
  - Separators

# Integrated Circuit Layers

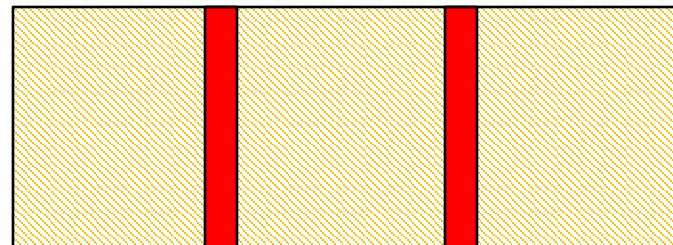
- Silicon substrate, insulator, and two wires (3D view)



- Side view

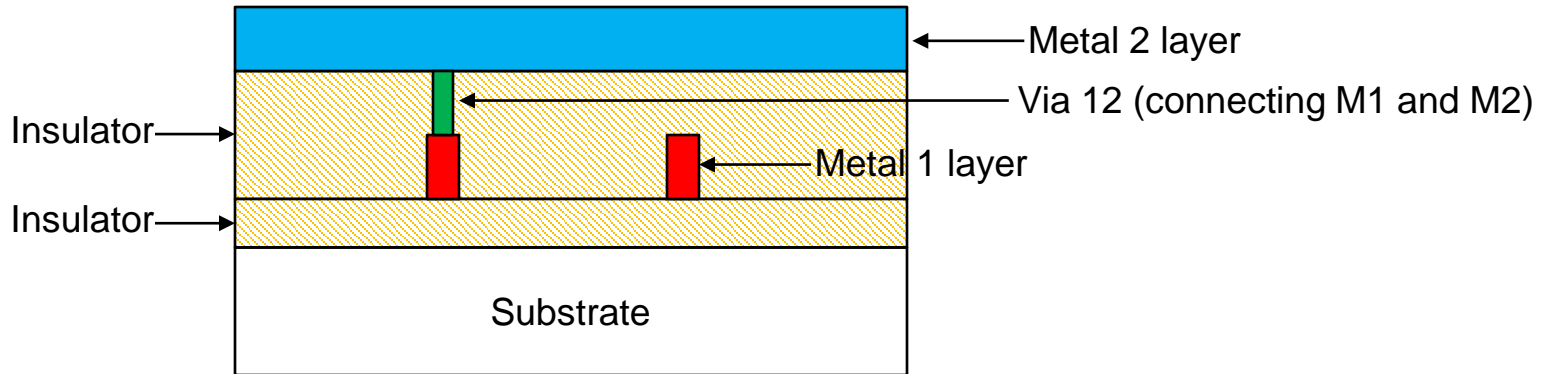


- Top view

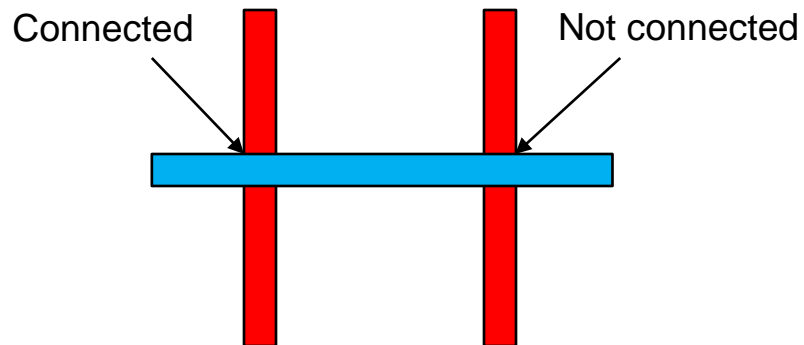


# Integrated Circuit Layers

- Two metal layers separated by insulator (side view)



- Top view

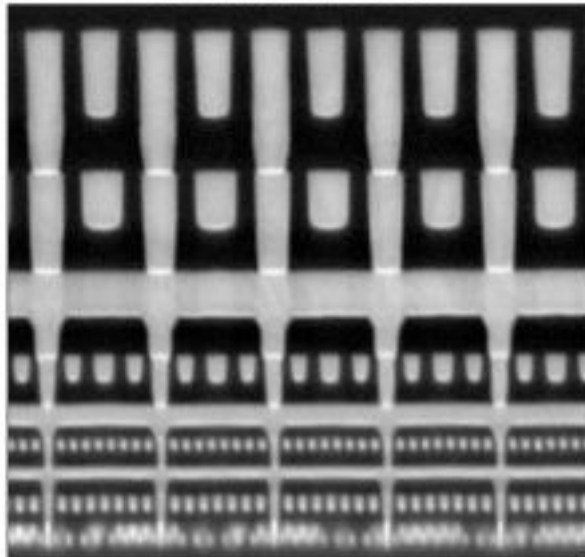


# Integrated Circuit Layers

Embargo until 8-11-14, 9 am PDT

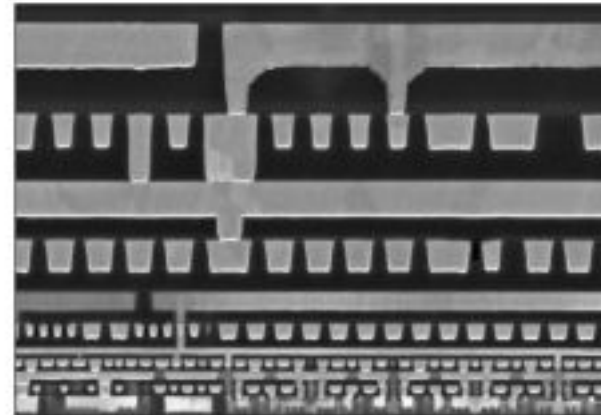
## Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process



52 nm (0.65x) minimum pitch

*52 nm Interconnect Pitch Provides  
Better-than-normal Interconnect Scaling*



# Integrated Circuit Layers

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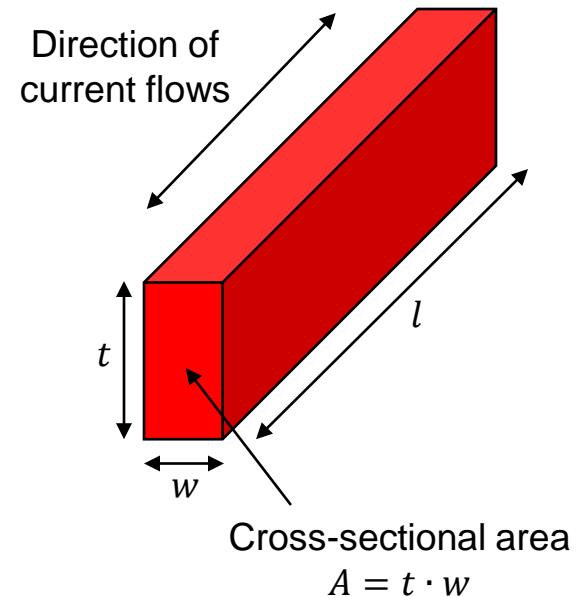
- Signal transfer speed is affected by the interconnect resistance and capacitance.
  - Resistance  $\uparrow \Rightarrow$  Signal delay  $\uparrow$
  - Capacitance  $\uparrow \Rightarrow$  Signal delay  $\uparrow$

# Integrated Circuit Layers

- Resistance

- $R = \rho \frac{l}{A} = \frac{\rho}{t} \cdot \frac{l}{w} = R_S \cdot \frac{l}{w}$

- $R_S$ : sheet resistance (constant)
    - $\rho$ : resistivity ( $= \frac{1}{\sigma}$ ,  $\sigma$ : conductivity)
      - Material property (constant)
      - Unit:  $\Omega \cdot m$
    - $t$ : thickness (constant)
    - $w$ : width (variable)
    - $l$ : length (variable)



- Example

- $\rho: 17.1n\Omega \cdot m, t: 0.13\mu m, w: 65nm, l: 1000\mu m$

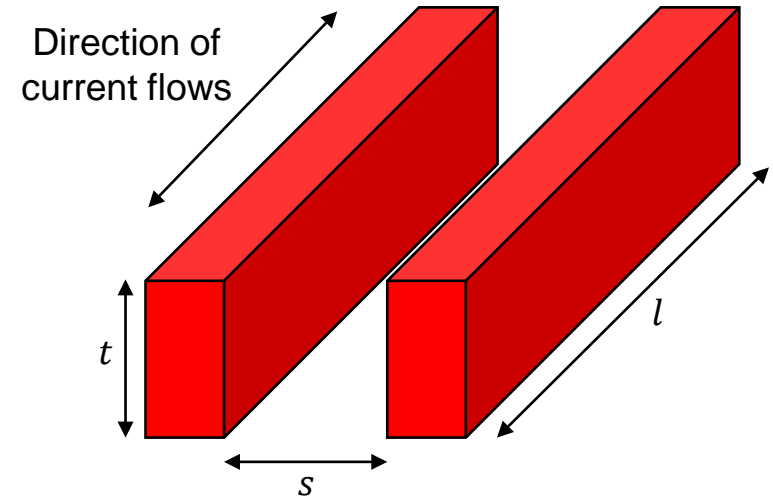
- $R = (17.1 \cdot 10^{-9}\Omega \cdot m) \cdot \frac{1000 \cdot 10^{-6}m}{(0.13 \cdot 10^{-6}m) \cdot (65 \cdot 10^{-9}m)} = 2023\Omega$

# Integrated Circuit Layers

- Capacitance

- $C = \epsilon \frac{t \cdot l}{s}$

- $\epsilon$ : permittivity
      - Material property (constant)
      - Unit: F/m
    - $s$ : distance between two conductors



- Example

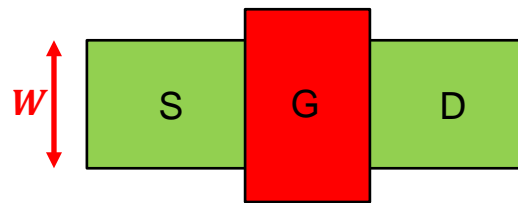
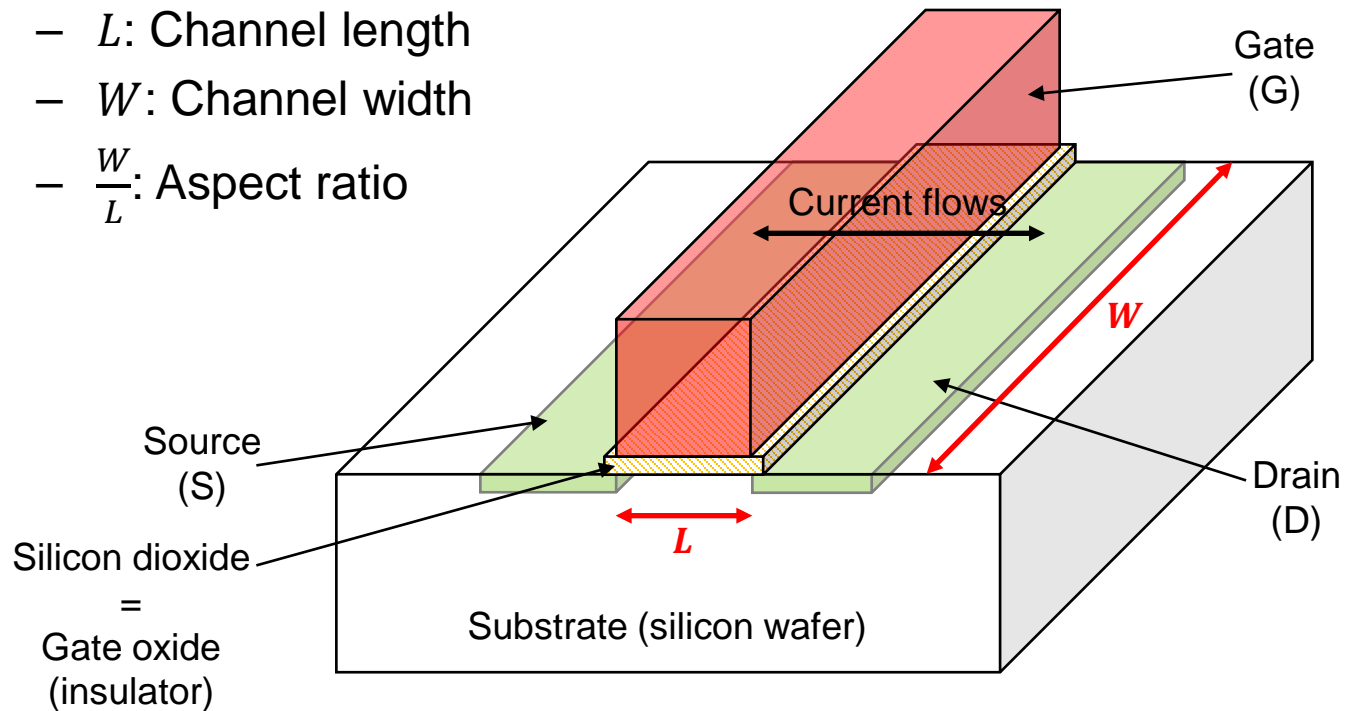
- $\epsilon: 1.8 \cdot 10^{-11} F/m, t: 0.13 \mu m, s: 65 nm, l: 1000 \mu m$

- $C = (1.8 \cdot 10^{-11} F/m) \cdot \frac{(0.13 \cdot 10^{-6} m) \cdot (1000 \cdot 10^{-6} m)}{65 \cdot 10^{-9} m} = 3.6 \cdot 10^{-14} F = 36 fF$

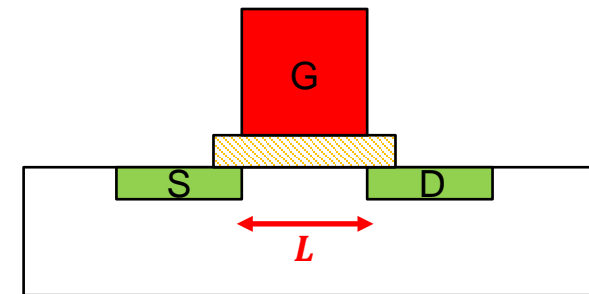
# MOSFETs – Physical Shape

- What a MOSFET looks like at the physical level

- $L$ : Channel length
- $W$ : Channel width
- $\frac{W}{L}$ : Aspect ratio



Top view



Side view

# MOSFETs – Device Physics

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- Atomic density of a silicon crystal
  - $N_{Si} \approx 5 \times 10^{22}$
- Intrinsic carrier density
  - # free electrons (due to thermal excitations)
  - $n_i \approx 1.45 \times 10^{10} / \text{cm}^3$  (at room temperature)
- Mass action law when no current flows in pure silicon
  - $n = p = n_i$
  - $np = n_i^2$ 
    - $n$ : # free electrons
    - $p$ : # free holes

# MOSFETs – Device Physics

- Doping
  - Add impurity atoms (dopants) to enhance # electrons or # holes.
  - n-type material: if more electrons are added (donors).
    - $N_d$ : # donors ( $10^{16} \sim 10^{19} / \text{cm}^3$ )
    - # free electrons (majority carriers):  $n_n \approx N_d / \text{cm}^3$
    - # holes (minority carriers):  $p_n \approx \frac{n_i^2}{N_d} / \text{cm}^3$
    - $n_n \gg p_n$
  - p-type material: if more holes are added (acceptors).
    - $N_a$ : # acceptors ( $10^{14} \sim 10^{19} / \text{cm}^3$ )
    - # holes (majority carriers):  $p_p \approx N_a / \text{cm}^3$
    - # free electrons (minority carriers):  $n_p \approx \frac{n_i^2}{N_a} / \text{cm}^3$
    - $p_p \gg n_p$

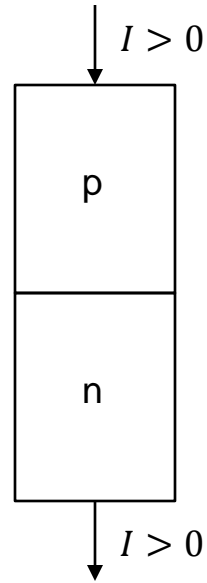
# MOSFETs – Device Physics

- Conductivity
  - $\sigma = q(\mu_n \cdot n + \mu_p \cdot p)$ 
    - $q$ : The charge of an electron ( $-1.602 \cdot 10^{-19}$ )
    - $\mu_n$ : Electron mobility ( $1360 \text{cm}^2 / \text{V} \cdot \text{s}$ )
    - $\mu_p$ : Hole mobility ( $480 \text{cm}^2 / \text{V} \cdot \text{s}$ )
- Intrinsic silicon
  - $\sigma \approx 4.27 \cdot 10^{-6}$
  - $\rho \approx 2.34 \cdot 10^5$
- Quartz glass (insulator)
  - $\rho \approx 10^{12}$
- Mobility
  - $\mu_n > \mu_p$
- Impurity scattering
  - Adding a large number of impurity atoms reduces the mobility.

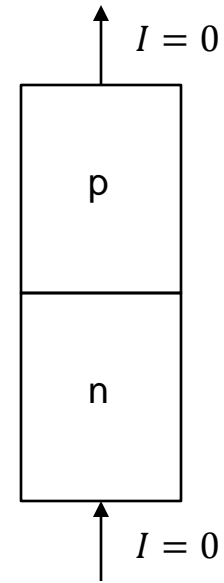
# PN Junction



pn junction



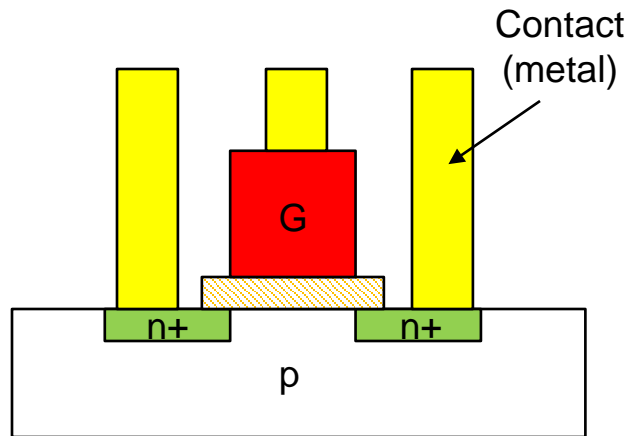
Forward current



Reverse blocking

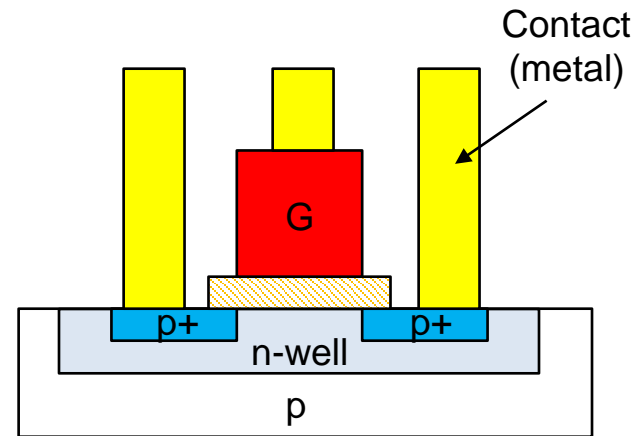


# MOSFETs



nFET

n+: heavily doped with donors



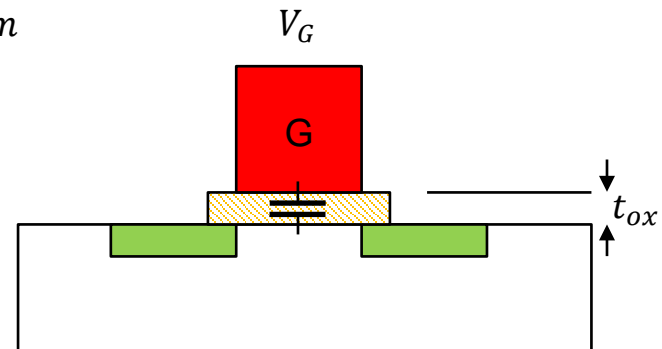
pFET

p+: heavily doped with acceptors

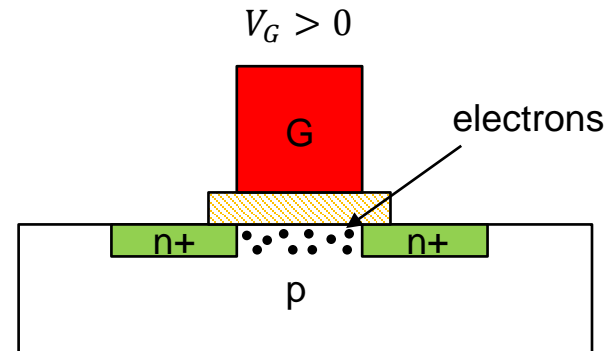
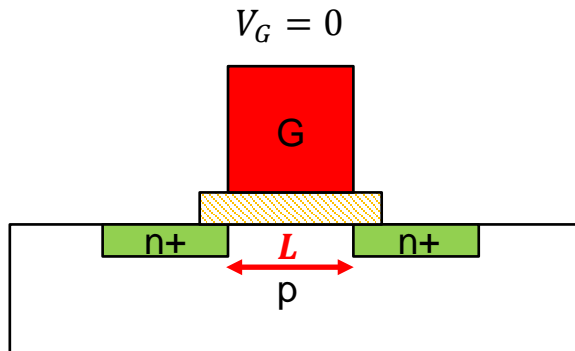
\* Contacts are used to connect source/drain/gate to metal 1.

# MOSFETs – Device Physics

- $t_{ox}$ : oxide thickness
  - Typically a few nm
- Gate material
  - Polysilicon (called poly)
  - Metal
- Oxide capacitance (Gate(M) – Insulator(O) – Semiconductor(S))
  - $C_G = c_{ox} \cdot A_G$ 
    - $c_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ : unit gate capacitance
      - $\epsilon_{ox} \approx 3.9\epsilon_0 = 3.9 \cdot 8.854 \cdot 10^{-12} F/m$
    - $A_G$ : gate area ( $= L \cdot W$ )
  - Example
    - $t_{ox} = 8nm, L = 45nm, W = 70nm$ 
      - $C_G \approx 0.013fF$



# MOSFETs – Device Physics (nFET)



- Current

- Channel charge:  $Q_c = -C_G(V_G - V_{Tn})$ 
  - No charge forms until  $V_G$  reaches  $V_{Tn}$ .

- Current flowing the channel:  $I = \frac{|Q_c|}{\tau_t}$

- $\tau_t = \frac{L}{v}$ : channel transit time (the average time needed for an electron to move from S to D).
- $v = \mu_n \cdot E = \mu_n \cdot \frac{V_{DS}}{L}$

- $I \approx \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_G - V_{Tn}) \cdot V_{DS}$

# MOSFETs – Device Physics (nFET)

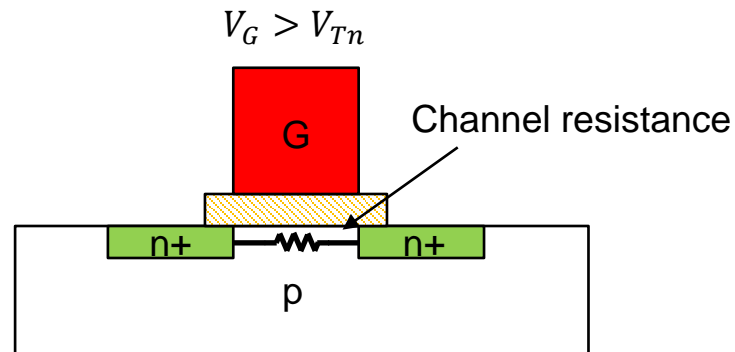
- Current through the channel

- $I \approx \mu_n \cdot c_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_G - V_{Tn}) \cdot V_{DS} = \beta_n \cdot (V_G - V_{Tn}) \cdot V_{DS}$

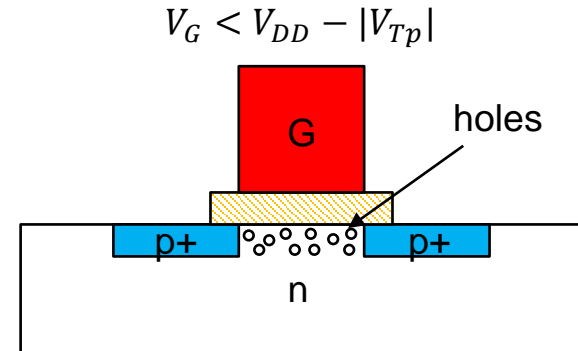
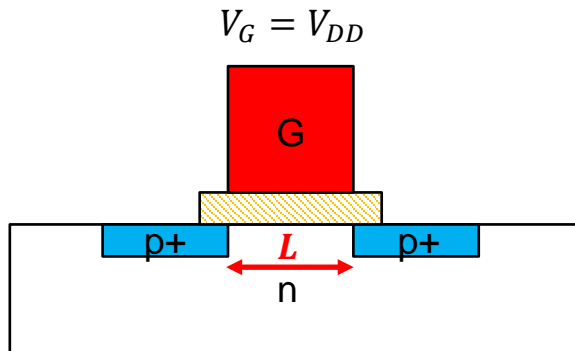
- $\beta_n = \mu_n \cdot c_{ox} \cdot \left(\frac{W}{L}\right)$ : device transconductance
    - $\mu_n, c_{ox}, V_{Tn}$ : constants
    - $L, W$ : variables (designers can decide)
    - $V_G, V_{DS}$ : variables (but either 0 or  $V_{DD}$ )

- Channel resistance

- $R_n = \frac{V_{DS}}{I} = \frac{1}{\beta_n \cdot (V_G - V_{Tn})}$



# MOSFETs – Device Physics (pFET)



- Current

- Channel charge:  $Q_c = C_G(V_G - |V_{Tp}|)$

- No charge forms until  $V_G$  reaches  $V_{DD} - |V_{Tp}|$ .

- Current flowing the channel:  $I = \frac{|Q_c|}{\tau_t}$

- $\tau_t = \frac{L}{v}$ : channel transit time (the average time needed for an electron to move from D to S).

- $v = \mu_p \cdot E = \mu_p \cdot \frac{V_{SD}}{L}$

- $I \approx \mu_p \cdot c_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_G - |V_{Tp}|) \cdot V_{SD}$

# MOSFETs – Device Physics

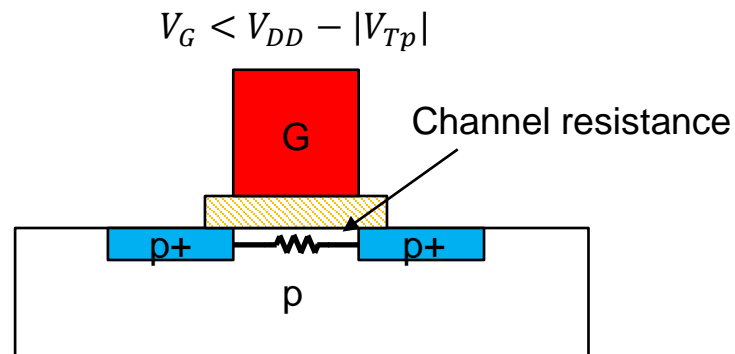
- Current through the channel

- $I \approx \mu_p \cdot c_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_G - |V_{Tp}|) \cdot V_{SD} = \beta_p \cdot (V_G - |V_{Tp}|) \cdot V_{SD}$

- $\beta_p = \mu_p \cdot c_{ox} \cdot \left(\frac{W}{L}\right)$ : device transconductance
    - $\mu_p, c_{ox}, V_{Tp}$ : constants
    - $L, W$ : variables (designers can decide)
    - $V_G, V_{SD}$ : variables (but either 0 or  $V_{DD}$ )

- Channel resistance

- $R_p = \frac{V_{SD}}{I} = \frac{1}{\beta_p \cdot (V_G - |V_{Tp}|)}$



# MOSFETs – Device Physics

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- Charging the gate requires current flows.
  - $i = C_G \frac{dV_G}{dt}$
  - The transistor itself has a signal delay.
  - If  $C_G$  is large, the delay goes up.
- Energy
  - $E = \int P dt = \int (V \cdot I) dt = \int \left( V \cdot C \frac{dV}{dt} \right) dt = \frac{1}{2} CV^2$
  - $E = \frac{1}{2} C_G V_{DD}^2$
  - Driving a transistor consumes energy (power dissipation).