EE434
ASIC & Digital Systems

Built-In Self Test (BIST)

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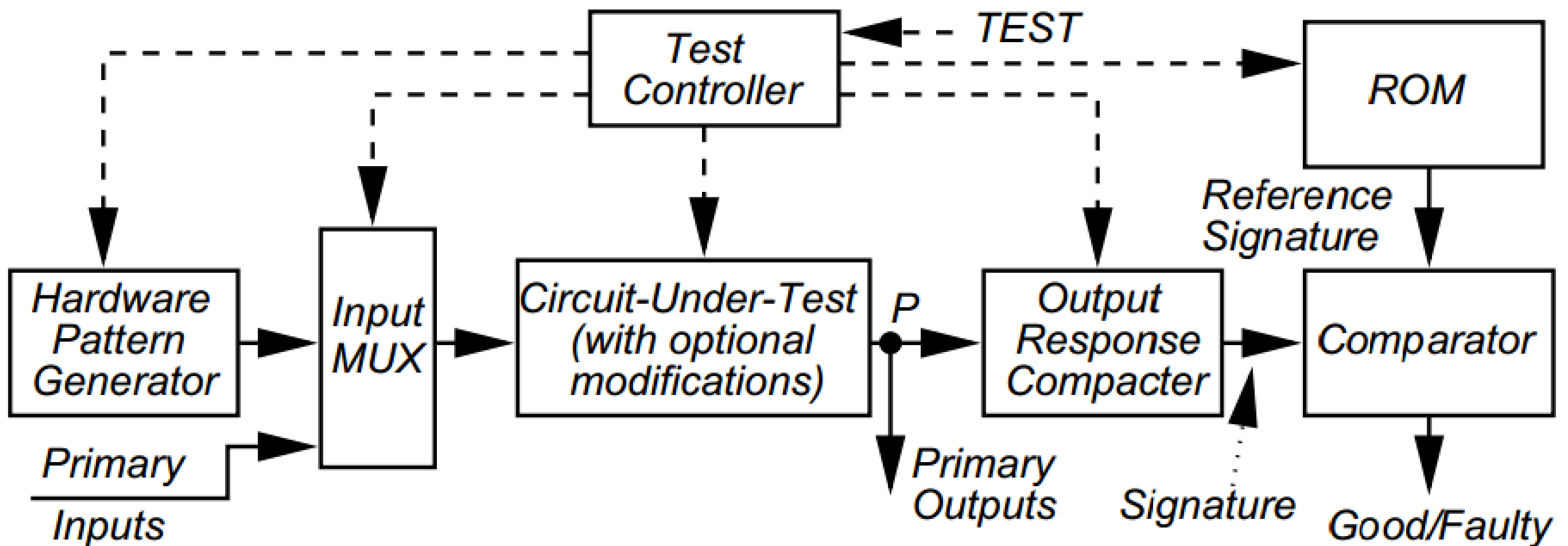
Dae Hyun Kim
daehyun@eecs.wsu.edu

BIST

- Test itself.
- On-line BIST
  - Test occurs during normal functional operating conditions.
  - Concurrent on-line BIST: testing + normal operation
  - Non-concurrent on-line BIST: testing is performed when a system is in idle mode.
- Off-line BIST

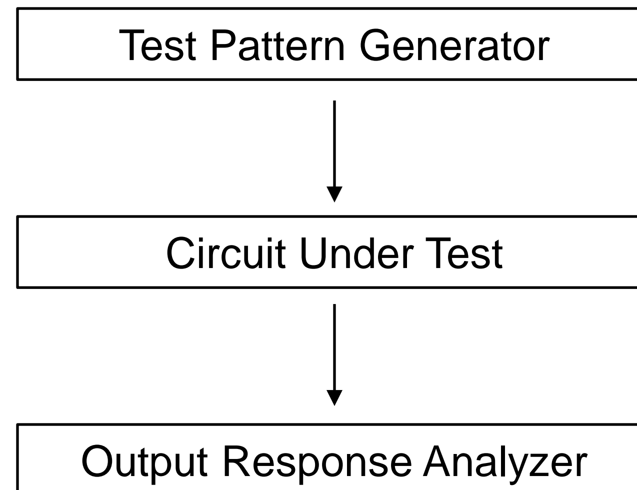
Test Pattern Generation for BIST

- BIST process



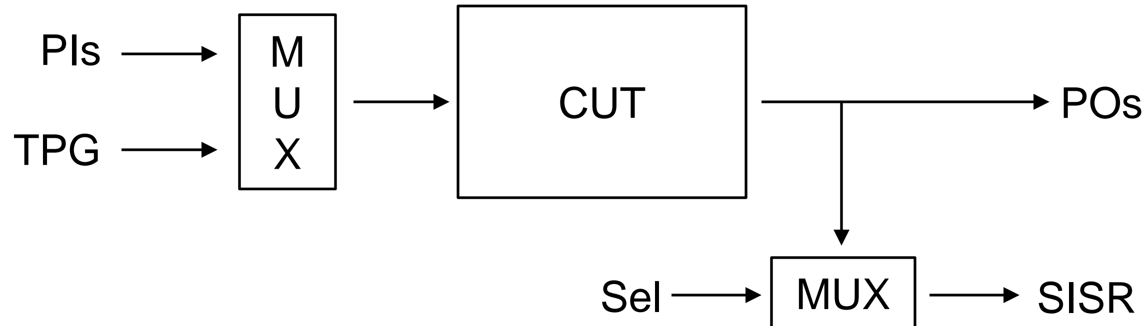
Basic BIST Architecture

- Test pattern generator
  - Exhaustive
  - Pseudoexhaustive
  - Pseudorandom
  - ...
- Test response compression
  - One’s count
  - Transition count
  - Parity checking
  - ...



BIST Architectures

- Centralized and Separate Board-Level BIST Architecture



PIs: Primary Inputs

TPG: Test Pattern Generator

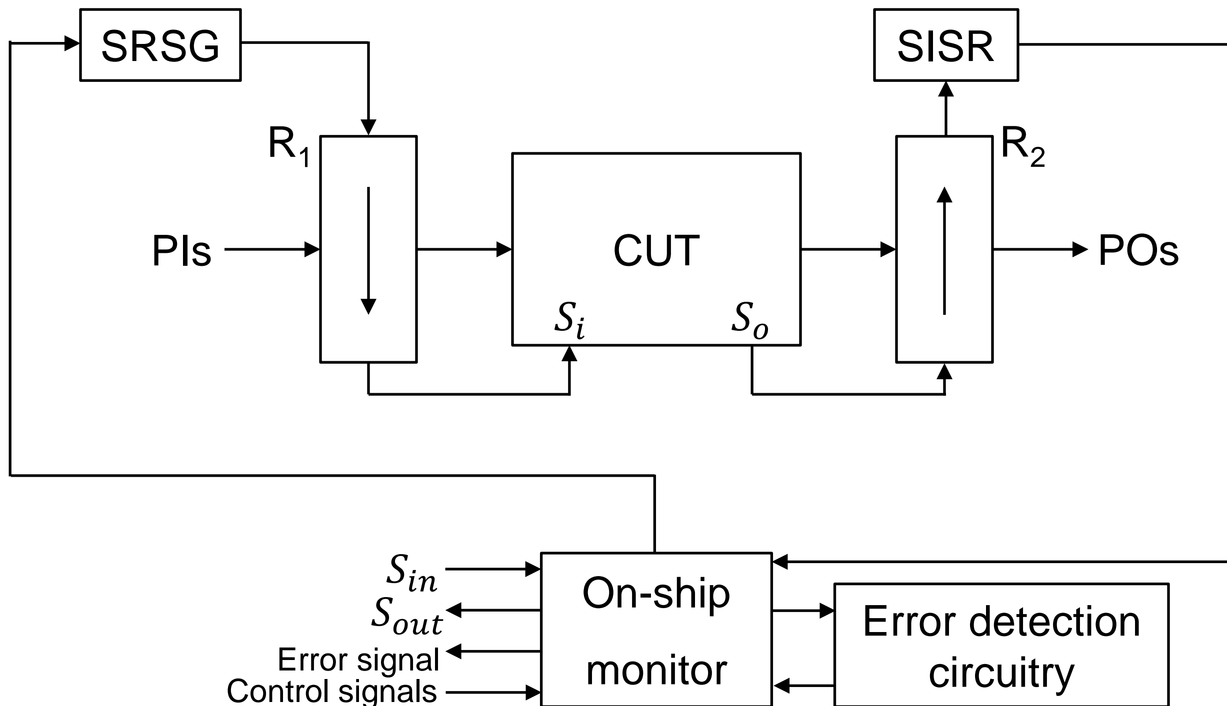
CUT: Circuit Under Test

POs: Primary Outputs

SISR: Single-Input Signature Register

BIST Architectures

- LSSD On-Chip Self-Test



SRSG: Shift Register Signal Generator

BIST Architectures

1. Initialize.
   – The scan path is loaded with seed data via S_{in}.

2. Activate self-test mode.
   – Disable system clocks on R_1 and R_2.
   – Enable LFSR (Linear Feedback Shift Register) operation.

3. Execute self-test operation.
   – Load the scan path with a pseudorandom test pattern.
   – Activate the system clocks for one cycle.

4. Check result.
   – Compare the final value with the known good signature.