EE434
ASIC & Digital Systems

VHDL
Behavioral Modeling

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Signals

- A signal is a local net.
- Signal assignment is done by

```
a <= b
```

- This is executed whenever b changes.
  - b is in the sensitivity list of this statement.
- What if the new value is equal to the old one?
  - Nothing happens.
- What if the new value is different from the old one?
  - An event is scheduled for signal a.

Signal Assignment

- Signal assignment with delay

```
a <= b  AFTER  10  NS;
```

  - This is only for simulation.

- A two-input NAND gate with a delay value

```
ARCHITECTURE  vand2_arch  OF  vand2  IS
BEGIN
   z <= (a AND b) AFTER 10 NS;
END  vand2_arch;
```

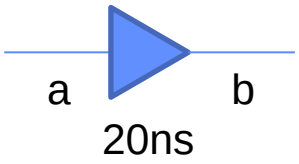
Signal Assignment

- A four-input MUX with a delay value

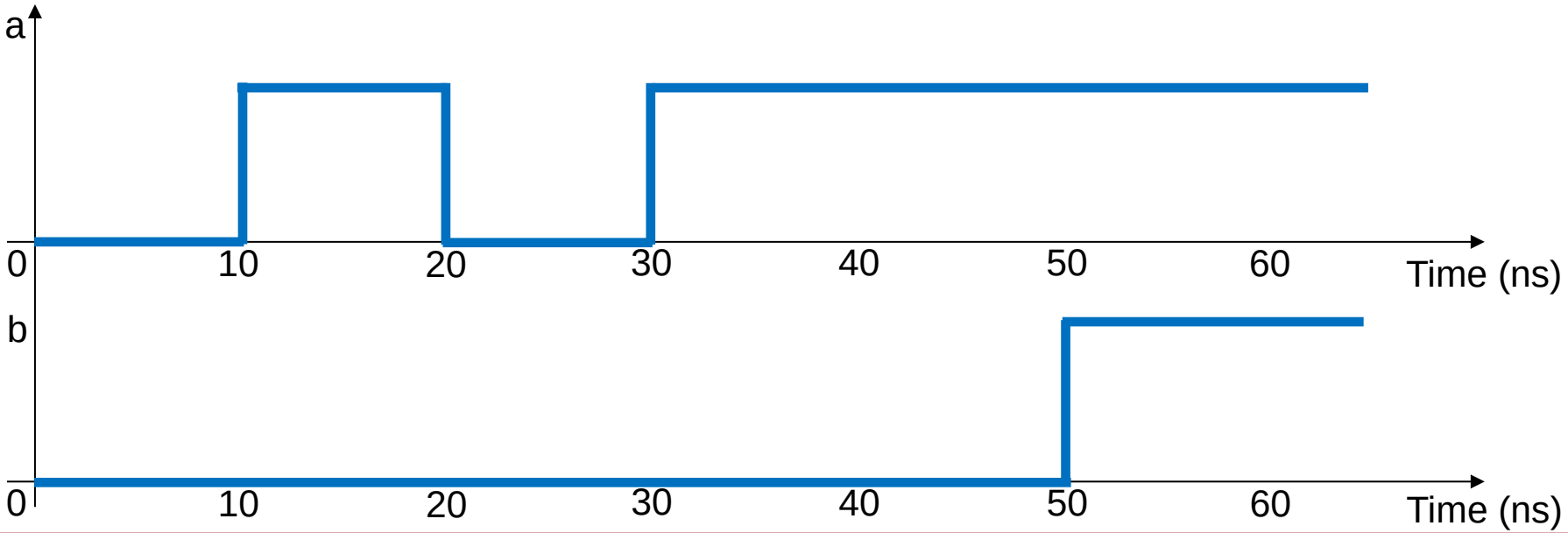
```
ARCHITECTURE vmux4_arch OF vmux4 IS
BEGIN
   z <= in0 AFTER 5 NS WHEN s1 = '0' AND s0 = '0'
     ELSE in1 AFTER 7 NS WHEN s1 = '0' AND s0 = '1'
     ELSE in2 AFTER 6 NS WHEN s1 = '1' AND s0 = '0'
     ELSE in3 AFTER 4 NS;
END vmux4;
```

Delay Model

- Inertial delay model
  - Glitches shorter than the delay value are ignored.




```
a <= b AFTER 20 NS;
```



Delay Model

- Transport delay model
  - All changes are propagated.


```
a <= TRANSPORT b AFTER 20 NS;
```