Homework Assignment 3
(Due Feb. 10th at the beginning of the class)

***** Submission policy: Please zip all your result files into a single file and send it to daehyun@eecs.wsu.edu. The file name should be *lastname_firststname*.zip (or .tar.gz or .tar …)

Go to the course website, click "Labs", and open "tutorial-design_compiler.pdf" and complete it (but you don't need to submit anything for the tutorial).

(1) **[Library Analysis, 10 points]** Open ng45.lib in a text editor. This is the Nangate 45nm standard cell timing/power library.

- Find cell INV_X1. It has all the information about the smallest inverter cell (X1 is the size). Most of the lines in the file are self-explanatory.
- [**Submit**] The area of the INV_X1 cell. (the area unit is um^2).
- [**Submit**] Find the output pin (ZN) of INV_X1. What is the function of the output pin?
- Find cell FA_X1. This is a full-adder cell.
- [**Submit**] The area of the FA_X1 cell.
- [**Submit**] Find the carry-out pin (CO) of FA_X1. What is the function of the output pin? (Express the function as a function of the input pins A, B, CI and the Boolean operations, • (AND) and + (OR).)
- Find cell DFF_X1. This is a D F/F cell.
- [**Submit**] The area of the DFF_X1 cell.
- [**Submit**] The "cell_leakage_power" of the DFF_X1 cell. The unit is nW.

(2) **[Synthesis, 20 points]** Download the following file into your working directory.

- http://eecs.wsu.edu/~ee434/Homework/hw03.zip
- Unzip it.
- Synthesize hw03_and6.v using the default compile command (compile –exact_map). It implements a six-input AND gate.
- [**Submit**] A gate-level schematic of the synthesized netlist.
- [**Submit**] Total area (run "report_area" to get the total area).

- Copy hw03_and6.v into hw03_and20.v.
    - cp hw03_and6.v hw03_and20.v
- We are going to make a 20-input AND gate. Modify hw03_and20.v in a text editor.
    - Change the module name from Vand6 to Vand20.
    - Change the input pin from [5:0] a to [19:0] a.
    - Change the assign statement to implement a 20-input AND gate.
- Synthesize it (compile –exact_map).
- **[Submit]** Total area.
- **[Submit]** Total dynamic power consumption (use "report_power").

(3) **[Synthesis, 10 points]** Timing optimization

- Create a 40-input AND gate.
- Synthesize it (compile –exact_map).
- [**Submit**] Total area and total dynamic power consumption.
- Run the following command to set up a timing constraint (160ps from any input to the output).
    - set_max_delay –from {a*} –to {z} 0.16
- Synthesize the design again, but add the following options.
    - compile –exact_map –map_effort high
- [**Submit**] Total area and total dynamic power consumption.
- Run "report_timing" to get timing info.
- [**Submit**] Slack (the last line in the timing report).