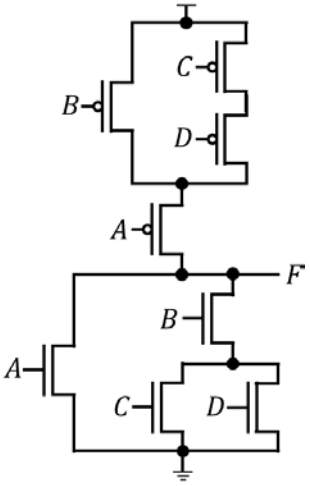
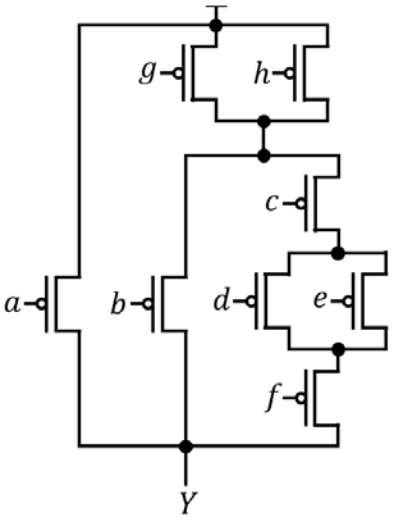
Homework Assignment 4
(Due Feb. 17th at the beginning of the class)

- R_n is the resistance of a 1X nFET.
- $\mu_n = 2\mu_p$.
- C_L is the load capacitance connected to the output.
- Target time constant: $R_n C_L$

(1) **[FET Sizing, 10 points]** Size the transistors in the following gate to satisfy the time constant. You should **minimize** the total width of the transistors.



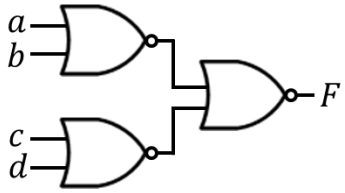
(2) **[FET Sizing, 10 points]** Size the transistors in the following pFET network to satisfy the time constant. **Try to minimize** the total width of the transistors.



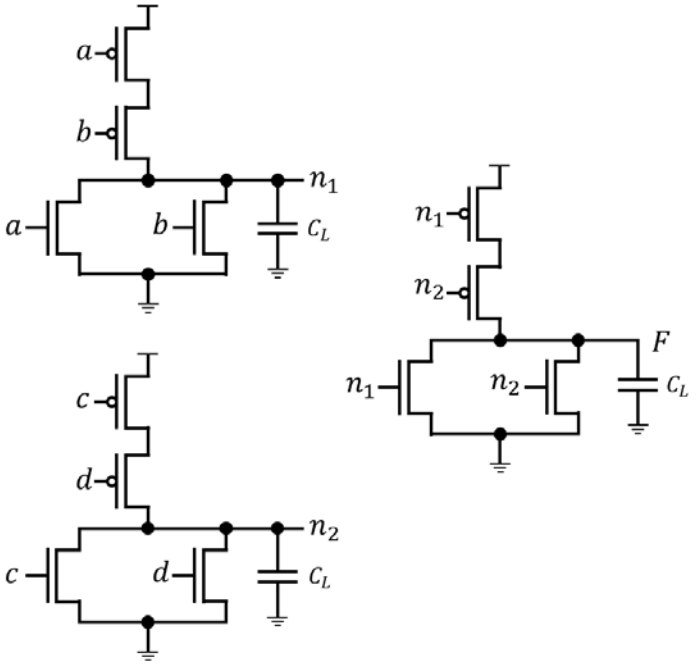
(3) **[FET Sizing, 10 points]** We are going to design the following logic:

$$\boldsymbol{F = (a + b) \cdot (c + d)}$$

We can design this logic as follows:



The schematic shown above can be modeled as follows to compute the delay from the inputs to the output:



To simplify the problem, we assume that the delay from an input to the output is computed by $\tau_1 + \tau_2$ where τ_1 and τ_2 are the time constants for charging or discharging the first and the second NOR gates, respectively. The target time constant is still $R_n C_L$. Size all the transistors in the three NOR gates to satisfy the target time constant. **Minimize** the total width of the transistors.