Homework Assignment 5
(Due Mar. 8th at the beginning of the class)

*** Submission policy: Please zip your files into a single zip file and send it to daehyun@eecs.wsu.edu. Please name the file "lastname, firstname.zip (or tar.gz or …)".**

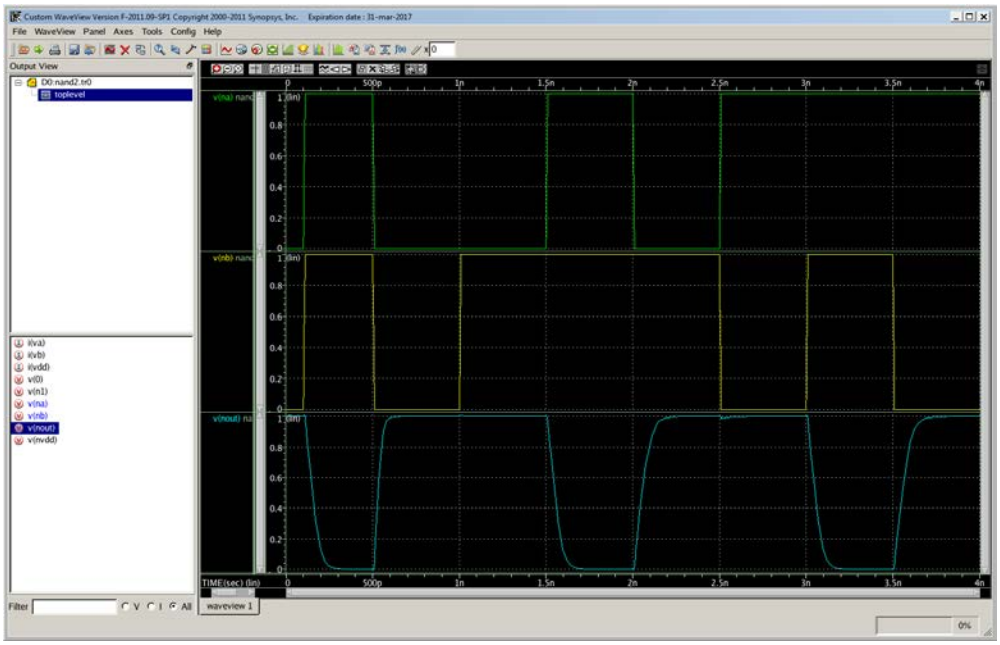
Go to "Labs" and see "tutorial-hspice.pdf". It shows how to use HSpice. Open inv.sp in the "tutorial-hspice.zip" file and read the comment carefully. Follow the tutorial. Now, you are ready for homework 5.

(1) **[Mobility Estimation, 10 points]**

- We are using 45nm technology. In this problem, we want to estimate the ratio between the electron mobility (μ_n) and the hole mobility (μ_p).
- Open inv.sp.
- **The minimum width of a transistor is 90nm** in this 45nm technology.
- Set the widths of the nFET and the pFET in the inverter to 90nm. (By default, they are set to 90nm. If not, set them to 90nm as follows: "mn1 Nout Nin 0 0 NMOS_HP L=45n W=90n" "mp1 Nout Nin Nvdd Nvdd PMOS_HP L=45n W=90n").
- Run HSpice simulation and open the waveform by running "wv inv.tr0". Measure the fall delay (when the output is 0.1Vdd) and the rise delay (when the output is 0.9Vdd). In my simulation, the fall delay is 117ps and the rise delay is 180ps.
- Size the pFET to match the rise delay with the fall delay, i.e., upsize the pFET to achieve 117~120ps rise delay. (**Note: the step size for the TR upsizing is 5nm, i.e., the width of a TR should be 5*N(nm) where N is an integer greater than or equal to 18**).
- [**Submit**] The width of the pFET after sizing and μ_n/μ_p estimated from the sizing.
    - When Wp=140nm, the rise delay is 120ps, so we accept it for the size of the pFET.
    - In this case, $\frac{\mu_n}{\mu_p} = \frac{W_p}{W_n} \approx 1.55$.

(2) [**Netlist Manipulation, 10 points**]

- Write a 1X two-input NAND gate netlist.
- Properly size the TRs so that it is a 1X gate.
- Modify the input waveform so that 1) you have two input waves, A and B and 2) you simulate the following six transition cases of the inputs (AB=00→11, 01→11, 10→11, 11→00, 11→01, 11→10). The input transition time should be 10ps. Simulate it.
- [**Submit**] Your HSpice source code and the output delay for each case.
    - input 00→11 (output 1→0): 110ps
    - input 01→11 (output 1→0): 110ps
    - input 10→11 (output 1→0): 110ps
    - input 11→00 (output 0→1): 62ps
    - input 11→01 (output 0→1): 120ps
    - input 11→10 (output 0→1): 120ps



(3) **[FET Sizing, 10 points]**

- Upsize the 1X two-input NAND gate to 4X by changing Wn and Wp.
- Simulate the six transition cases shown above.
- [**Submit**] The output delay for each case. For example,
    - input 00→11 (output 1→0): 36ps
    - input 01→11 (output 1→0): 30ps

- input 10→11 (output 1→0): 40ps
- input 11→00 (output 0→1): 21ps
- input 11→01 (output 0→1): 40ps
- input 11→10 (output 0→1): 40ps