Homework Assignment 11
(Due May 1st at the beginning of the class)

***** Submission policy: Please zip your source code and waveform screenshots into a single file and send it to daehyun@eecs.wsu.edu. The file name should be *firstname_lastname*.zip (or .tar.gz or .tar …)

(1) **[VHDL, 15 points]** Make a VHDL code for a 3:1 mux and test it with the following spec.

- Input ports: i0, i1, i2, (three data inputs), s1, s0 (two selection inputs)
- Output port: z
- Function: z=i0 when (s1s0=000), z=i1 when (s1s0=01), z=i2 when (s1s0=10), z=0 when (s1s0=11)
- Test input vectors (i2,i1,i0,s1,s0)
  - 00000 → 00001 → 00010 → 00100 → 00101 → 00110 → 01000 → 01001 → 01010 → 01100 → 01101 → 01110 → 10000 → 10001 → 10010 → 10100 → 10101 → 10110 → 11000 → 11001 → 11010 → 11100 → 11101 → 11110
- [**Submit**] Source code + test waveform (inputs + outputs)

(2) **[VHDL, 15 points]** Make a VHDL code for a D-latch with Enable and test it with the following spec.

- Input ports: D (data input), EN (enable), Clk (clock)
- Output ports: Q
- Function: If EN=0, $Q=Q_{prev}$. If EN=1 and Clk=0, $Q=Q_{prev}$. If EN=1 and Clk=1, Q=D.
- Test input vectors (D, EN, Clk)
  - 000 → 001 → 000 → 100 → 101 → 100 → 000 → 010 → 011 → 111 → 011 → 111 → 110 → 111 → 011 → 010 → 110 → 010
- [**Submit**] Source code + test waveform (inputs + outputs)