Tutorial – Synopsys Design Compiler

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Goal

- Learn how to use Synopsys Design Compiler

Overview

- Netlist synthesis converts given HDL source codes into a netlist.

- Synthesis software
  - Synopsys Design Compiler
  - Cadence Genus
  - ...

Setup

- Open a terminal.
- Create a work directory in your directory.
  - mkdir hw03
- Go to the directory.
  - cd hw03
- Check your shell by the following command.
  - echo $SHELL
- If the terminal says you are using not bash (e.g., /bin/bash) but something else (e.g., /bin/csh), run bash as follows.
  - bash
- **Notice**
  - **If your default shell is not bash, you will have to run bash every time you log in to your account.**
  - **If you want to change the default shell to bash and forget it, run "chsh –s /bin/bash".**

Setup

- Get the tutorial file. This will download tutorial-dc.zip.
    - wget http://eecs.wsu.edu/~ee434/Labs/tutorial-dc.zip
- Unzip it.
    - unzip tutorial-dc.zip
- Run the following command to list all the files in your current directory.
    - ls –al
- Make sure you have the following files.
    - ictools_generic.sh
    - synopsys.sh
    - ng45.db (Nangate 45nm library file)
    - ng45.lib (Nangate 45nm library file)

Setup

- Run the following commands.
  - source ictools_generic.sh
  - source synopsys.sh
- If you see any error, you will have to fix it or contact the TA or me to fix it.
- Now you are ready to run DC.

Run DC

- Run the following command.
  - design_vision –no_gui
- You will see the following message.

```
                    DC Professional (TM)
                       DC Expert (TM)
                       DC Ultra (TM)
                   FloorPlan Manager (TM)
                      HDL Compiler (TM)
                      VHDL Compiler (TM)
                     Library Compiler (TM)
                  DesignWare Developer (TM)
                      DFT Compiler (TM)
                        BSD Compiler
                     Power Compiler (TM)

        Version D-2010.03-SP5-2 for linux -- Jan 21, 2011
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for which you have lawfully obtained a valid license key.

Initializing...
design_vision>
```

Run DC

- Set libraries.
  - set link_library {ng45.db}
  - set target_library {ng45.db}
- Read a source file.
  - read_file –format verilog {ex.v}
- Compile (synthesis)
  - compile –exact_map
- Save the synthesized netlist.
  - write –format verilog –output ex_syn.v
- Exit from DC.
  - exit

Netlists

- Open ex.v in a text editor.
  - Draw a gate-level schematic for the netlist.
    - Input: a [4:0]
    - Output: z
  - Express z as a Boolean function of the inputs.

- Open ex_syn.v in a text editor.
  - Draw a gate-level schematic for the netlist.
  - Express z as a Boolean function of the inputs.

- Are they equivalent?