SYNOPSYS

Before you run any synopsys product, you need to source synopsys. In your directory where you want to run synopsys, type the following command:

% source /net/ictools/csh/synopsys.csh (if you are using c shell)

If you are using synopsys to running a ***test bench***, see **Part 1**.

If you are using synopsys for the ***synthesis***, see **Part 2**.

Part 1: Using synopsys running a test bench

At this point, you have two vhdl files, one is your behavior file and the other is your test bench file. For instance, CNT_BHV.vhd and TB_CNT_BHV.vhd if we using a counter as a sample.

Follow the steps listed:

1. **vhdlan** CNT_BHV.vhd
2. **vhdlan** TB_CNT_BHV.vhd
3. **vcs –debug_all** CFG_TB_CNT_BHV
4. **./simv**
5. **dve &**

After the last step, you should see GUI interface, then follow the instructions here:

1) Simulator (Menu Option)
    a) Setup
        i) Simulator Executable Browse
            (1) Find and Select **simv**
        ii) Simulator Arguments
            (1) Type **-ucligui**
        iii) Click OK
2) Select wanted signals, usually all of them (should be second panel in GUI, ctrl click to select multiple)
    a) Right click
        i) Add To Waves
            (1) New Wave View
3) Simulator (Menu Option)
    a) Start (F5 works also)

Part 2: Using synopsys running a synthesis

You need to configure your **.synopsys_dc.setup** before you run design_analyzor.
Place the **.synopsys_dc.setup** file in your home directory. The template is as shown below for 65nm:

```
#########################################################################
set designer "Paul Wettin"
set company "Washington State University, EECS"

set search_path "$search_path /net/ictools/pdk/CMOS065/CORE65LPSVT_SNPS-AVT-CDS_4.1/libs /net/ictools/pdk/CMOS065/CORE65LPSVT_SNPS-AVT-CDS_4.1/PLIB"
set physical_library "CORE65LPSVT.pdb"
set link_library "* CORE65LPSVT_nom_1.00V_25C.db"
set target_library "CORE65LPSVT_nom_1.00V_25C.db"
set symbol_library "CORE65LPSVT.sdb"
#########################################################################
```

After you setup your configure file, type command **design_vision &**.
Then following steps needs to be done: (ASSUMES YOU HAVE A SIGNAL NAMED “clk”!!!!!)

1) File
    1. Read design (open .vhd file)
        1. Click file (ctrl click for multiple files)
2) Command Line
    1. **elaborate** <name>
    2. **current_design** <name>
    3. **link**
    4. **uniquify**
    5. **create_clock –name “myclk” –period 10 {clk}** (creates clk signal with period of 10 and attaches itself to the clk pin)
    6. **create_clock –name “vclk” –period 10** (creates virtual clk signal with period of 10; MAY OR MAY NOT be needed)
    7. **set_input_delay –max 0 –clock myclk [remove_from_collection [all_inputs] [get_ports clk]]** (if report_timing and report_power don’t work, you might need to add this line, synchronizes the data to clk, DON’T USE UNLESS THE REPORTS FAIL)
    8. **compile –map_effort medium** (**low** or **high** work also)
    9. **report_timing** (only shows worst case)
    10. **report_timing –nworst 10** (shows the top 10 worst cases, 100 would show 100, etc.)
    11. **report_power** (shows total power)
    12. **report_power –flat** (shows power for each individual gate. WARNING: will take a LONG LONG LONG time to run this simulation)
    13. **report_power -hier** (shows power for each block, if there are blocks, else will just show total power)