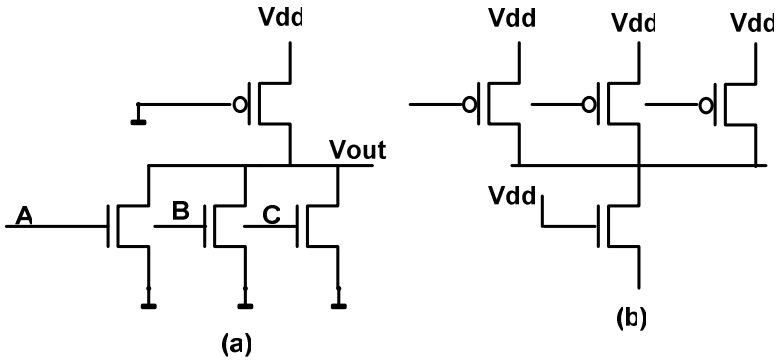
EE434 ASIC & DIGITAL SYSTEMS
FINAL EXAM
17th December 2008

School of Electrical Engineering and Computer Science
Washington State University

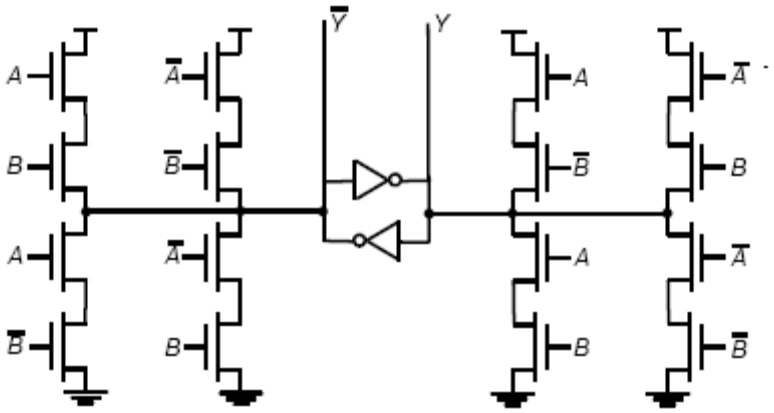
Time: 120 minutes
Maximum Points: 55

(1)

(a) The circuits (a) and (b) below are pseudo-NMOS and pseudo-PMOS gates respectively. What function is performed by each gate? Which one of the following gates is favorable over the other? [5]



(b) What is the logic function (Y) computed by the following circuit? [5]



(2)

(a) Illustrate how to implement the following function in an 8:1 multiplexer [5]

$$F = \overline{A \oplus B \oplus C \oplus D}$$

(b) Implement the following Boolean function with the help of one two-input LUT and another three-input LUT. You are allowed to use only these two LUTs, nothing else. [5]

$$f = \overline{x}_1 x_2 x_3 + x_1 \overline{x}_2 x_3 + x_1 x_2 x_4 + \overline{x}_1 \overline{x}_2 x_4$$

(3)
(a) A four-input multiplexer is described by the following entity declaration

```
Entity mux4 is
        Port (i0, i1, i2, i3, sel0, sel1: in bit;
                                  Z: out bit);
        End entity mux4;
```

You are asked to implement a two-input multiplexer with this component. Please show your port mapping implementing the two-input multiplexer. [4]

(b) The data on a diskette is arranged in 18 sectors per track, 80 tracks per side and two sides per diskette. A computer system maintains a map of free sectors. Write a three-dimensional array type declaration in VHDL to represent such a map, with a '1' element representing a free sector and a '0' element representing an occupied sector. [2]

(4)

(a) The verilog code for a priority encoder is given below. When we tried to synthesize this in Synopsys we got the following comment *"Inferred memory devices in process in routine priority_always"*. Explain the reason behind this. [3]

```
Module priority_always (input [3:0] a, output reg [3:0] y);
Always @ (*)
If (a [3]) y<=4'b1000;
Else if (a [2]) y<=4'b0100;
Else if (a [1]) y<=4'b0010;
Else if (a [0]) y<=4'b0001;

Endmodule
```

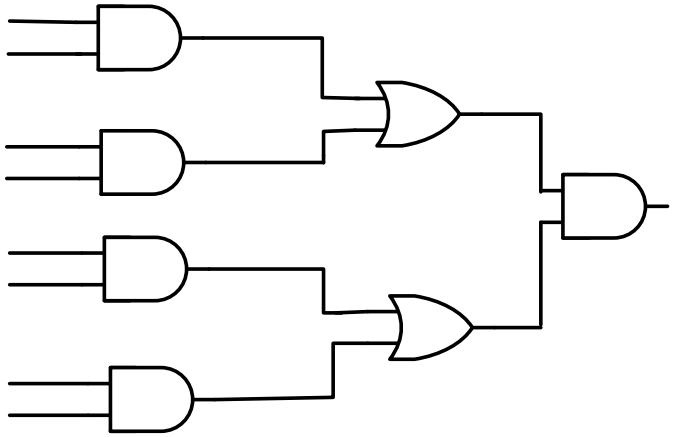
(b) A state machine has 5 states. The state encoding is shown in the following table

State	q_0	q_1	q_2
idle	0	0	0
decision	0	0	1
read1	0	1	0
read2	0	1	1
read3	1	0	0

What might be the problem when you express this state machine in VHDL? How that can be resolved? Note: You do not have to write the code for the whole state machine; just show the step, which will resolve the problem. [3]

(5)

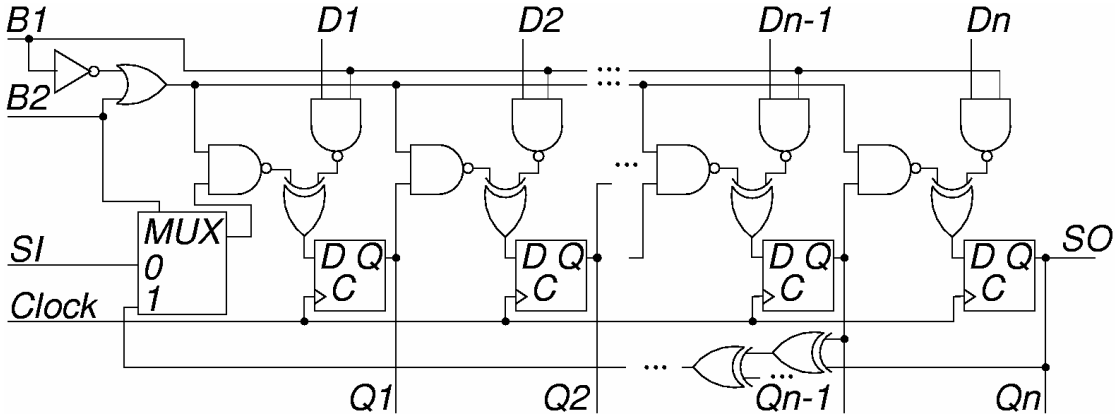
(a) What is the total number of single stuck-at faults in the following circuit? What will be this number after equivalent fault collapsing? [4]



(b) Design a *modular* LFSR for the following polynomial [4]

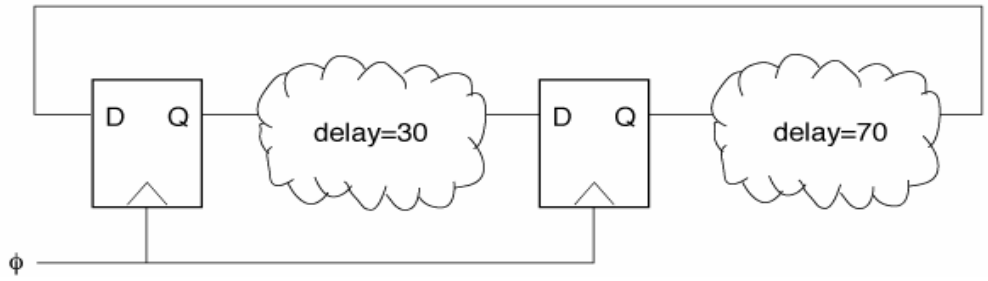
$$f(x) = 1 + x^2 + x^7 + x^8$$

(c) What are the values of the control signals B1 and B2, if we want to use the following BILBO in the "pattern generator" mode? Show the path activated in this mode. [2]



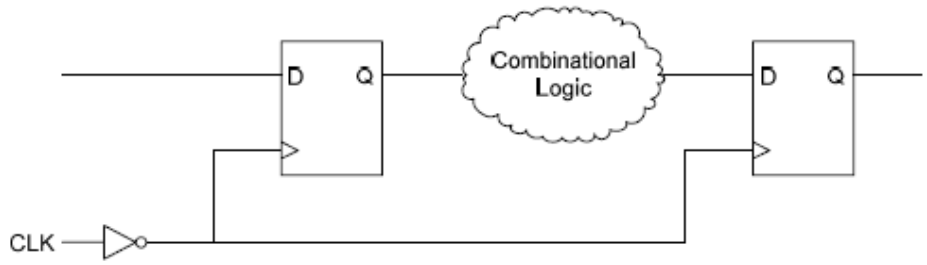
(6)

(a) Do you see any problem with the following two phase machine? How can you resolve that? [2]

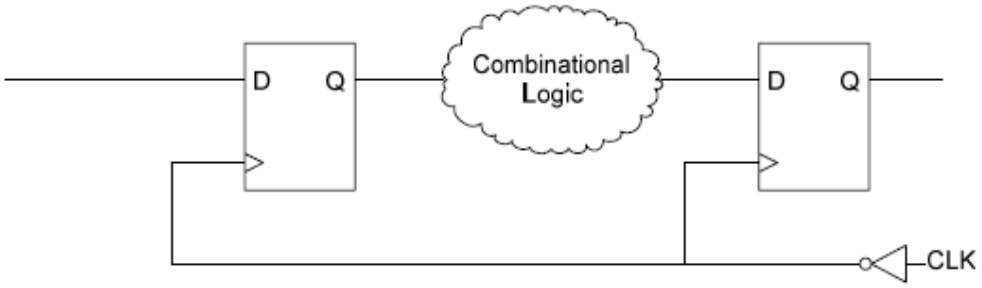


(b) Suppose you are designing a datapath using custom-layout techniques. Your data flows from left to right, as shown in the following two diagrams. In the first diagram, the clock is driven by a driver on the left side of the chip, and the clock propagates from left to right. In the second diagram, the clock is driven by a driver on the right side of the chip, and the clock propagates from the right to the left. Which design is safer? [3]

Layout 1:

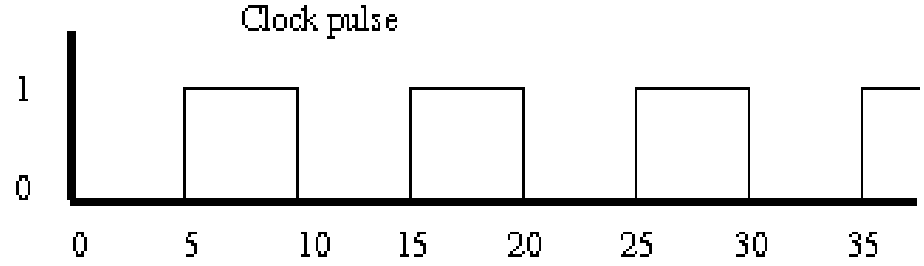


Layout 2:



(7)

(a) Write the verilog statements between the begin and end block to generate the following pulse trains [3]



begin
……
…….
End

(b) What are the possible fault types in a transistor? [2]

(c) Why do we need a Test Access Mechanism (TAM) while testing a SoC? What is the role of the wrapper in this context? [3]