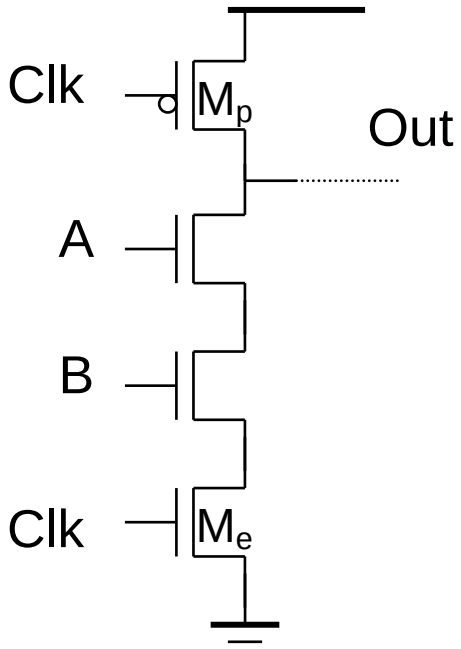
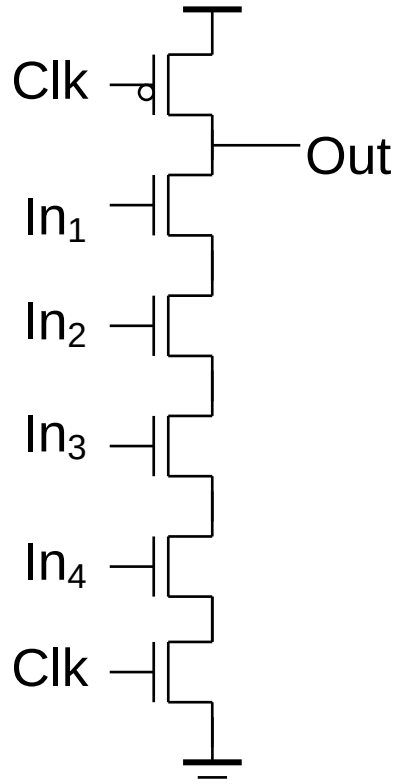
EE434 ASIC & DIGITAL SYSTEMS
MIDTERM EXAM
6th October 2010
2.10-3 pm
School of Electrical Engineering and Computer Science
Washington State University
Maximum Points: 35

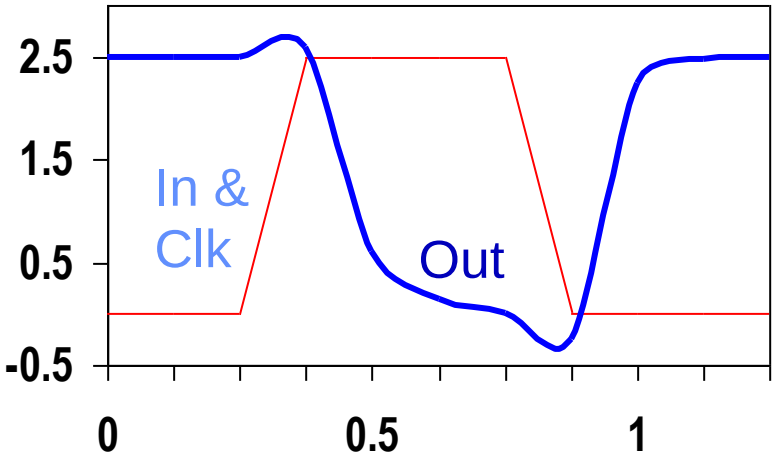
(1)

(a) In the following circuit at the evaluation phase, A=1, but B=0. What will happen to the voltage at the output node? How can you solve that problem? [3]



(b) In the following circuit the input and the output waveforms are shown in the adjacent figure. Do you see any problem with the output waveform? What is the reason behind that? [3]

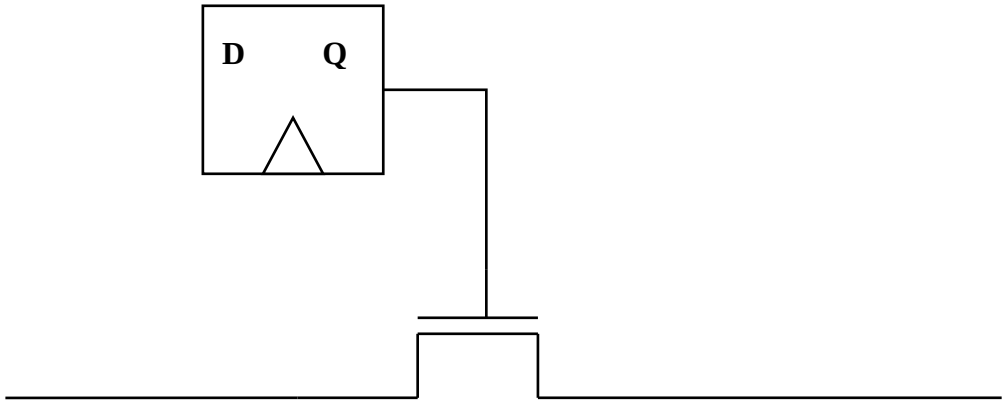




(2)

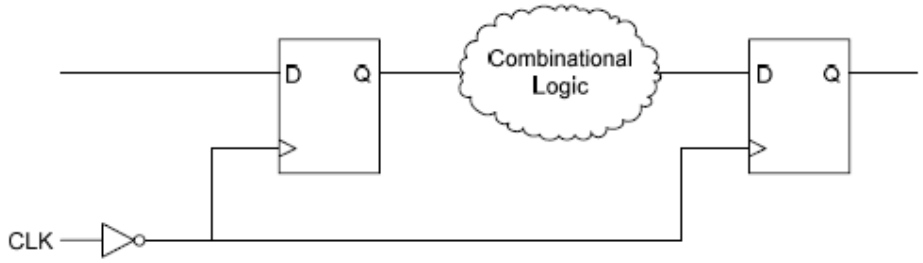
(a) Given the function $f = x_1 x_2 x_4 + x_2 x_3 \overline{x_4} + \overline{x_1}\,\overline{x_2}\,\overline{x_3}$, show a circuit of two-input LUTs that realizes the function. You can use **only** 7 two-input LUTs. Label the output of each LUT with an expression representing the logic function that it implements. [4]

(b) One of the common configurations for creating programmable interconnects in FPGAs is shown below. What are the principal disadvantages of this in terms of delay and power? [2]

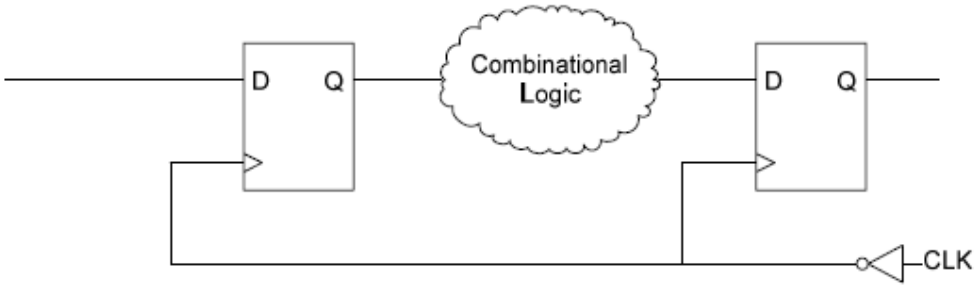


(c) Suppose you are designing a datapath using custom-layout techniques. Your data flows from left to right, as shown in the following two diagrams. In the first diagram, the clock is driven by a driver on the left side of the chip, and the clock propagates from left to right. In the second diagram, the clock is driven by a driver on the right side of the chip, and the clock propagates from the right to the left. Which design is safer? [3]

Layout 1:

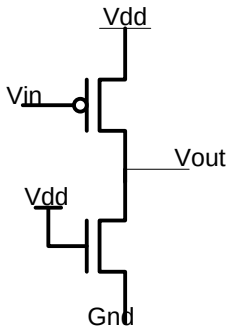


Layout 2:



(3)

(a) A new logic family is proposed whereby the NMOS device acts as a load device and the PMOS device acts as the inverting device, as shown in the following figure. What are the advantage and disadvantages of this pseudo-PMOS architecture over the pseudo-NMOS architecture? [4]



(b) What will be the Process statement of the following concurrent signal assignment? You just need to write the process statement with proper sensitivity list [4]

cnt_out <= (others => ‘z’) when oe= ‘o’ else cnt;

4.

(a) Suppose a part of your VHDL code has the following statements. Will this VHDL be synthesizable? If not, please explain the reason [3]

```
signal VALUE: INTEGER range 0 to 15;
signal OUT_1: BIT;
case VALUE is
when 0 to 10 =>
OUT_1 <= '1';
when 5 to 15 =>
OUT_1 <= '0';
end case;
```

(b) Using *three* 2:1 multiplexers implement the following function

F = (a and b_bar) or (c and d) [3]

(c) The two CMOS circuits shown below are intended to be simple latches. Do these gates work as latches? Are there any problems with using them as latches? Is one better than the other? Explain [5]