EE434
ASIC & Digital Systems

Lab 3

Design of a Switch Block for FPGA

Spring 2015
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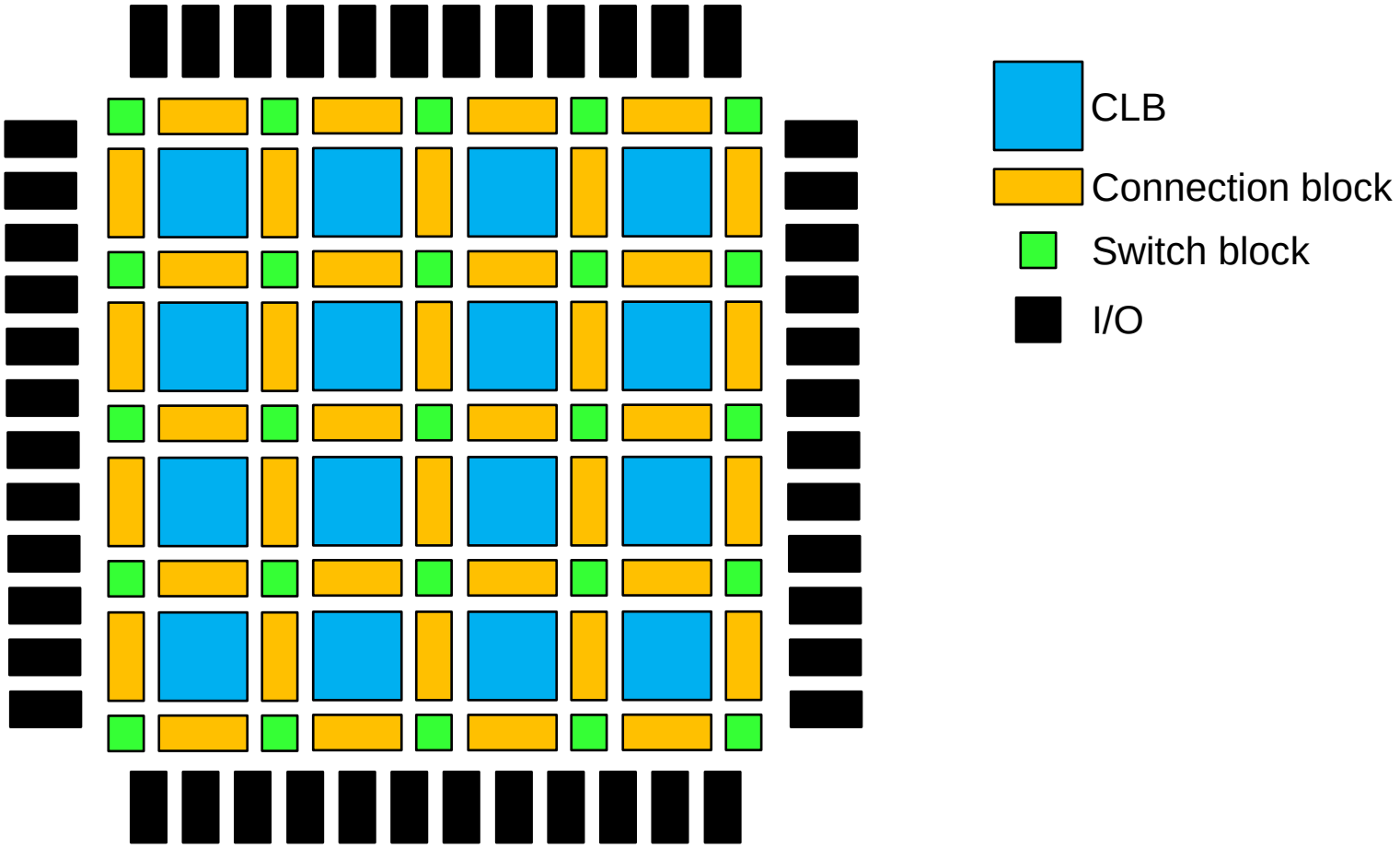
Lab 3

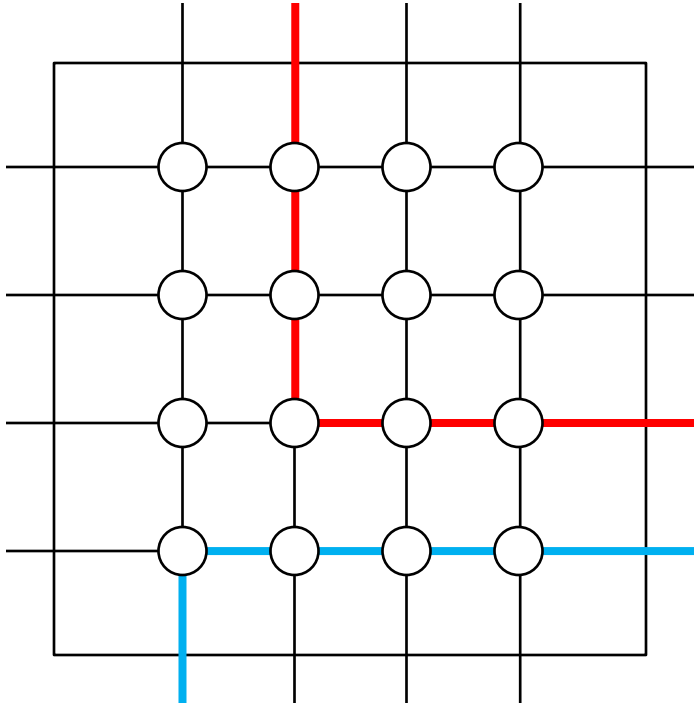
- Due Apr. 24 (firm)

FPGA

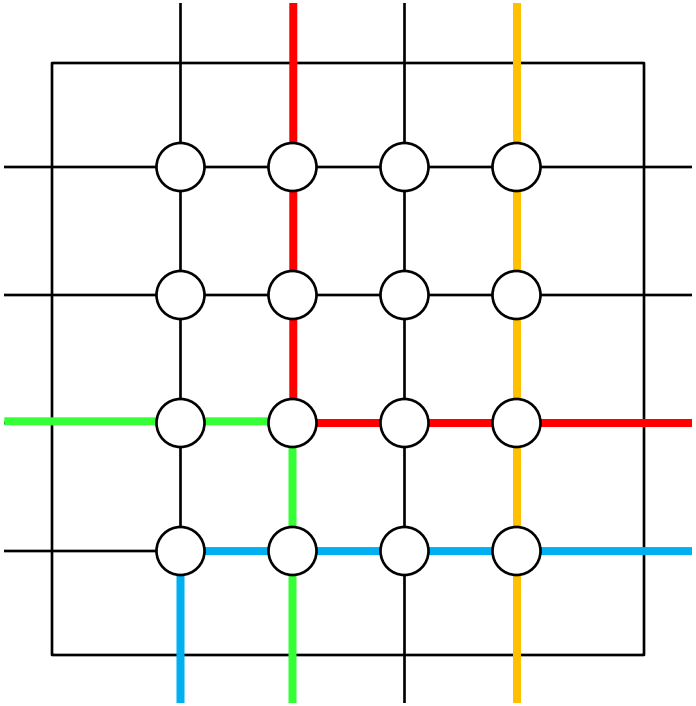
- Reconfigurable logic



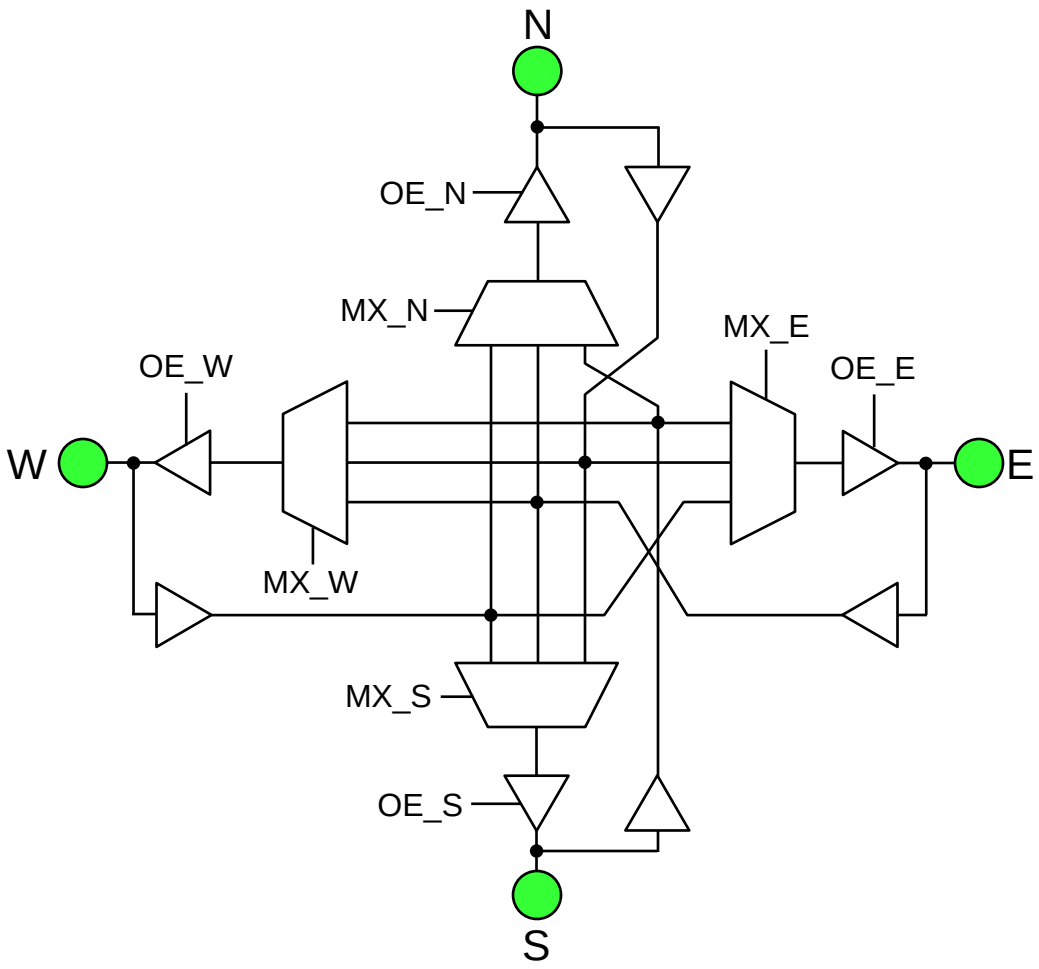
Connection Block



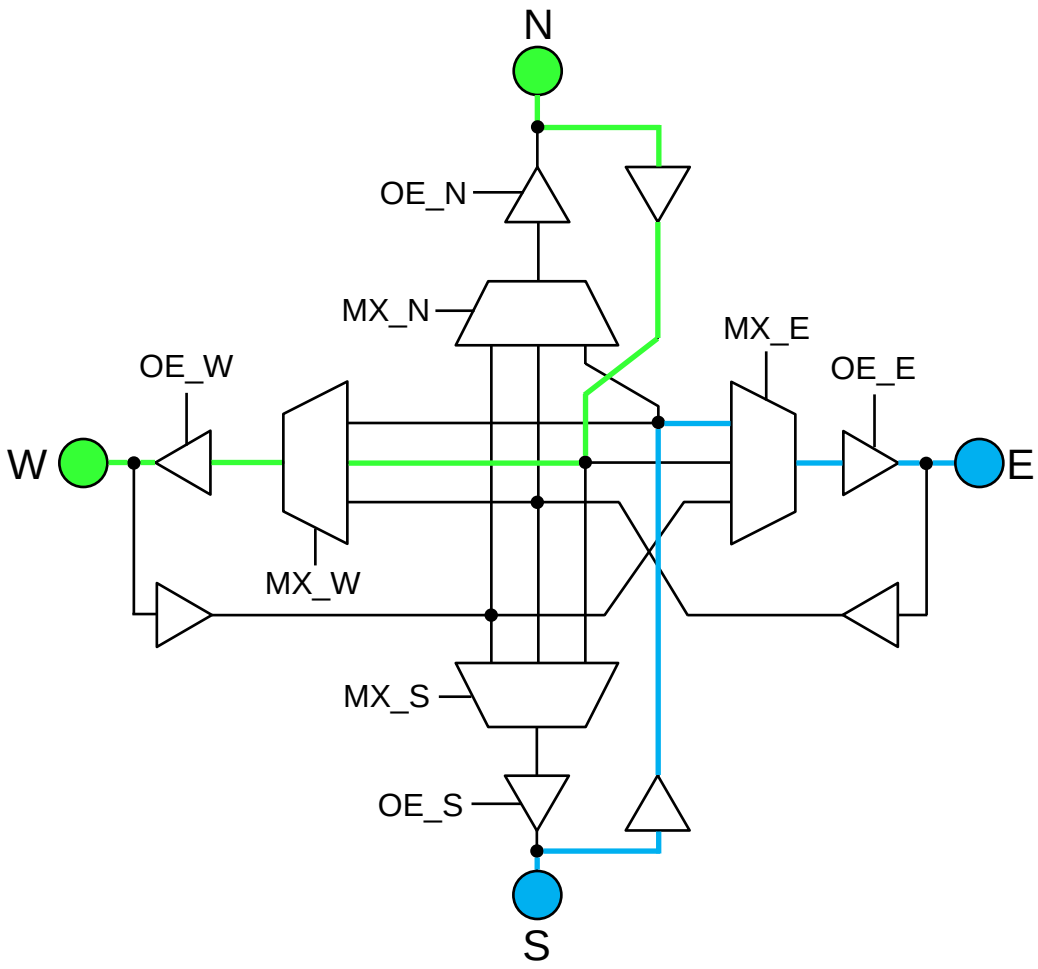
Switch Block

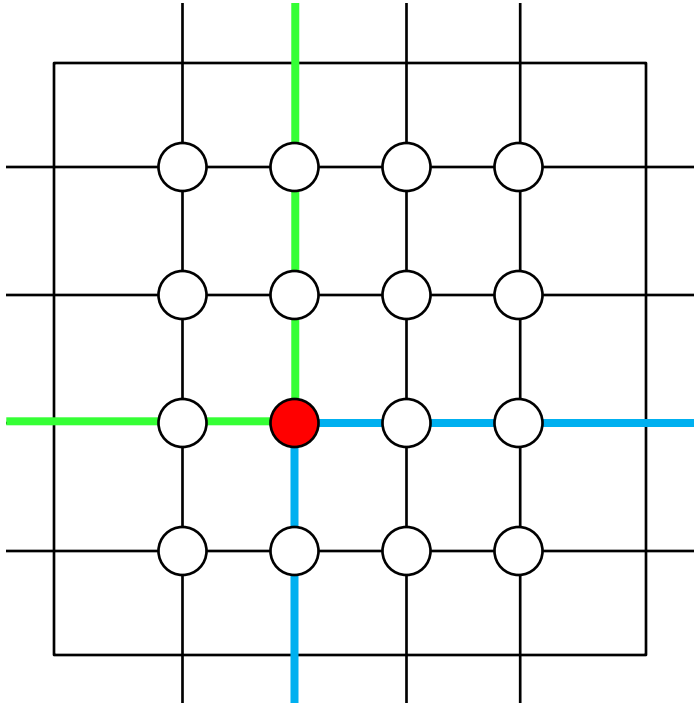


Switch Block



Switch Block





Inputs and Outputs

- Four primary inouts

- 12 control signals
  - Four output enable (OE_X) signals
  - Eight mux_control signals (two for each mux)

How to Proceed

1. Conceptually design the switch block.

2. Design each sub block (SPICE netlist).

3. Create a top-level SPICE netlist.
    1. Instantiate the sub-blocks.
    2. Apply test input vectors.
    3. Obtain worst-case rise and fall delays.

Simulation

- Notice that each primary inout pin (NSEW) is bidirectional.
- Therefore, you should attach a load cap (10fF) at each primary inout pin if it is used for output.
- You should apply a proper input signal waveform to each primary inout pin if the it is used for input.

Spec

- Rise delay, Fall delay: ≤ 1000ps
- Total power: ≤ 400uW
- Input transition time (10% - 90%) for simulation: 50ps

Submit

- SPICE netlists.
- Worst-case rise and fall delays
- Worst-case power consumption
- Description of how you designed the switching structure and each sub block.