EE434
ASIC & Digital Systems

Project

Design of a High-Speed Low-Power 32-Bit Adder

Spring 2015

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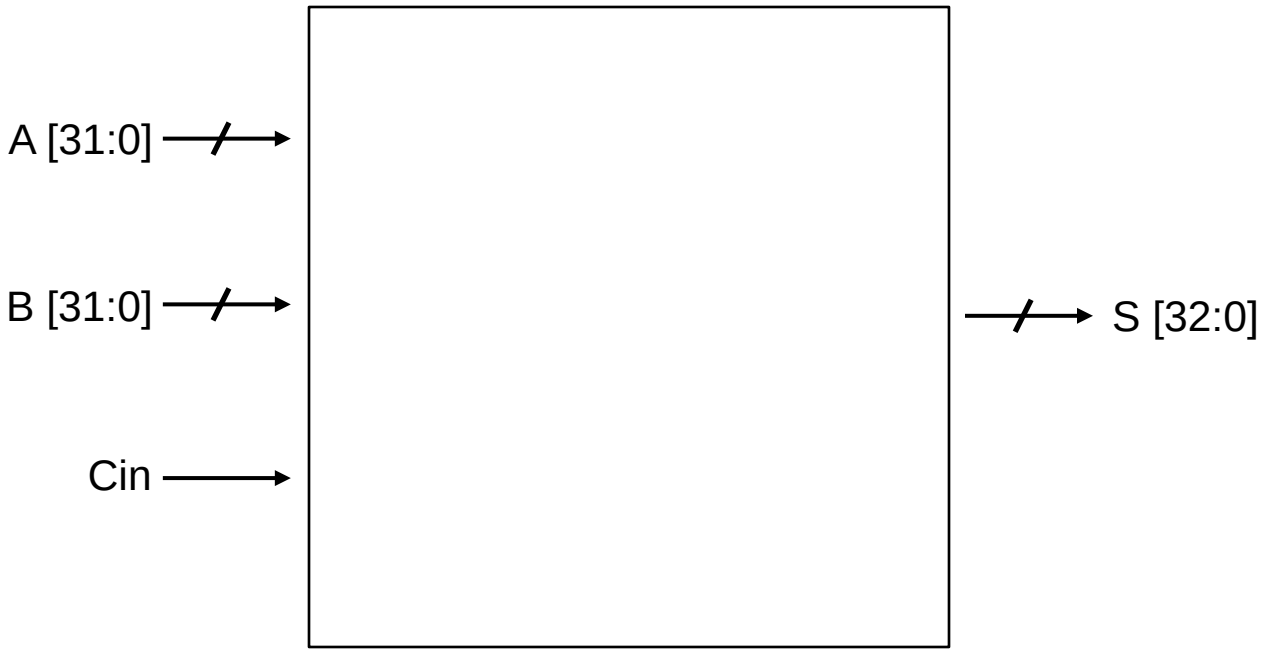
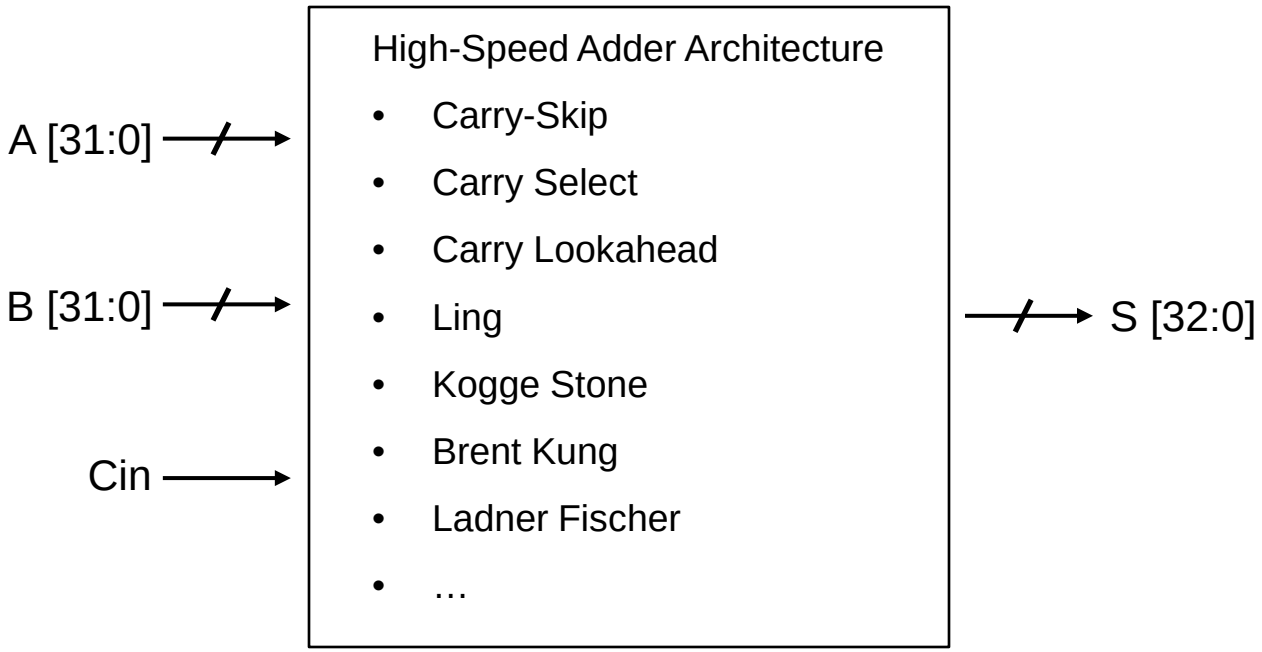
Project

- Due May 1 (firm)

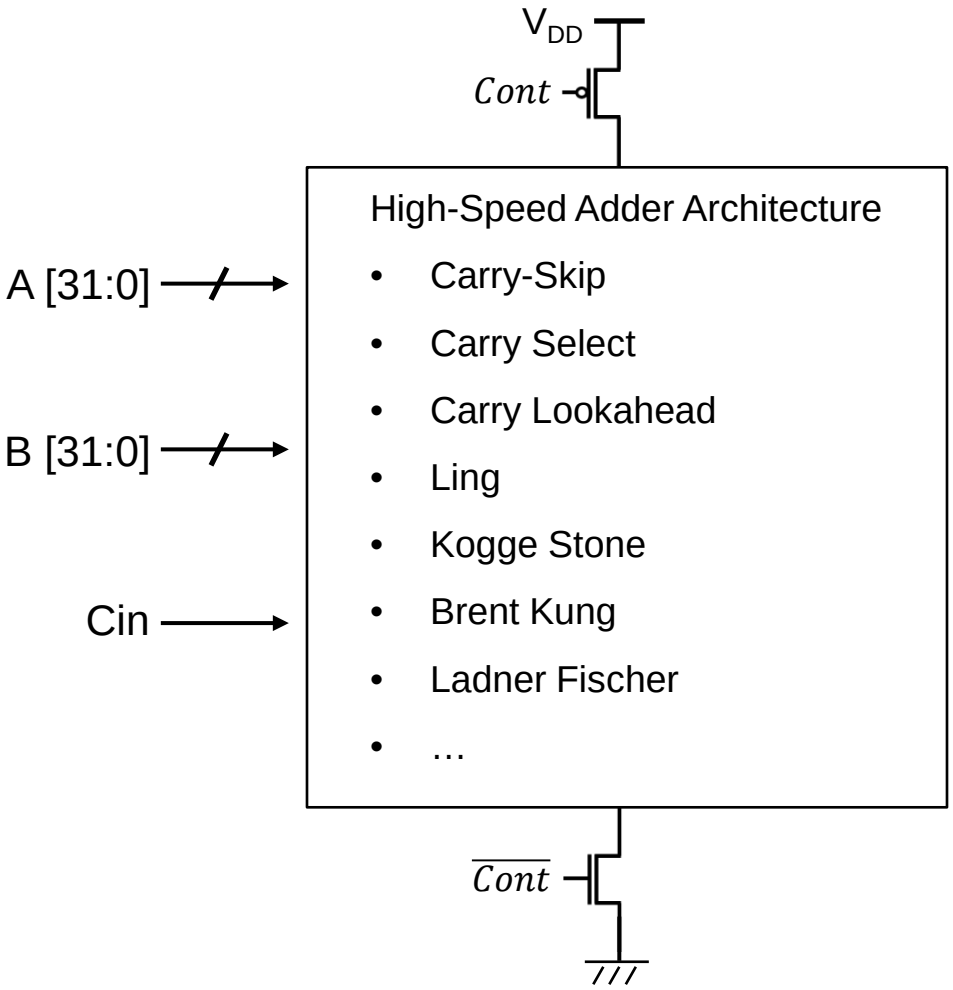
32-Bit Adder



High-Speed 32-Bit Adder



High-Speed Low-Power 32-Bit Adder

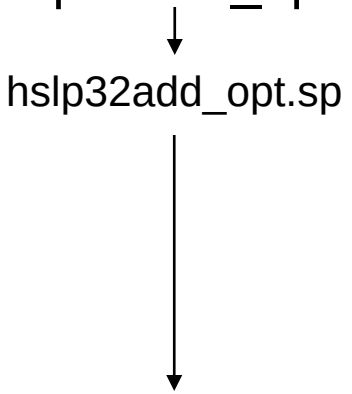


Power Gating

- When Cont=0: ON
- When Cont=1: OFF

Design Procedure

1. Verilog coding (hslp32add.v) ➡ This will be provided.
2. Automatic P&R and optimization (layout, hslp32add_opt.v)
3. Export (hslp32add.gds)
4. Import into Virtuoso.
5. Add sleep transistors. Modify the netlist.
6. DRC/LVS/xRC. Post-layout simulation and optimization.



Design Procedure

- Submit
  - Layout snapshot
  - Worst-case rise and fall delay (NOT rise and fall times) and waveforms
  - LVS/xRC report
  - Design report
    - Description of how you designed it, e.g., how you sized the PMOS and NMOS transistors.

Files

- Download the following file.
  - http://eecs.wsu.edu/~ee434/Labs/proj.tar.gz

How to Export GDS from Encounter

- Use the following command.
  - streamOut <gds_file_name> -mapFile <map_file> -libName <virtuoso_library_name> -structureName <top_level_cell_name> -disAreaAsBoundary -units 2000 -mode ALL
  - The map file will be provided.

- Example
  - streamOut 03_postrouteopt.gds -mapFile ng45nm.map -libName ng45nm_proj1 -structureName VKSA32 -dieAreaAsBoundary -units 2000 -mode ALL

Netlist Conversion (Verilog → SPICE)

- v2lvs –v <verilog_netlist> -l <verilog_library> -o <output>
  - Verilog_library will be provided.

- Example
  - v2lvs –v my_netlist.v -l Nangate.v -o my_netlist.sp

How to Proceed

1. Design an adder in Encounter.
   - The initial verilog netlist will be provided.
2. Export it into a gds file.

3. Create a new library in Virtuoso.
4. Import a standard cell library.
   - gds for standard cells will be provided.
5. Import the gds file you exported in Encounter into the library.
6. Export the top-level gds file.
7. Run LVS to make sure your initial DB is correct.
8. Run xRC to get a PEX SPICE netlist.

How to Proceed

9. Add sleep transistors to your PEX SPICE netlist.
10. Simulate it (HSpice) and optimize the sleep transistors.
11. Draw the sleep transistors in your layout (Virtuoso).
12. Run LVS and PEX.
13. Simulate it (HSpice).