EE434
ASIC & Digital Systems

From Layout to SPICE Simulation (Virtuoso, Calibre, HSpice)

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Preparation for Lab1

- Download the following file into your working directory.
  - wget http://eecs.wsu.edu/~ee434/Labs/lab1.tar.gz

- Unzip it.
  - tar xvfz lab1.tar.gz

Files

- Shortcuts
  - common_bindkeys.il
  - leBindKeys.il
  - schBindKeys.il
- sh
  - Files to source
- Tech file
  - tech_ng45nm.tf
- Display resource file
  - display.drf
- rules
  - layer.inc
  - calibreDRC.rul
  - calibreLVS.rul
  - calibrexRC.rul
- myInv_X1_LVS.sp: A netlist for LVS
- myInv_X1_simul.sp: A netlist to simulate an inverter with parasitic RC.
- myInv_X1_noRC_simul.sp: A netlist to simulate an inverter without parasitic RC.

What We Are Going To Do

1. Layout
2. DRC
3. LVS
4. xRC
5. SPICE simulation

How to Launch Virtuoso

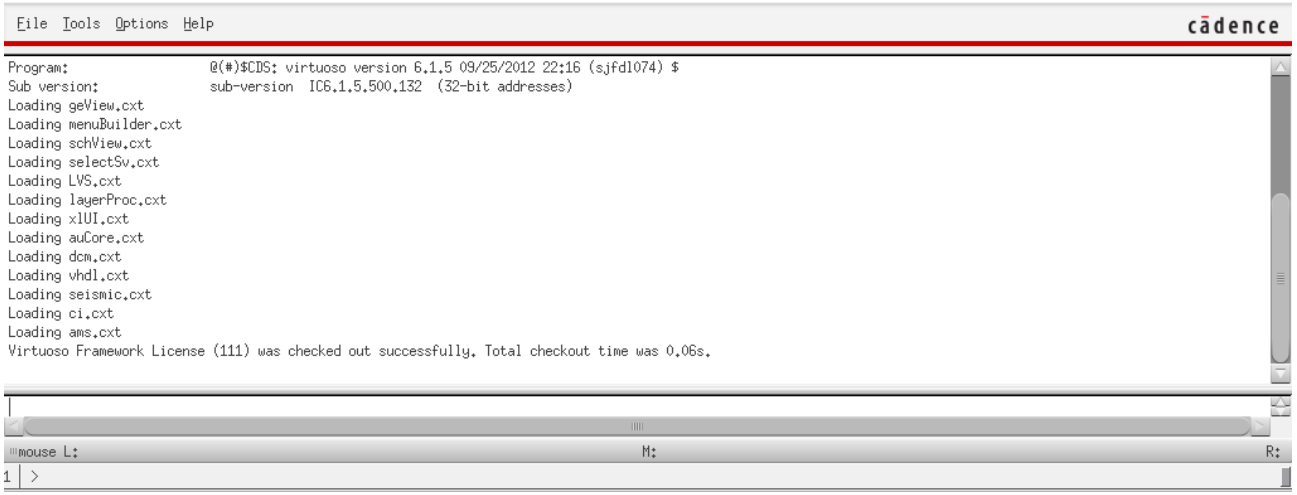
- Source the following file:

  > source sh/cadence-ic.sh

- Run Virtuoso

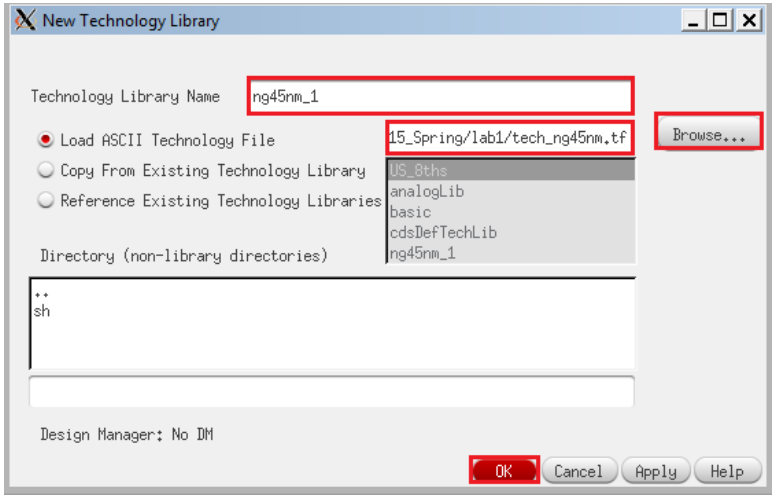
  > virtuoso

- You will see a Cadence logo and a main window (Command Interpreter Window, CIW) as follows:



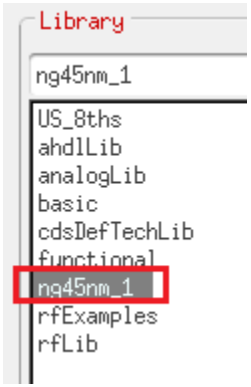
Create a Library

- In CIW
  - Click “Tools” → “Technology File Manager…”.
- In the Technology Tool Box window
  - Click “New…”.
- In the New Technology Library window
  - Enter a library name you want.
  - Click “Browse…” to load tech_ng45nm.tf.
  - Click OK.
- You will see the following message.



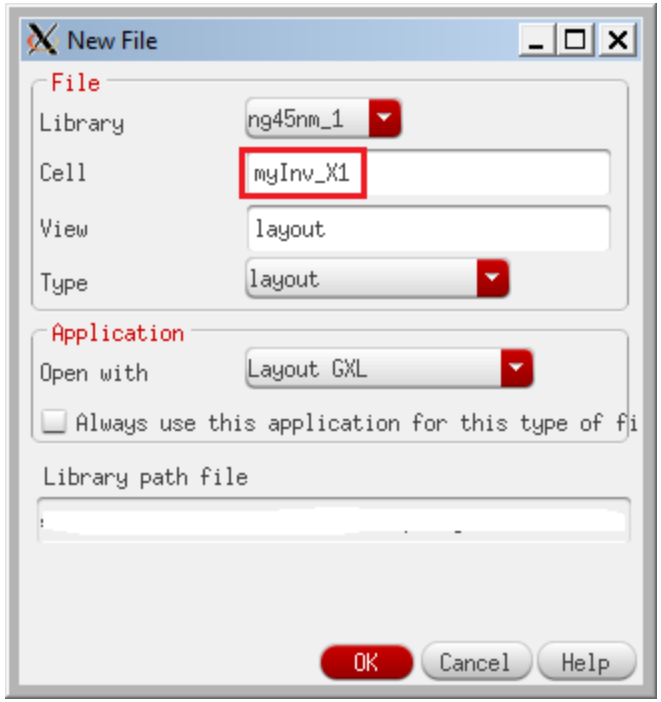
Create a Library

- Close the Technology Tool Box window.
- In CIW, click Tools → Library Manager …
- In the leftmost column, you will see both your library and some default libraries.



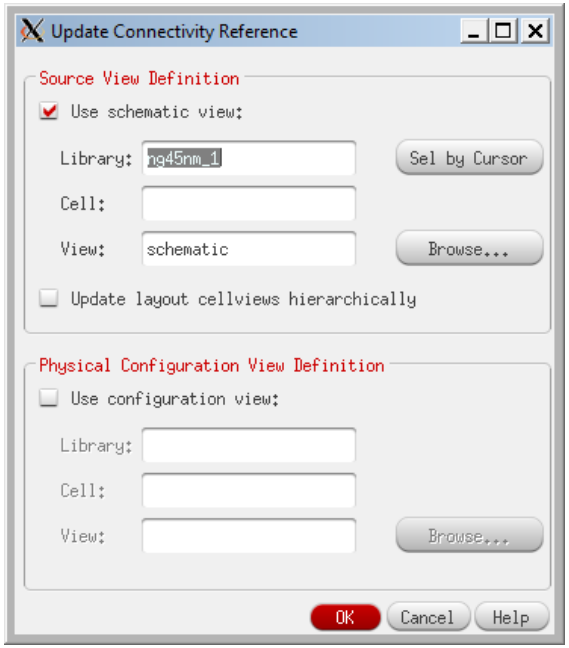
How to Create a Cell

- In the Library Manager window, click File → New → Cell View.
- Enter a cell name and click OK.

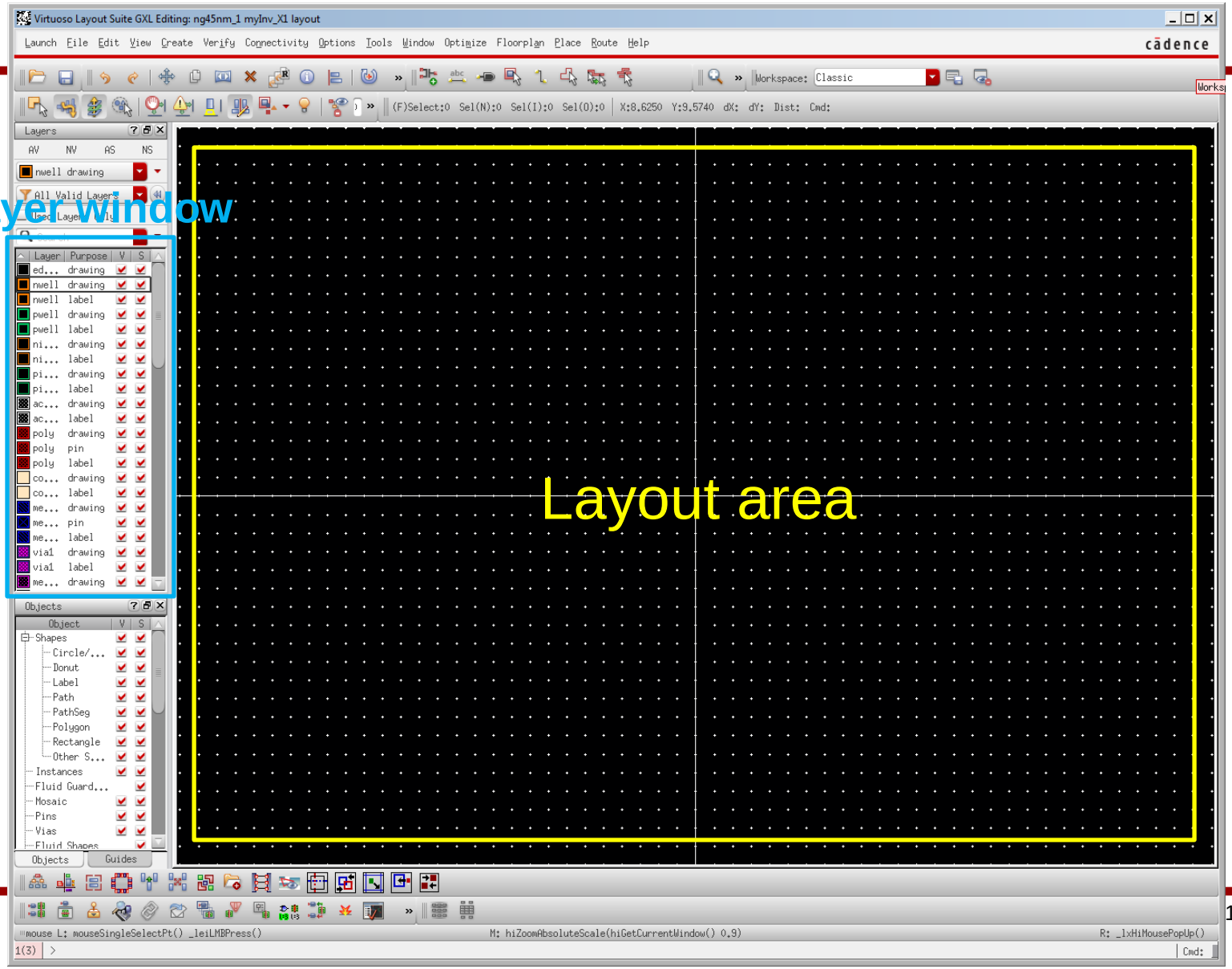


How to Create a Cell

- If the following window pops up, uncheck the “Use schematic view:” and click OK.

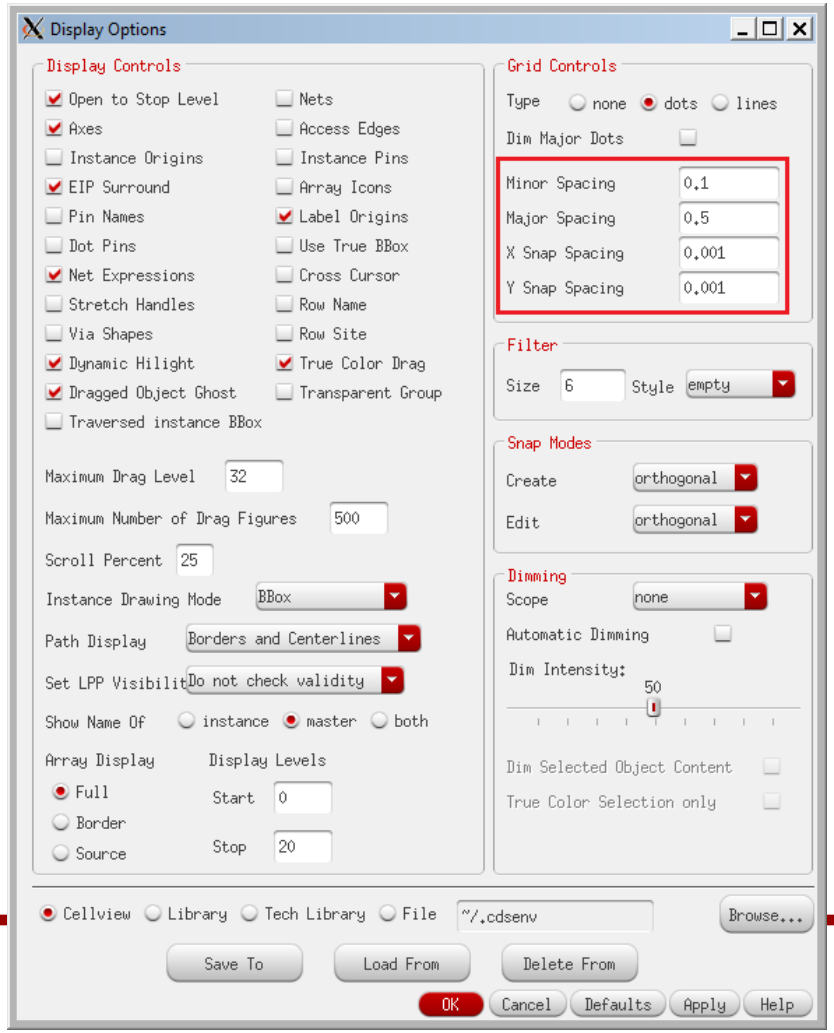


Layout Window



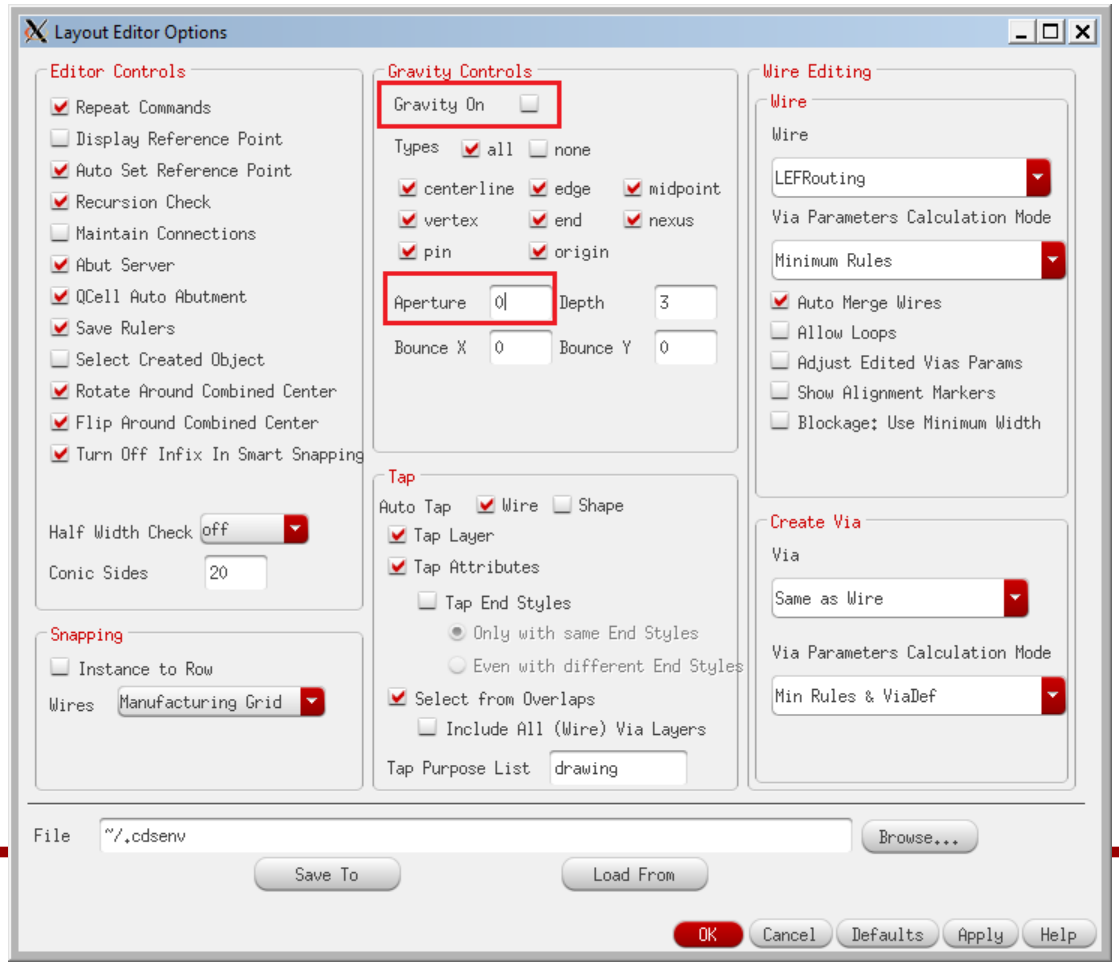
Editor Setup

- Press “e” or click “Options” → “Display…”. Use the following setting.



Editor Setup

- Press “Shift+e” or click “Options” → “Editor…”. Use the following setting. (Turn off “Gravity On”).

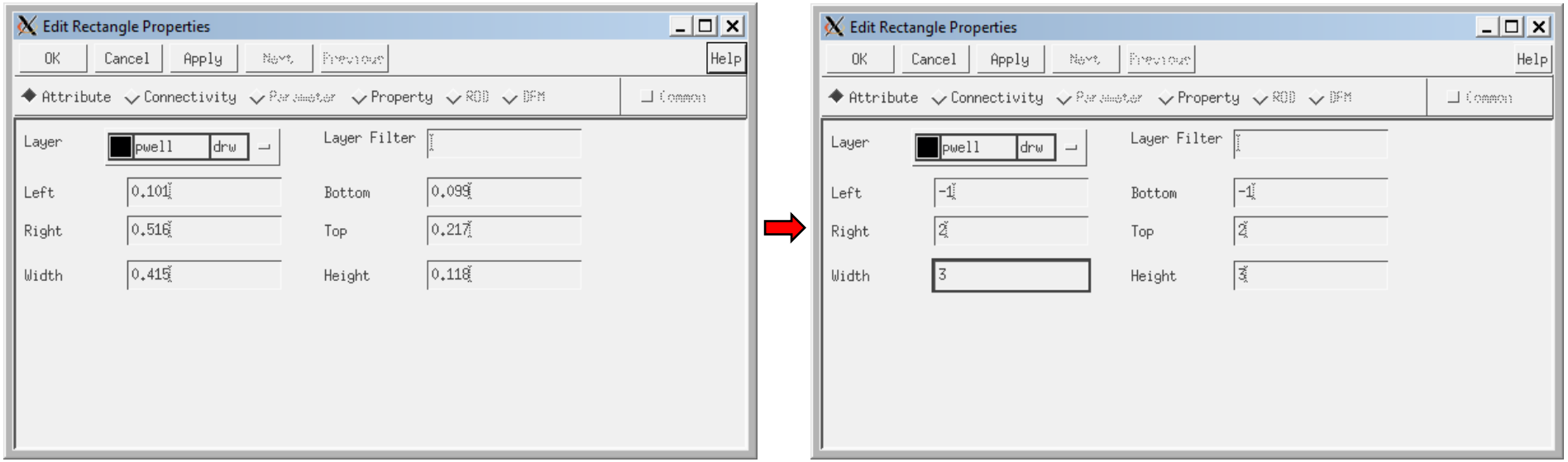


How to Draw Objects

- Use the right mouse button to zoom in.
- Choose a layer you want to draw in the layer window.
  - Choose “drawing” for the “Purpose”.
- Press “r” or Click “Create” → “Shape” → “Rectangle”. Now you are ready to draw a rectangle of the layer you selected.
- Draw a rectangle by clicking the left mouse button twice.

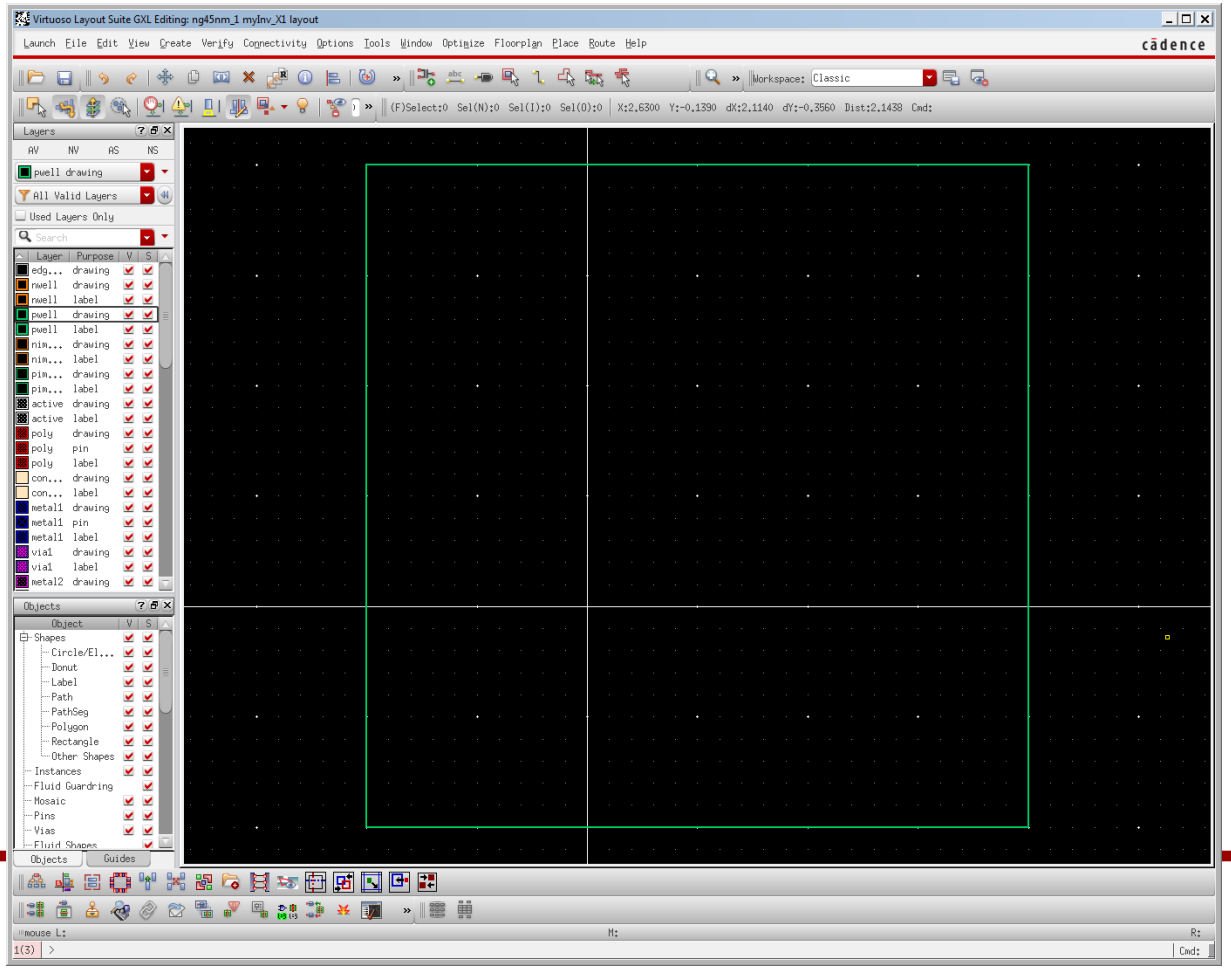
How to Draw Objects

- Press “ESC” to stop drawing rectangles.
- Click the rectangle you just drew.
- Press “q” to see the property of the rectangle.
- You can fine-control the coordinates in this window.
- Click “OK” to accept the change.



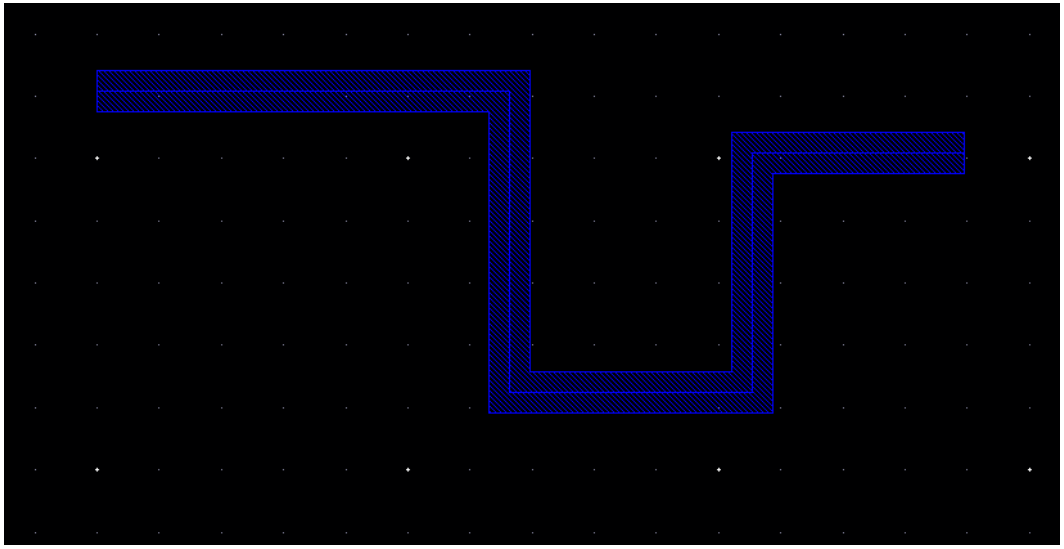
How to Draw Objects

- Press “f” to zoom out.
- Click whitespace to unselect the rectangle.



How to Draw Objects

- Drawing wires using rectangles is pretty painful.
- Click “metal 1 – drawing” in the layer window.
- Press “p” or click “Create” → “Shape” → “Path”.
- Now you are ready to draw a path of metal 1. Its width is pre-defined in the technology file.
- Try to draw some paths. To finish, double click the left button.



How to Draw Objects

- Move: choose an object, press “m”, and move it. Or, click whitespace to unselect, press “m”, and click and move an object.
- Copy: Click whitespace to unselect, press “c”, click the object you want to copy, and paste it.
- Stretch: click whitespace to unselect. Press “s” and stretch a boundary of an object.
- Ruler: press “k”.
- Clear ruler: shift+k.
- Merge: select two objects of the same type crossing each other and press “shift+m”. It will create a polygon object.
- Save: F2

Design Rules

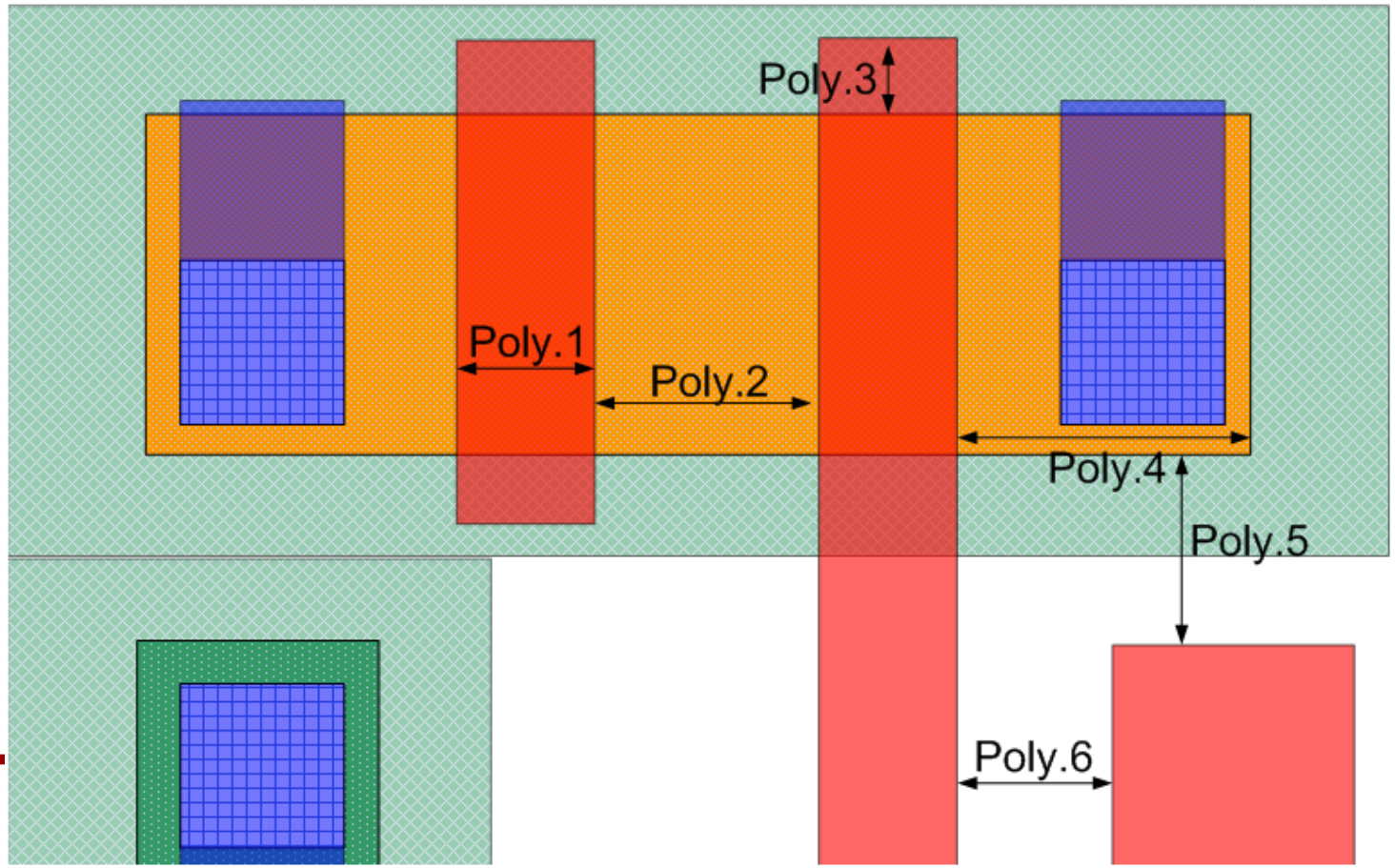
- See the following page:
  - http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

- Click each layer under “Design Rules”.

Design Rules

FreePDK45:PolyRules

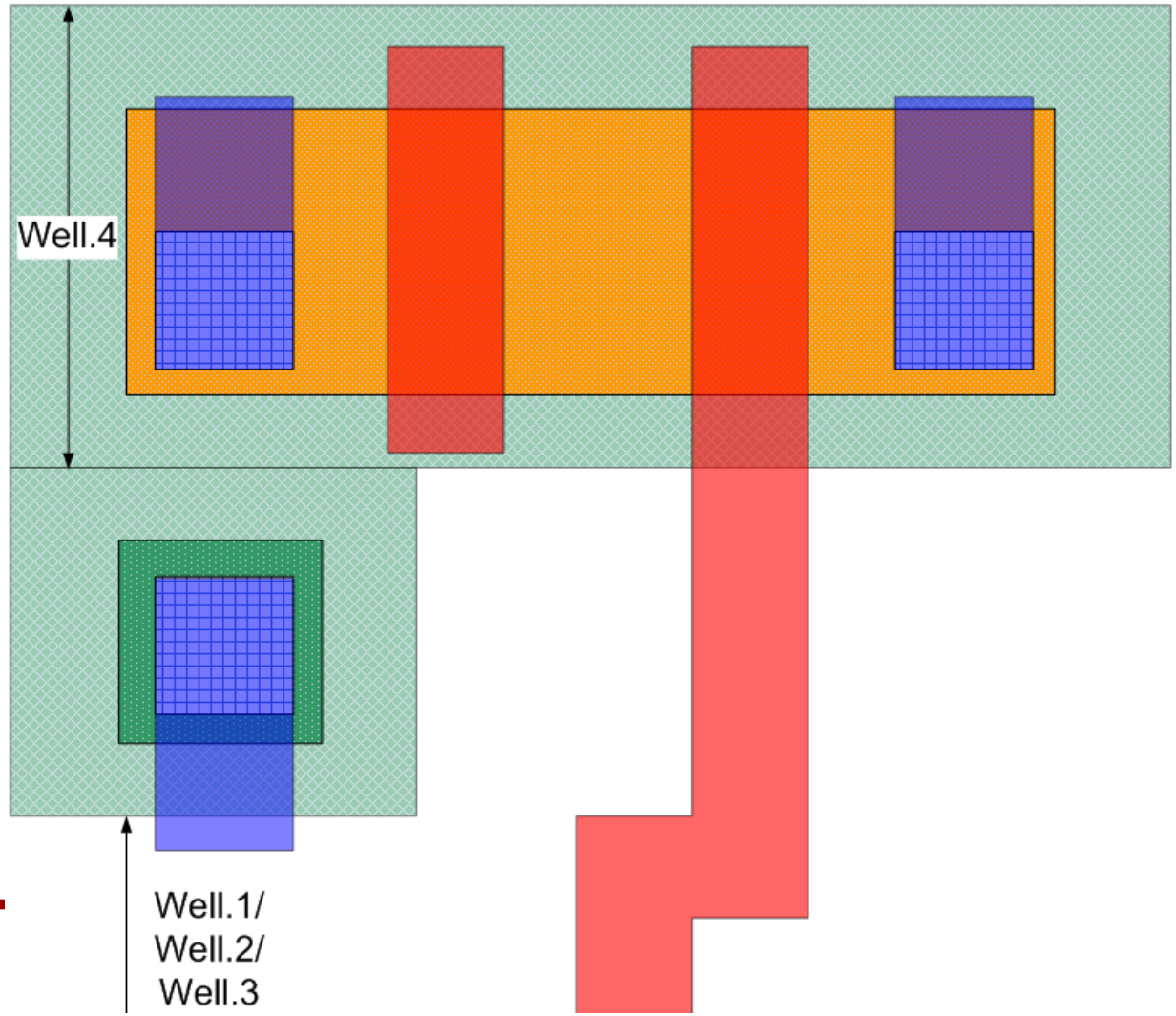
Rule	Value	Description
POLY.1	50 nm	Minimum width of poly
POLY.2	140 nm	Minimum spacing of poly AND active
POLY.3	55 nm	Minimum poly extension beyond active
POLY.4	70 nm	Minimum enclosure of active around gate
POLY.5	50 nm	Minimum spacing of field poly to active
POLY.6	75 nm	Minimum Minimum spacing of field poly



Design Rules

FreePDK45:WellRules

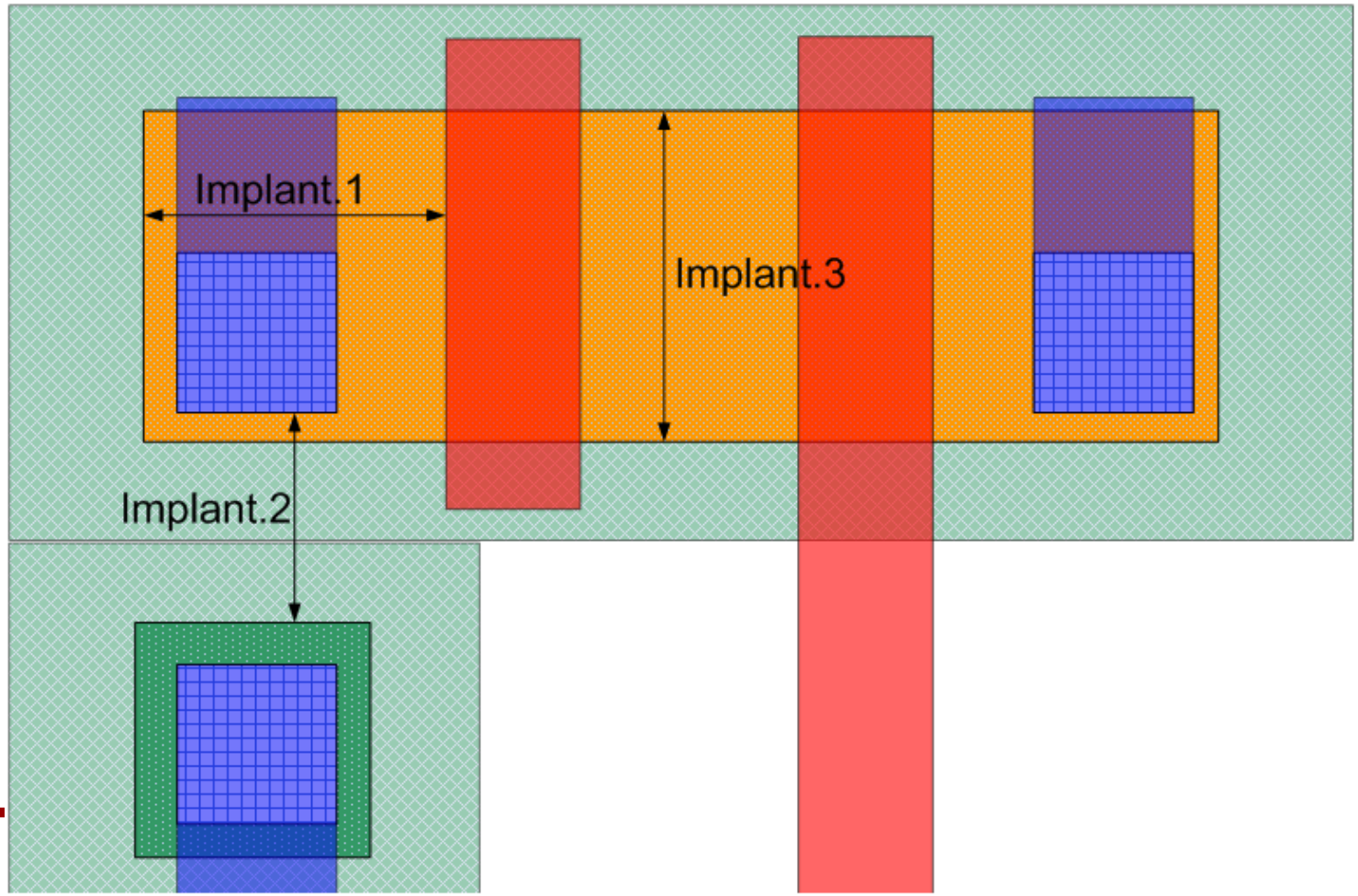
Rule	Value	Description
WELL.1	none	saveDerived: nwell/pwell must not overlap
WELL.2	225 nm	Minimum spacing of nwell/pwell at different potential
WELL.3	135 nm	Minimum spacing of nwell/pwell at the same potential
WELL.4	200 nm	Minimum width of nwell/pwell



Design Rules

FreePDK45:ImplantRules

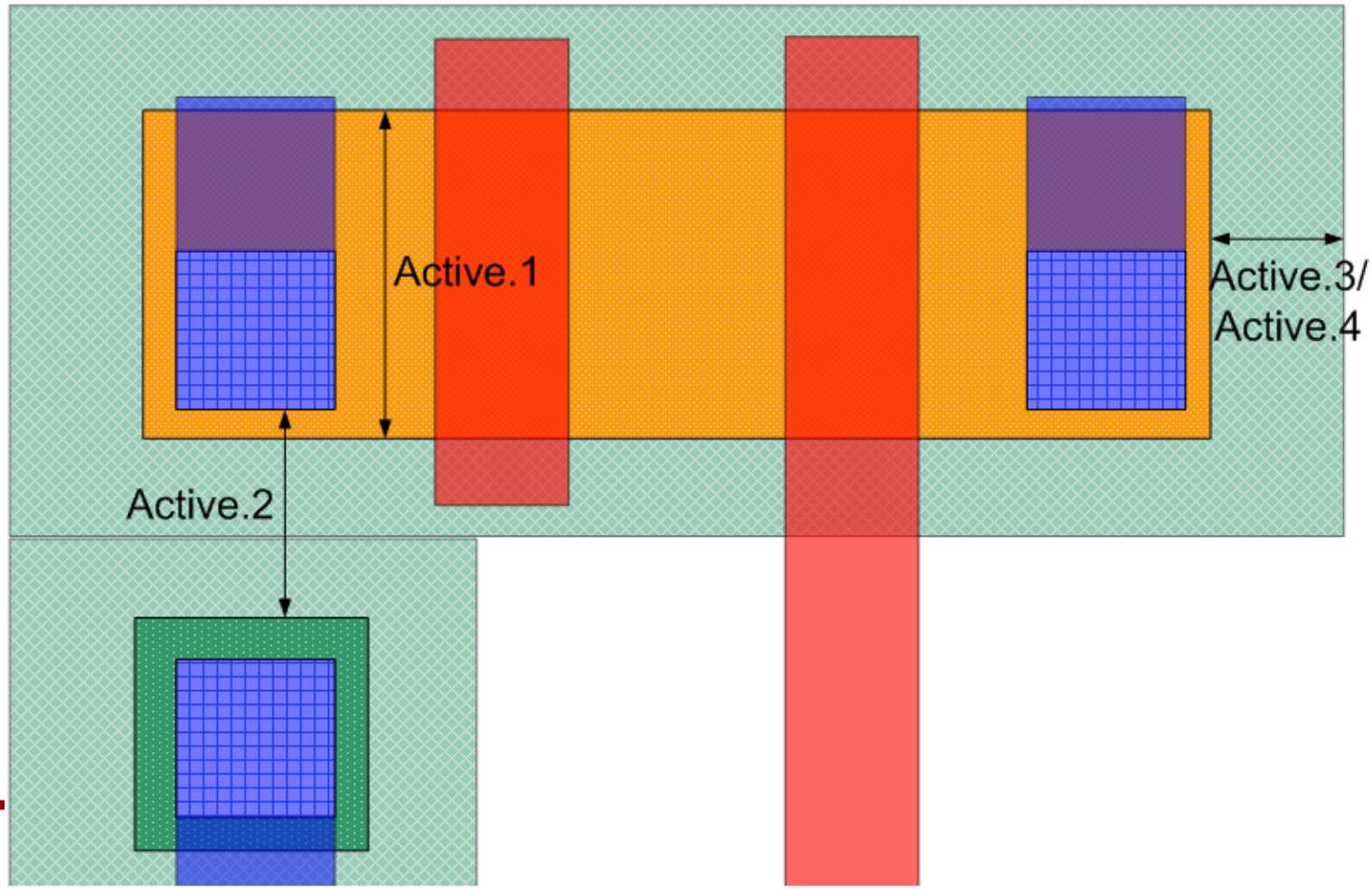
Rule	Value	Description
IMPLANT.1	70 nm	Minimum spacing of nimplant/ pimplant to channel
IMPLANT.2	25 nm	Minimum spacing of nimplant/ pimplant to contact
IMPLANT.3/4	45 nm	Minimum width/ spacing of nimplant/ pimplant
IMPLANT.5	none	Nimplant and pimplant must not overlap



Design Rules

FreePDK45:ActiveRules

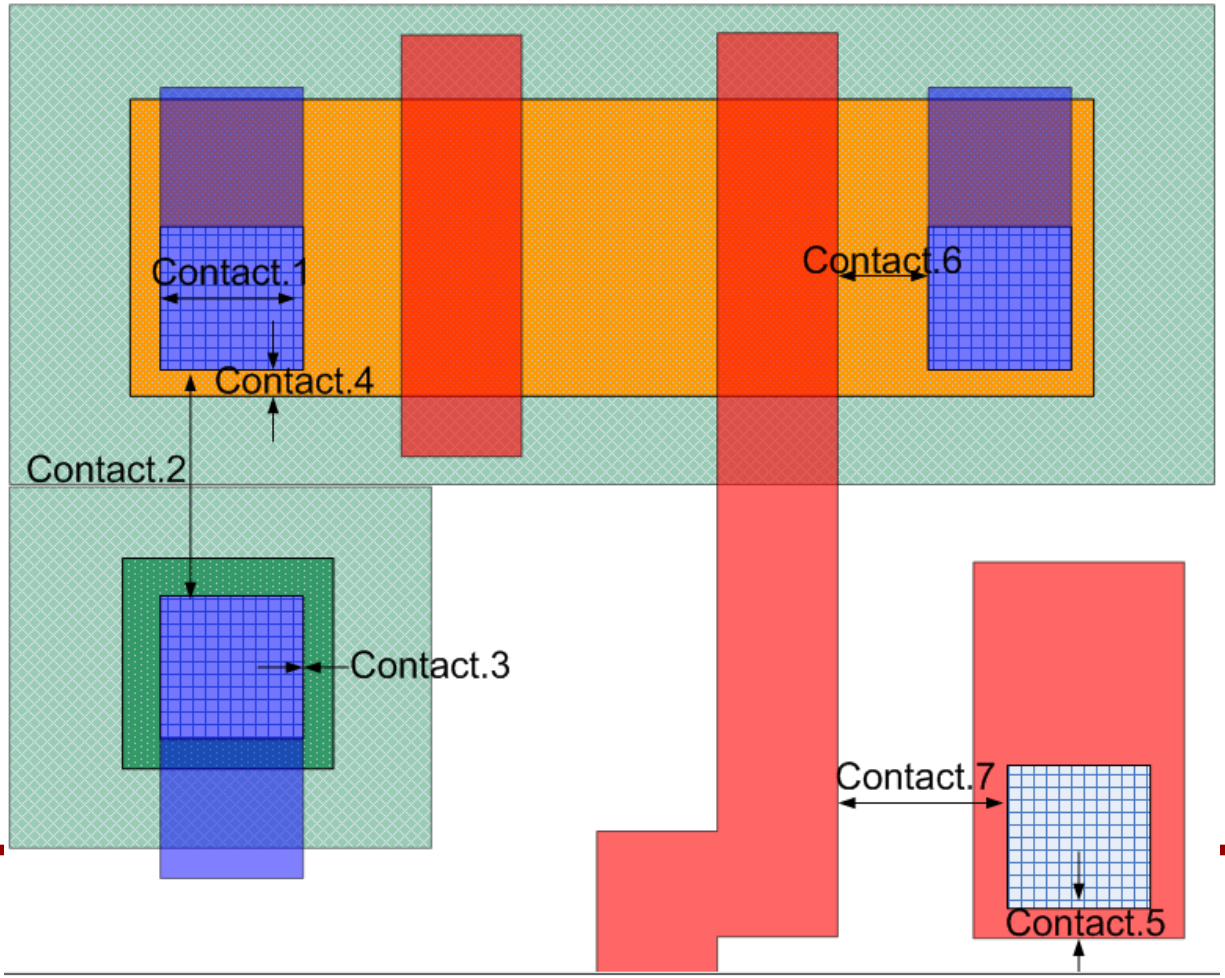
Rule	Value	Description
ACTIVE.1	90 nm	Minimum width of active
ACTIVE.2	80 nm	Minimum spacing of active
ACTIVE.3	55 nm	Minimum enclosure/spacing of nwell/pwell to active
ACTIVE.4	none	saveDerived: active must be inside nwell or pwell



Design Rules

FreePDK45:ContactRules

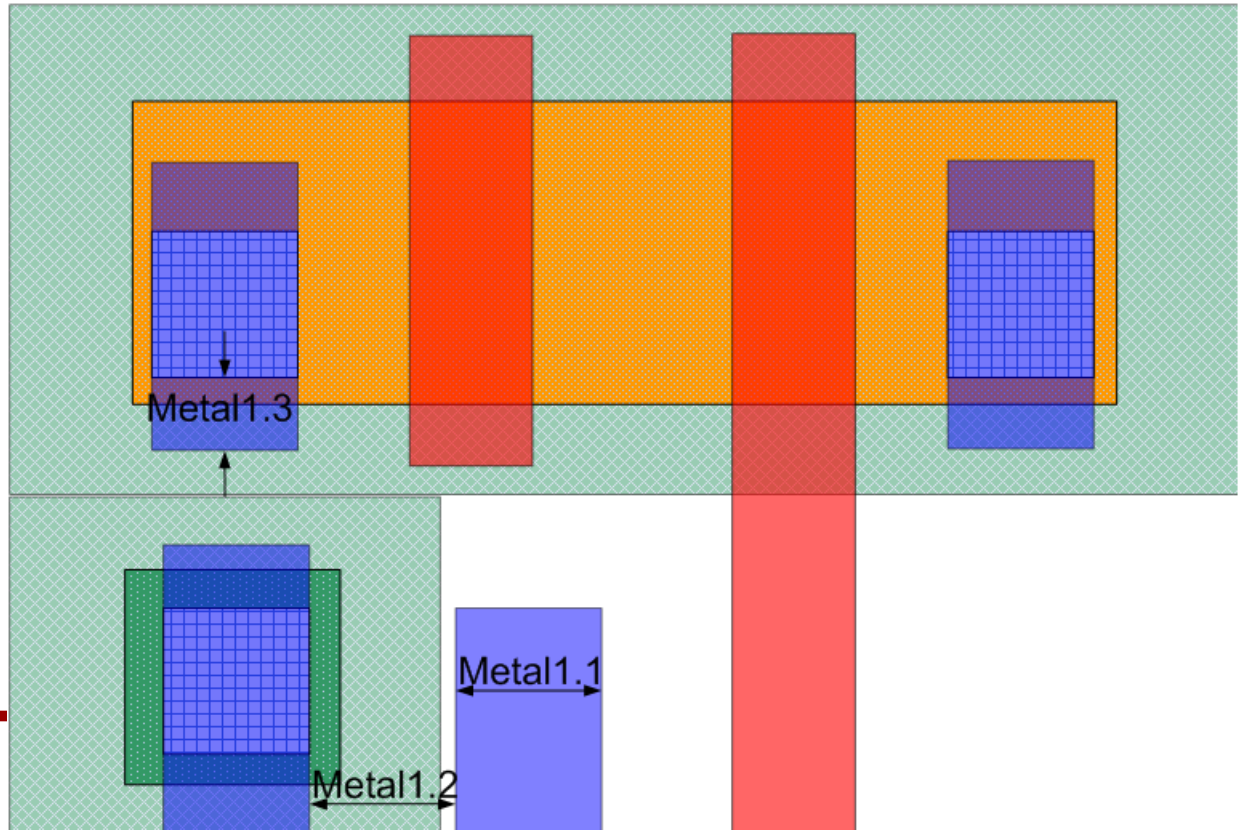
Rule	Value	Description
CONTACT.1	65 nm	Minimum width of contact
CONTACT.2	75 nm	Minimum spacing of contact
CONTACT.3	none	saveDerived: contact must be inside active or poly or metal1
CONTACT.4	5 nm	Minimum enclosure of active around contact
CONTACT.5	5 nm	Minimum enclosure of poly around contact
CONTACT.6	35 nm	Minimum spacing of contact and gate
CONTACT.7	90 nm	Minimum spacing of contact and poly



Design Rules

FreePDK45:Metal1Rules

Rule	Value	Description
METAL1.1	65 nm	Minimum width of metal1
METAL1.2	65 nm	Minimum spacing of metal1
METAL1.3	35 nm	Minimum enclosure around contact on two opposite sides
METAL1.4	35 nm	Minimum enclosure around via1 on two opposite sides
METAL1.5	90 nm	Minimum spacing of metal wider than 90 nm and longer than 900 nm
METAL1.6	270 nm	Minimum spacing of metal wider than 270 nm and longer than 300 nm
METAL1.7	500 nm	Minimum spacing of metal wider than 500 nm and longer than 1.8um
METAL1.8	900 nm	Minimum spacing of metal wider than 900 nm and longer than 2.7 um
METAL1.9	1500 nm	Minimum spacing of metal wider than 1500 nm and longer than 4.0 um



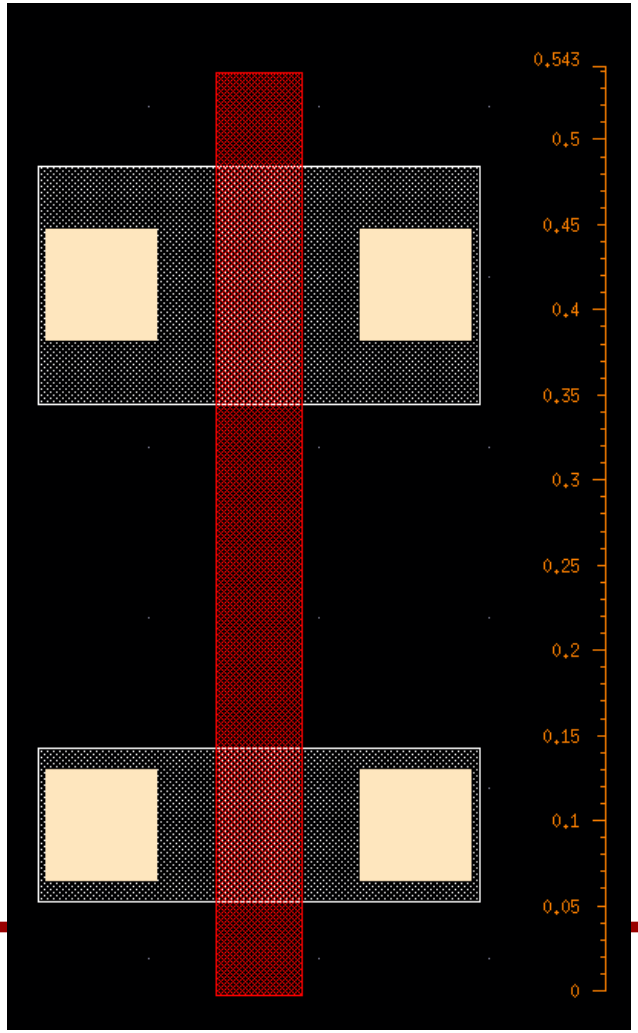
Design Rules

FreePDK45:Via1Rules

Rule	Value	Description
VIA1.1	65 nm	Minimum width of via1
VIA1.2	75 nm	Minimum spacing of via1
VIA1.3	none	saveDerived: via1 must be inside metal1
VIA1.4	none	saveDerived: via1 must be inside metal2

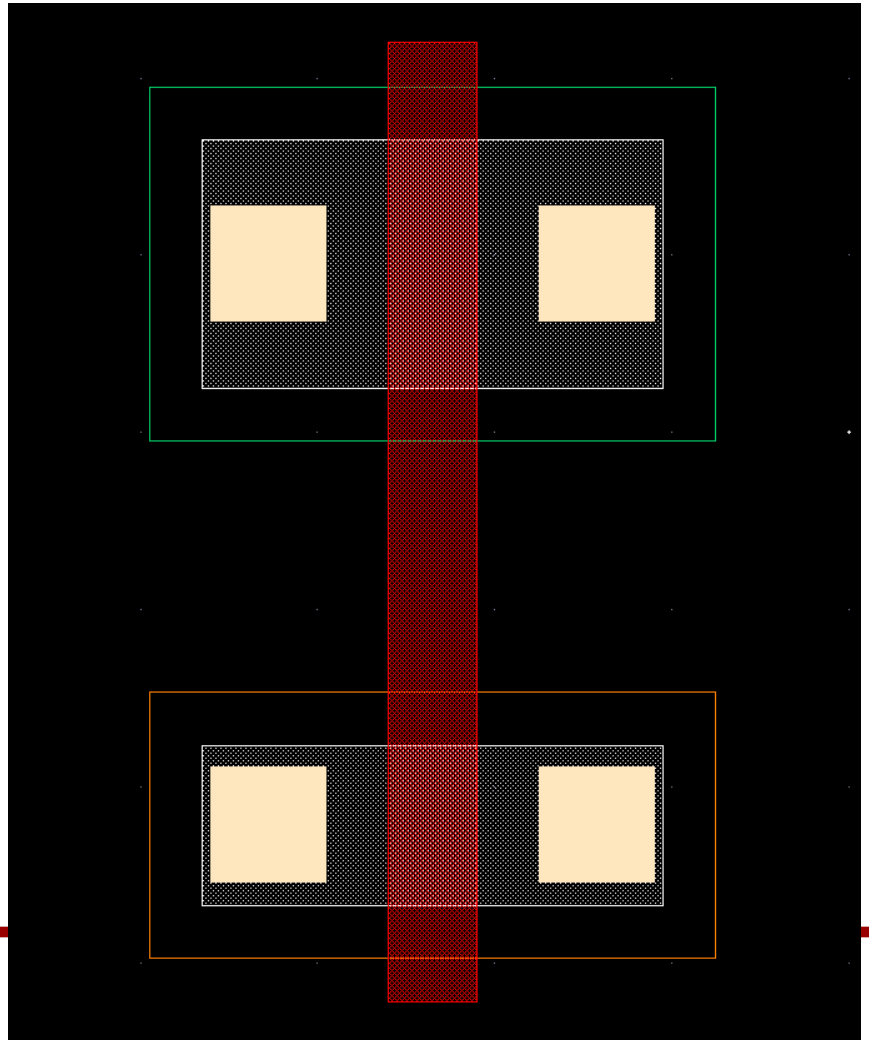
Example – Inverter Layout

1. poly, active, and contact (Ln=50nm, Wn=90nm, Lp=50nm, Wp=140nm).



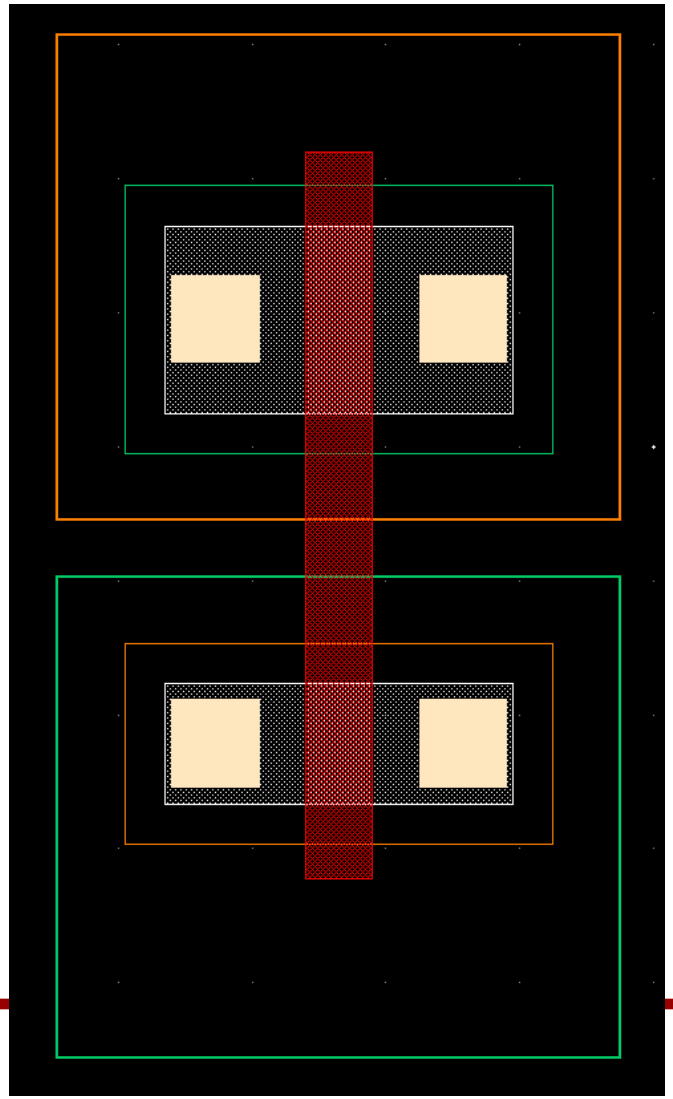
Example – Inverter Layout

2. pimplant and nimplant.



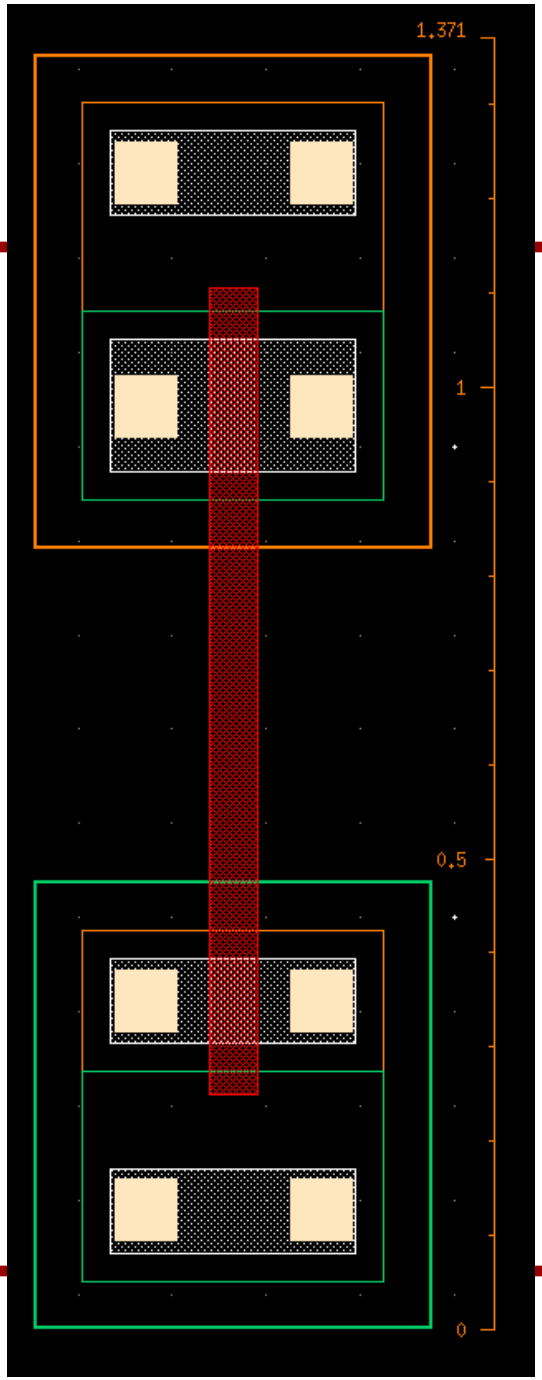
Example – Inverter Layout

3. pwell and nwell



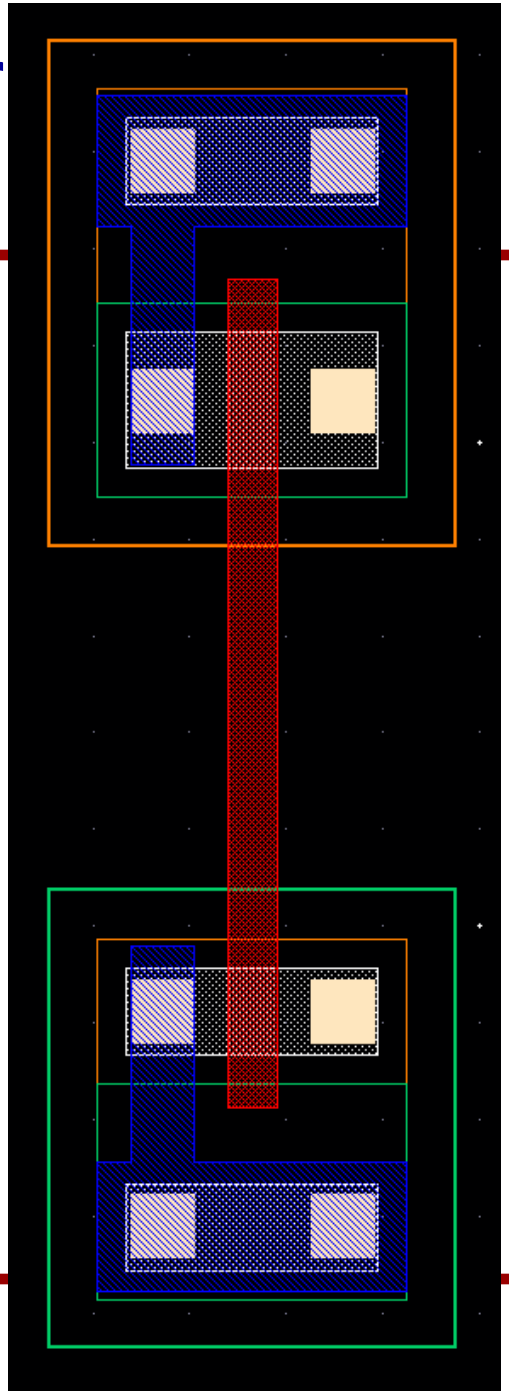
Example – Inverter Layout

4. body contacts.



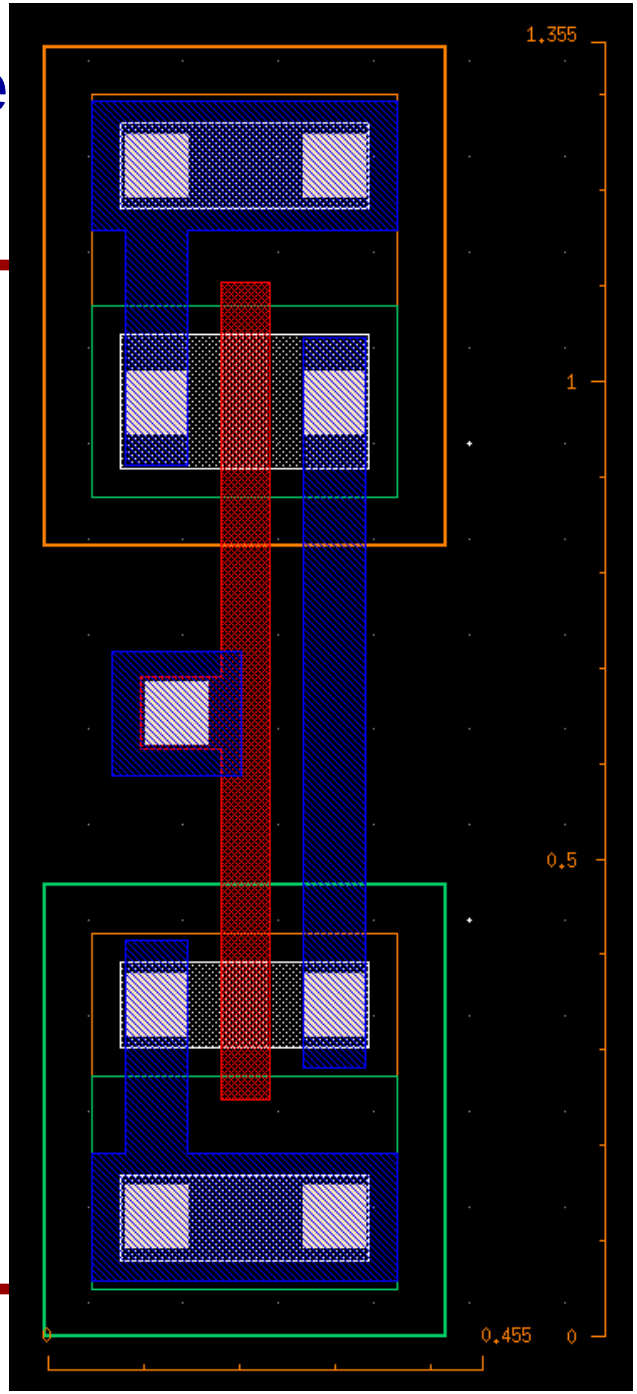
Example – Inverter Layout

5. VDD and VSS.



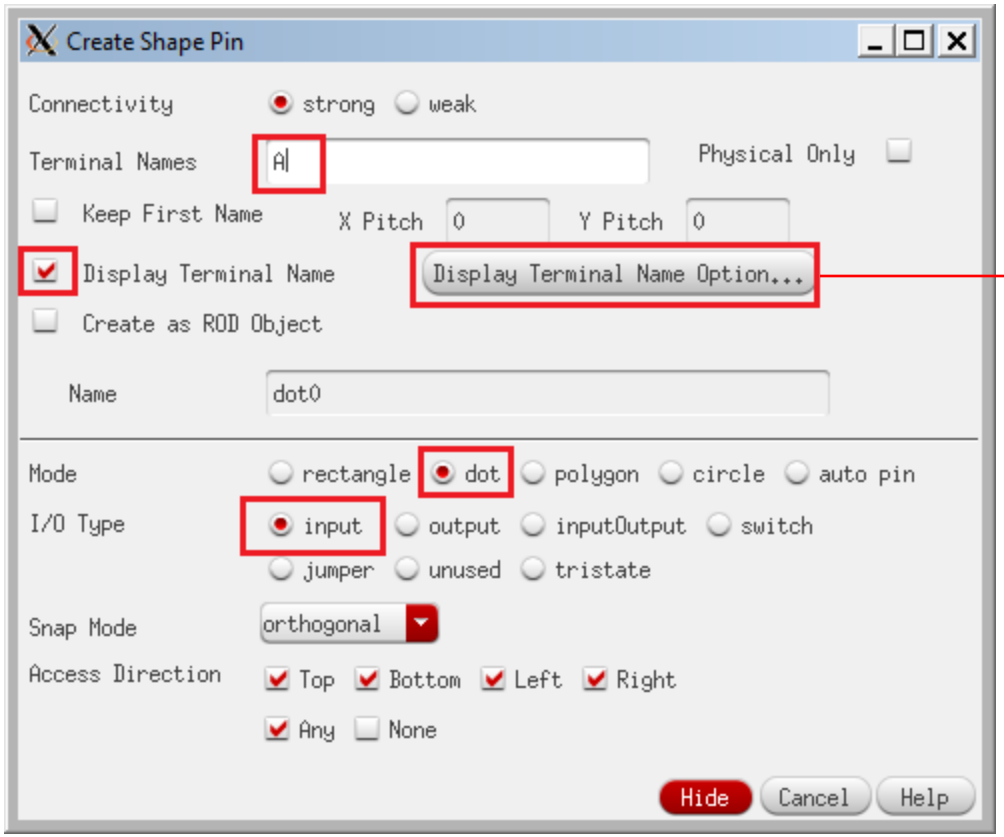
Example – Inverte Layout

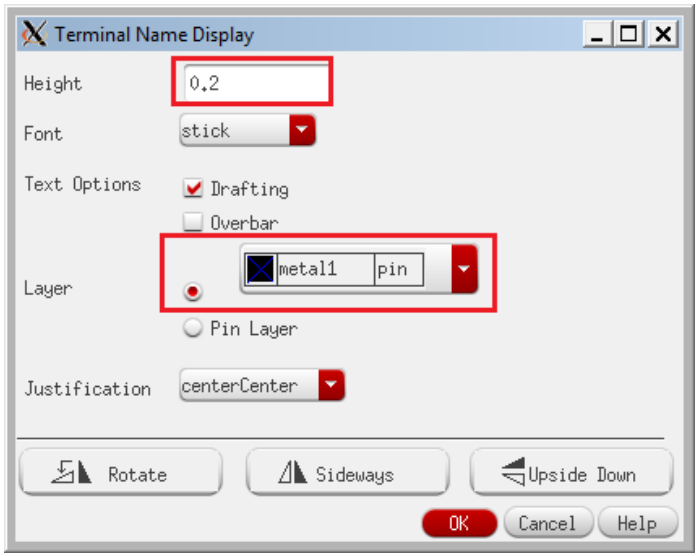
6. Input and output.



Example – Inverter Layout

7. Create pins (A, ZN, VDD, VSS).
   - “Create” → “Pin…”



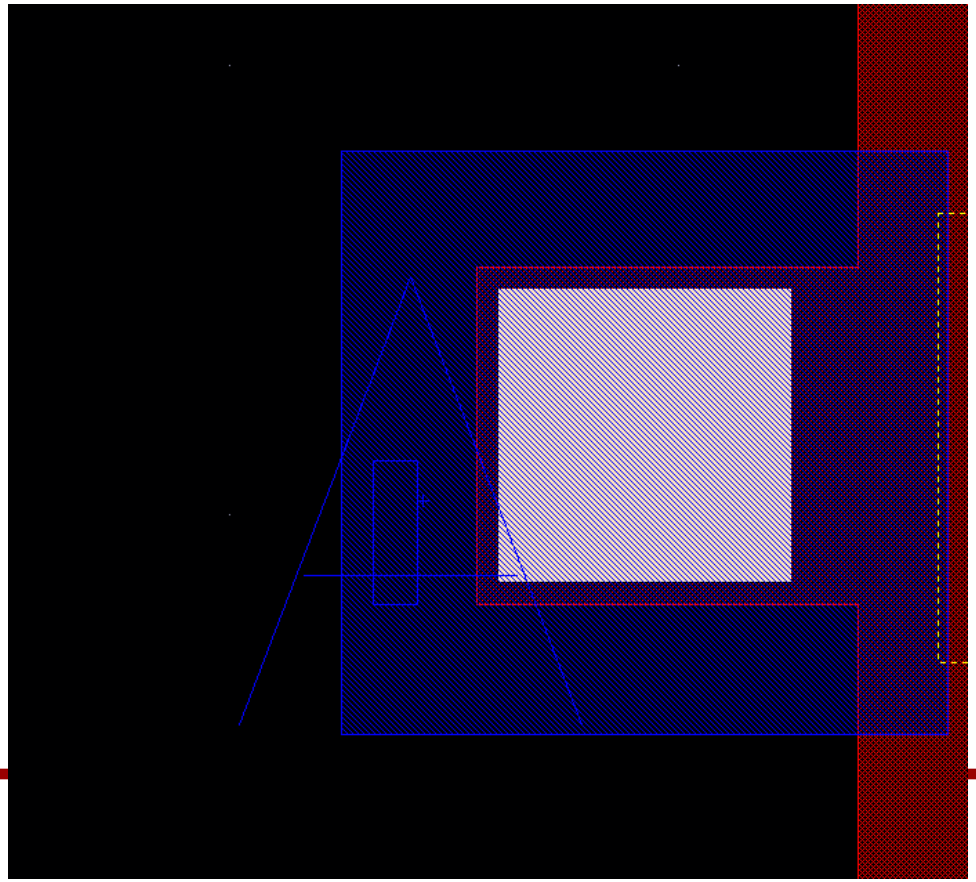


Example – Inverter Layout

7. Create pins (A, ZN, VDD, VSS).

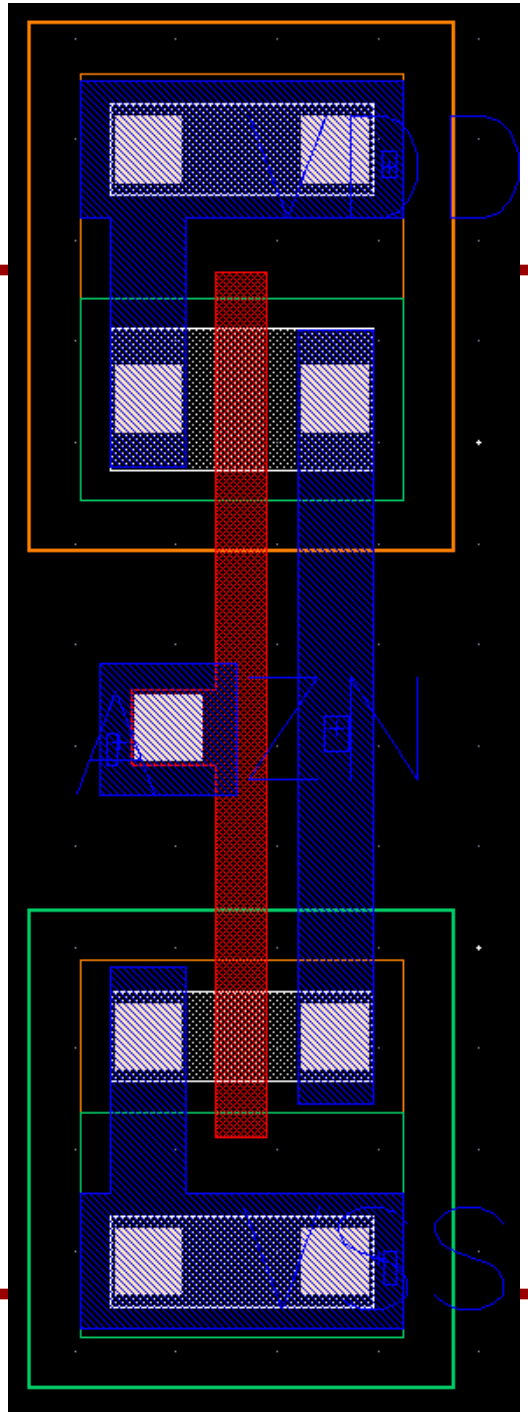
- Then, create a small rectangle inside the target pin.

- Make sure that the + mark of the pin is placed inside the wire object.



Example – Inverter Layout

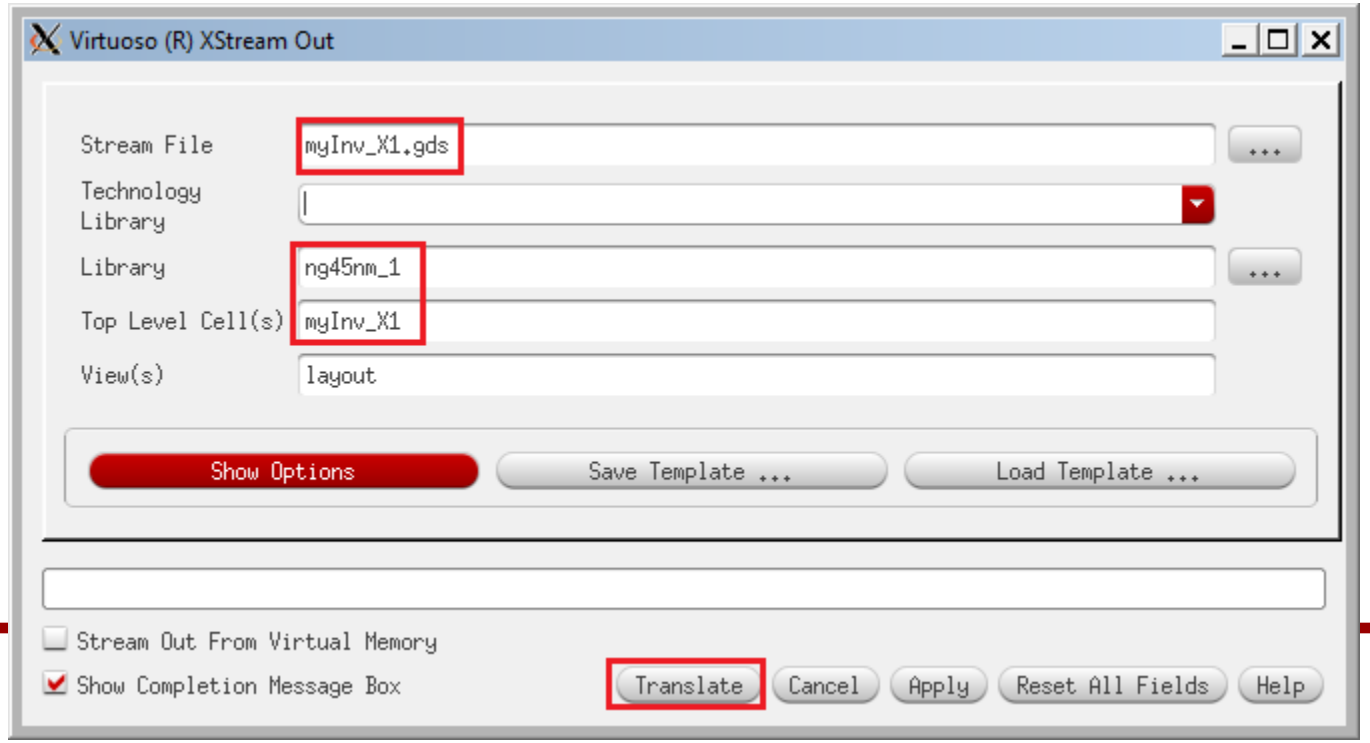
7. Create pins (A, ZN, VDD, VSS).
   - A: input
   - ZN: output
   - VDD, VSS: inputOutput



Example – Inverter Layout

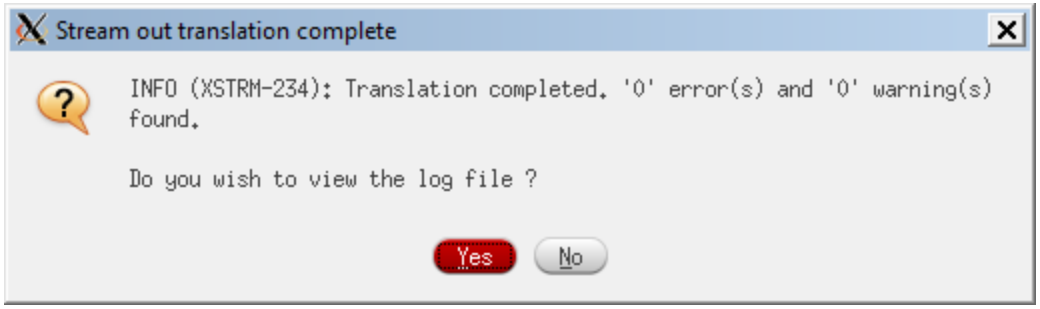
8. Save the design.

9. Export the design into gdsii.
   - In CIW, click “File” → “Export” → “Stream…”.
   - Click “Translate”.



Example – Inverter Layout

10. Export



Example – Inverter
DRC

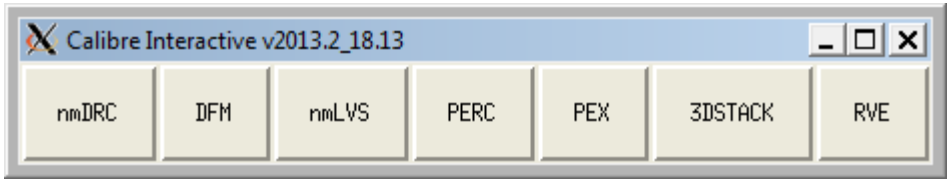
1. Let’s run DRC.

2. Source calibre.sh.

   > source sh/calibre.sh

3. Run Calibre.

   > calibre -gui

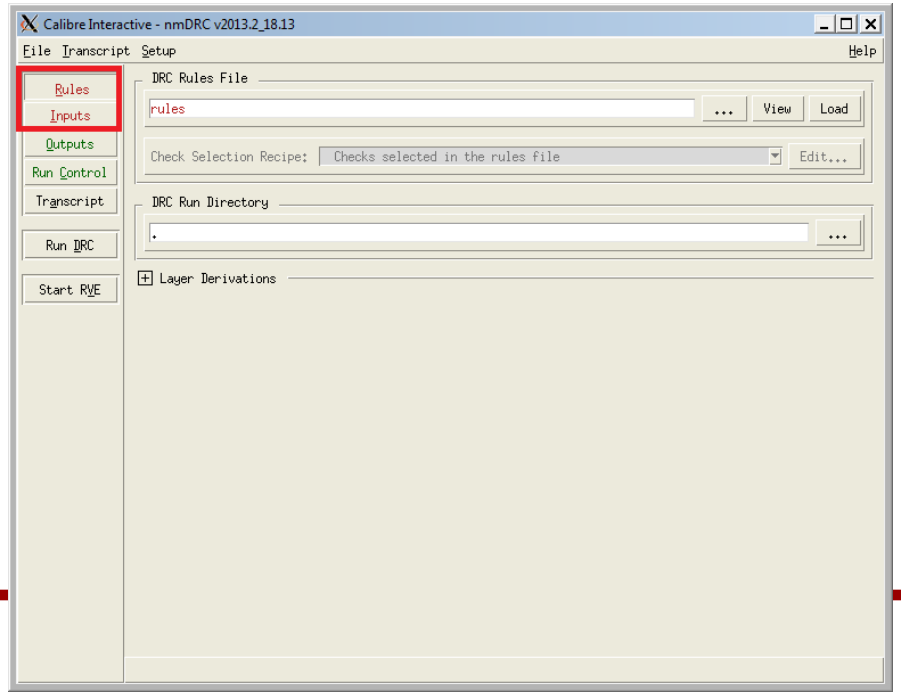


Example – Inverter
DRC

4. Click “nmDRC”.

5. Close the “Load Runset File” window.

6. The red texts mean that some files in the input tabs are missing.

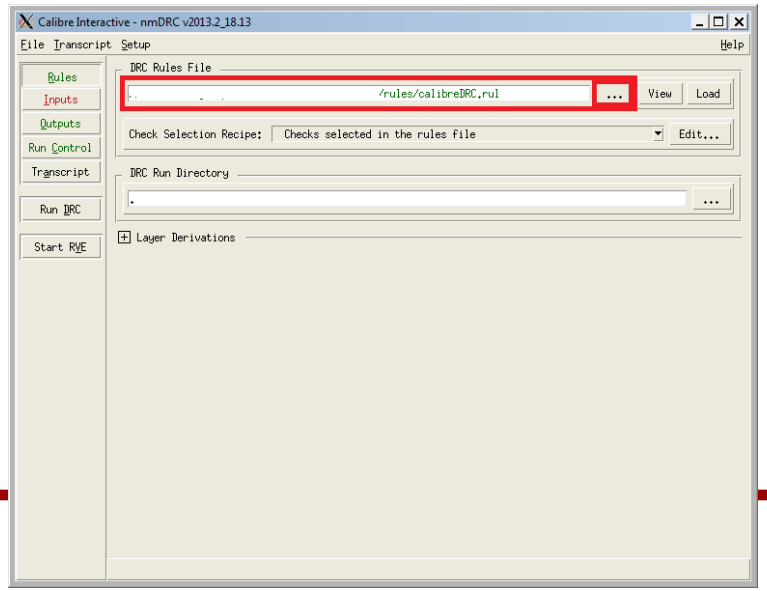


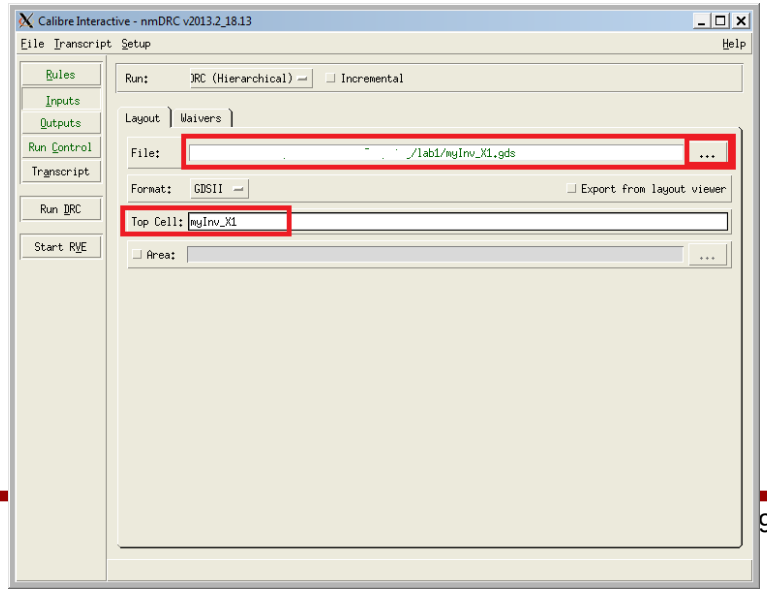
Example – Inverter
DRC

7. Click “Rules”, and “…” in the “DRC Rules File” and choose “rules/calibreDRC.rul”.

8. Click “Inputs” and “…” in the “File” and choose the gdsii file you exported.

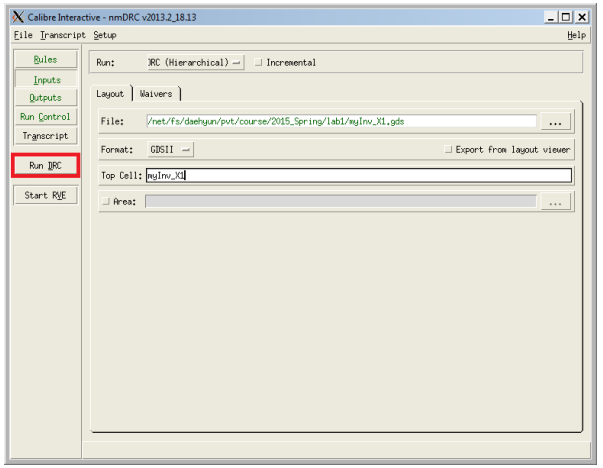
9. Enter the name of your inverter cell.





Example – Inverter
DRC

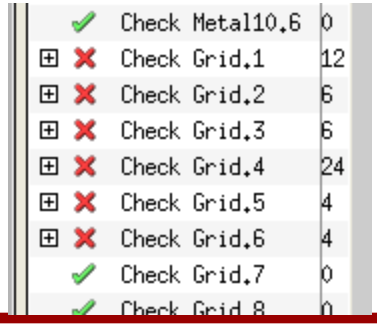
10. Click “Run DRC” to run Calibre DRC.



11. It will show two windows.
  - DRC Summary Report
  - Calibre – RVE

12. Close the Summary Report window.

13. See the RVE window. I have the following errors.



Example – Inverter
DRC

14. Ignore the “Check Grid.#” errors.

15. If you have any errors, fix them in the layout window (Virtuoso), re-export, and run DRC again.

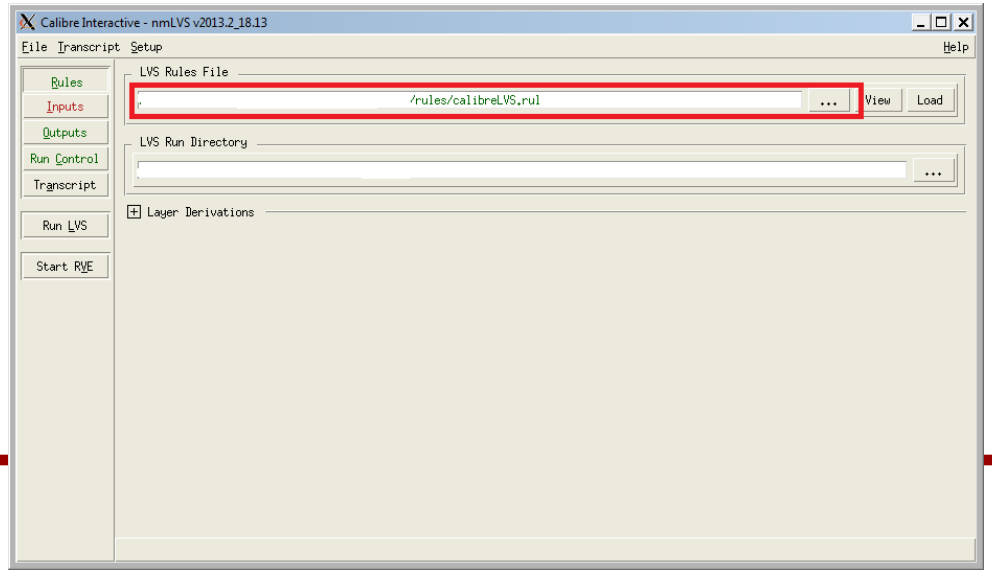
Example – Inverter
LVS

1. Let's run LVS.

2. Click "nmLVS" in the main Calibre window.

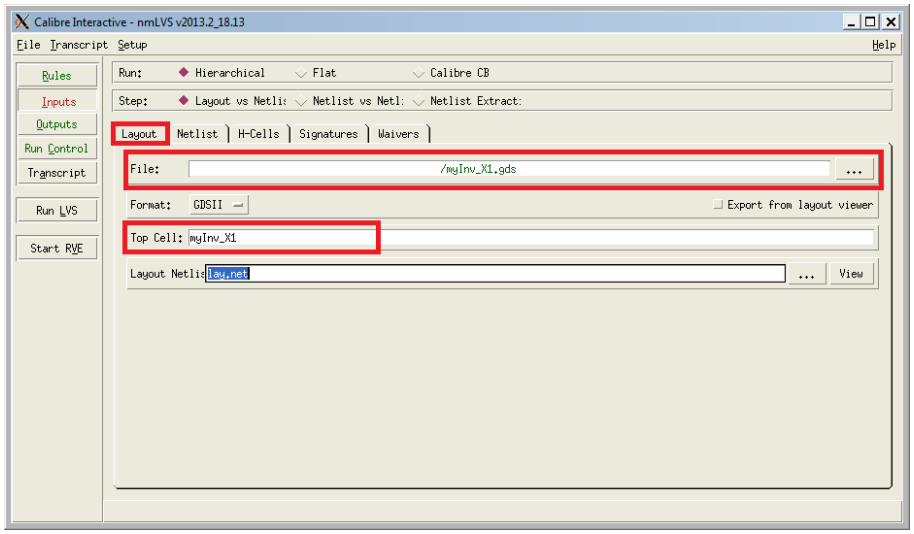
3. Close the "Load Runset File" window.

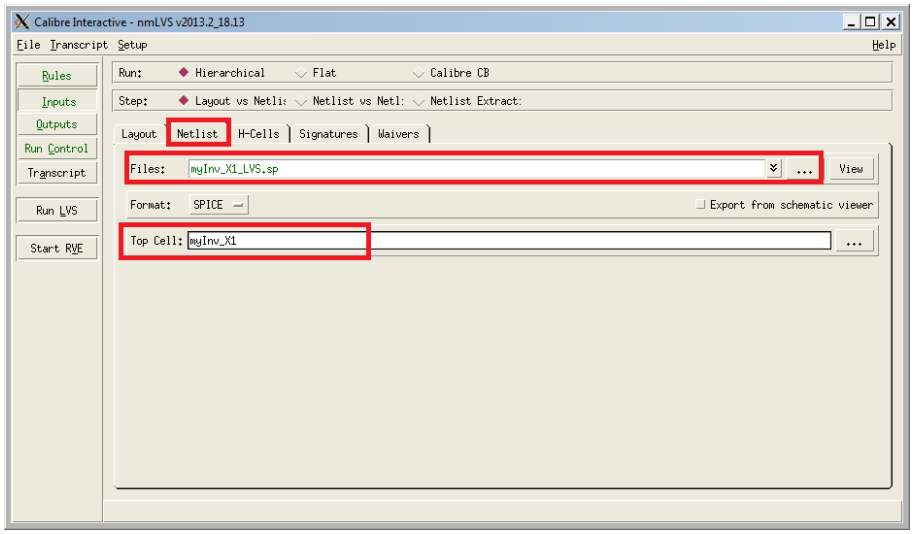
4. Select the "calibreLVS.rul" in the LVS rule file section.



Example – Inverter
LVS

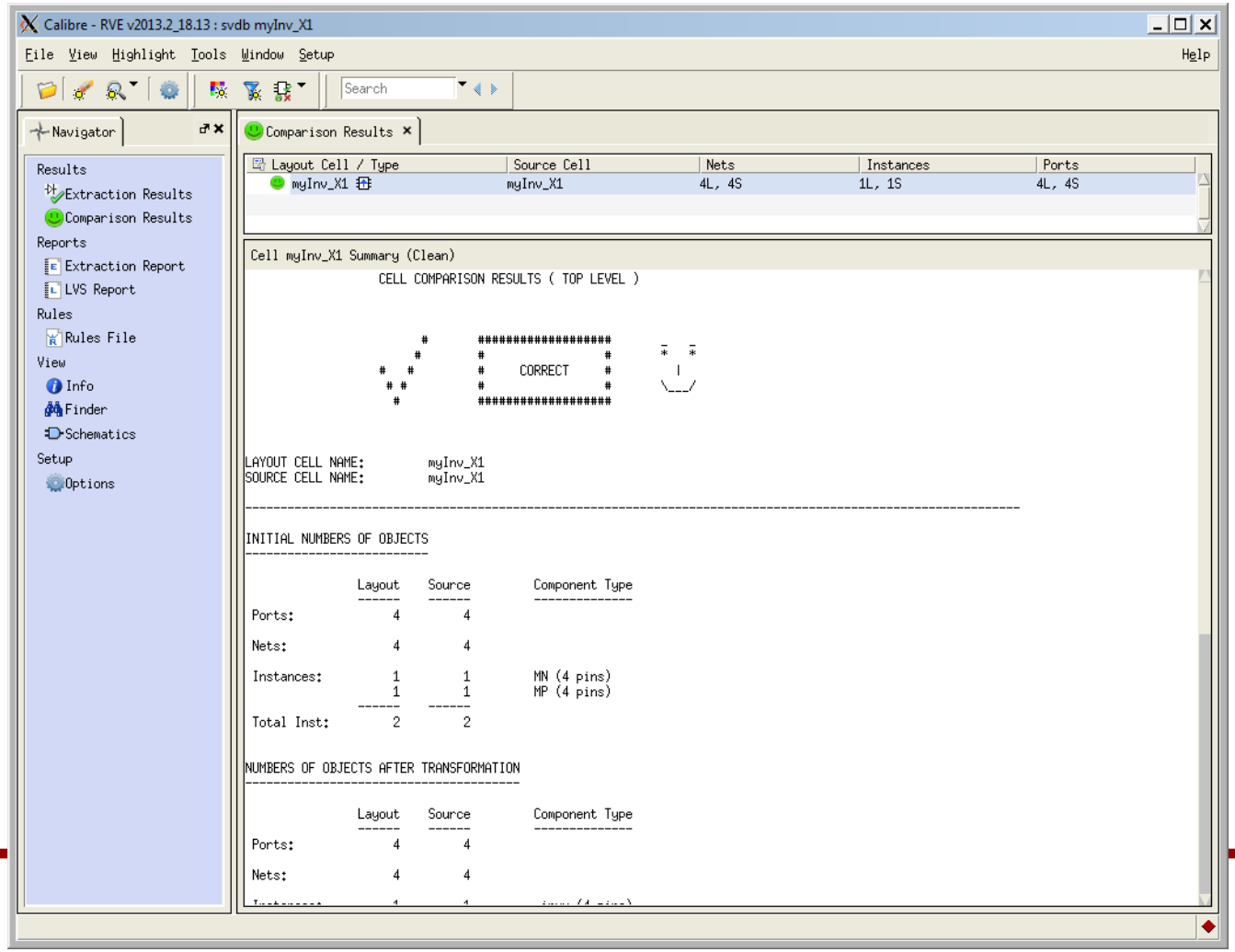
5. Click “Inputs”. We need to enter the name of the file containing the layout and the netlist file.





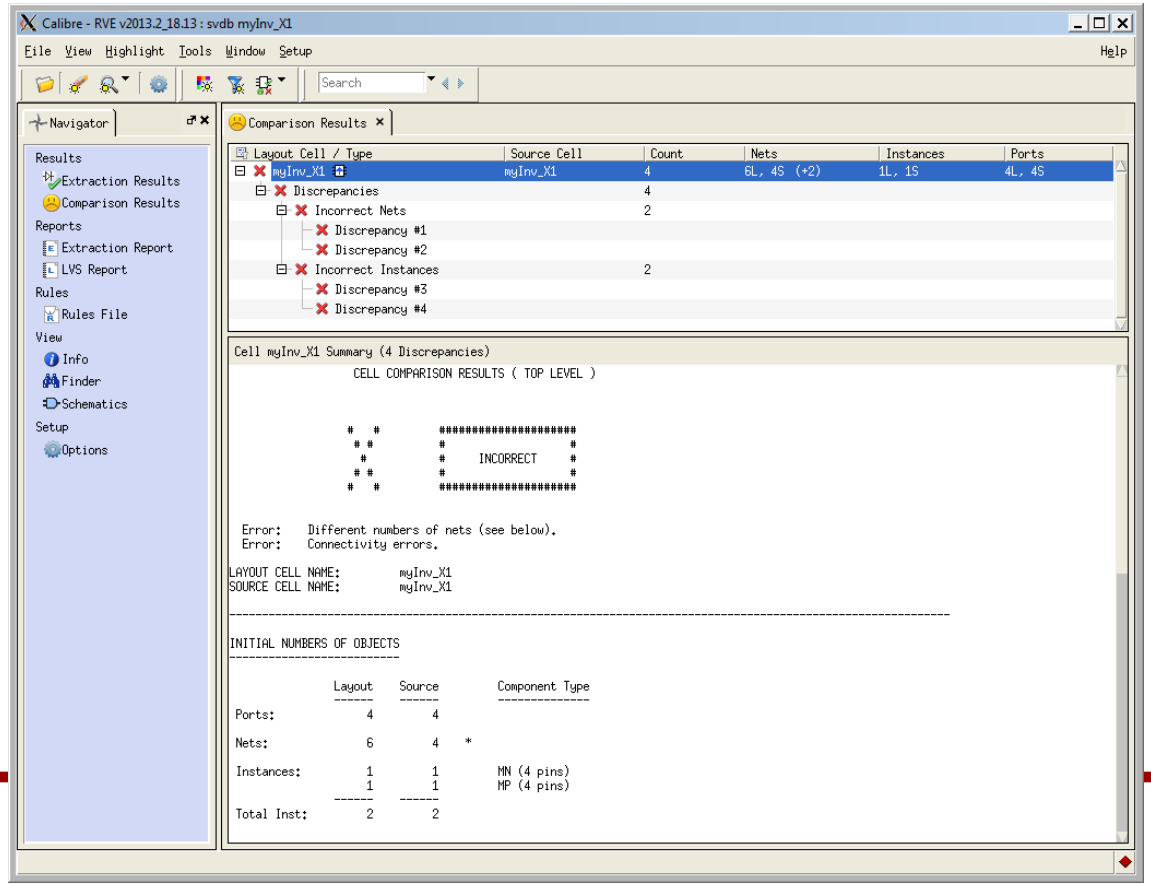
Example – Inverter
LVS

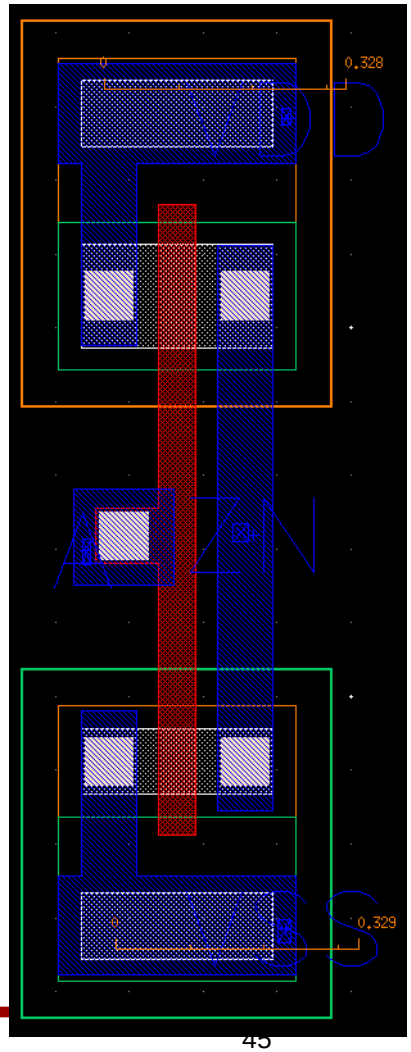
6. If everything is good, you will see the following window:



Example – Inverter
LVS

7. I'll remove the body contacts and see what happens.





Example – Inverter
LVS

8. First of all, match “Ports”, which are primary inputs and outputs.

	Layout	Source	Component Type
Ports:	4	4	

9. Then, match “Instances”.

Instances:	1	1	MN (4 pins)
	1	1	MP (4 pins)
Total Inst:	2	2	

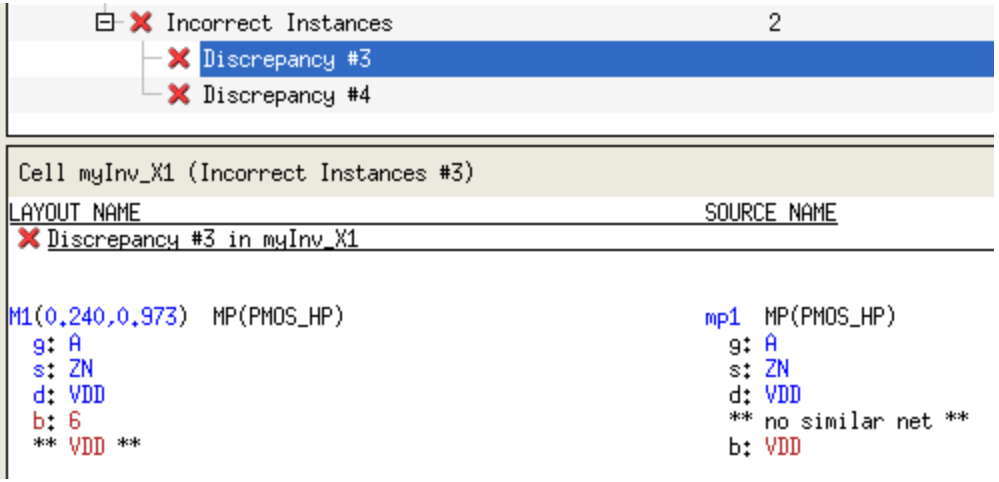
10. Then, match “Nets”.

Nets:	6	4	*

- In the source (the SPICE netlist), there are four nets, which makes sense (A, ZN, VDD, VSS).
- In the layout, however, there are six nets, so something is wrong in the layout.

Example – Inverter
LVS

11. Click “Discrepancy #”.



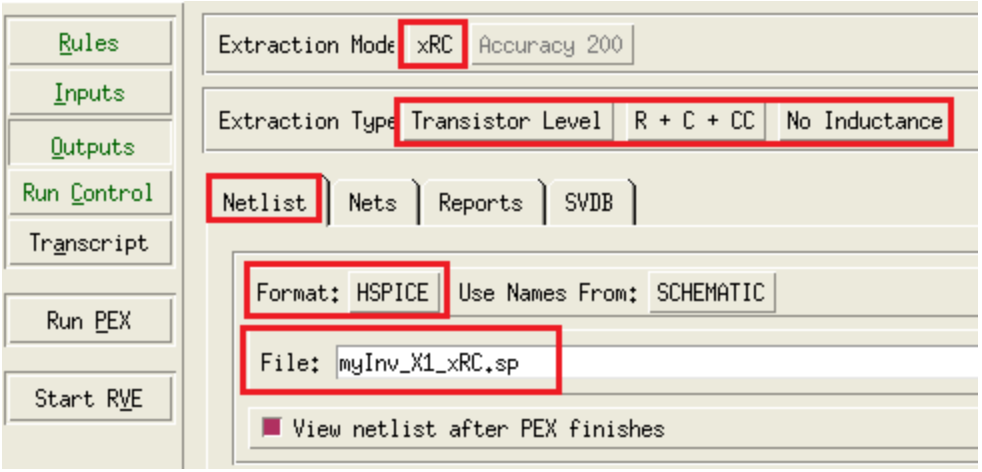
- It says that the body (substrate) of M1 (the PMOS transistor) in the layout is connected to net “6”, but that in the source is connected to “VDD”.

- From this, we know that the body of M1 is NOT connected VDD.

Example – Inverter
xRC

1. Let's run xRC.
2. Click "PEX" in the Calibre main window.

Example – Inverter
xRC



3. Click “Run PEX”.

Example – Inverter
xRC

4. xRC netlist (myInv_X1_xRC.sp)

```
* File: myInv_X1_xRC.sp
* Created: Mon Feb 16 13:29:12 2015
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "myInv_X1_xRC.sp.pex"
.subckt myInv_X1  A VSS VDD ZN
*
* ZN    ZN
* VDD   VDD
* VSS   VSS
* A     A
mn1 N_ZN_mn1_d N_A_mn1_g N_VSS_mn1_s N_VSS_mn1_b NMOS_HP L=5e-08 W=9e-08
+ AD=9.45e-15 AS=9.45e-15 PD=3.9e-07 PS=3.9e-07
mp1 N_ZN_mp1_d N_A_mp1_g N_VDD_mp1_s N_VDD_mp1_b PMOS_HP L=5e-08 W=1.4e-07
+ AD=1.47e-14 AS=1.47e-14 PD=4.9e-07 PS=4.9e-07
*
.include "myInv_X1_xRC.sp.MYINV_X1.pxi"
*
.ends
```

Example – Inverter SPICE Simulation

1. Let's run HSPICE for the inverter.

   > hspice myInv_X1_simul.sp

   > hspice myInv_X1_noRC_simul.sp

2. The following shows my result:

	Fall	Rise
Without RC	112.67ps	123.11ps
With parasitic RC	119.29ps	132.62ps
Difference	+6.62ps	+9.51ps